Magnetic Tunnel Junction based non-volatile Magnetoresistive RAM

S. Tehrani, M. Durlam, P. Naji, M. DeHerrera, E. Y. Chen, J. M. Slaughter, N. Rizzo, and B. Engel

Motorola Labs, Physical Sciences Research Laboratories
Tempe, Arizona- USA

This work is supported in part by DARPA

MOTOROLA LABS

Physical Sciences Research Labs

Outline

- MRAM attributes
- MRAM cell architecture
- Magnetic Tunnel Junction (MTJ) bit characteristics
- MTJ/CMOS integration challenges and results
- Integrated circuit demonstration results

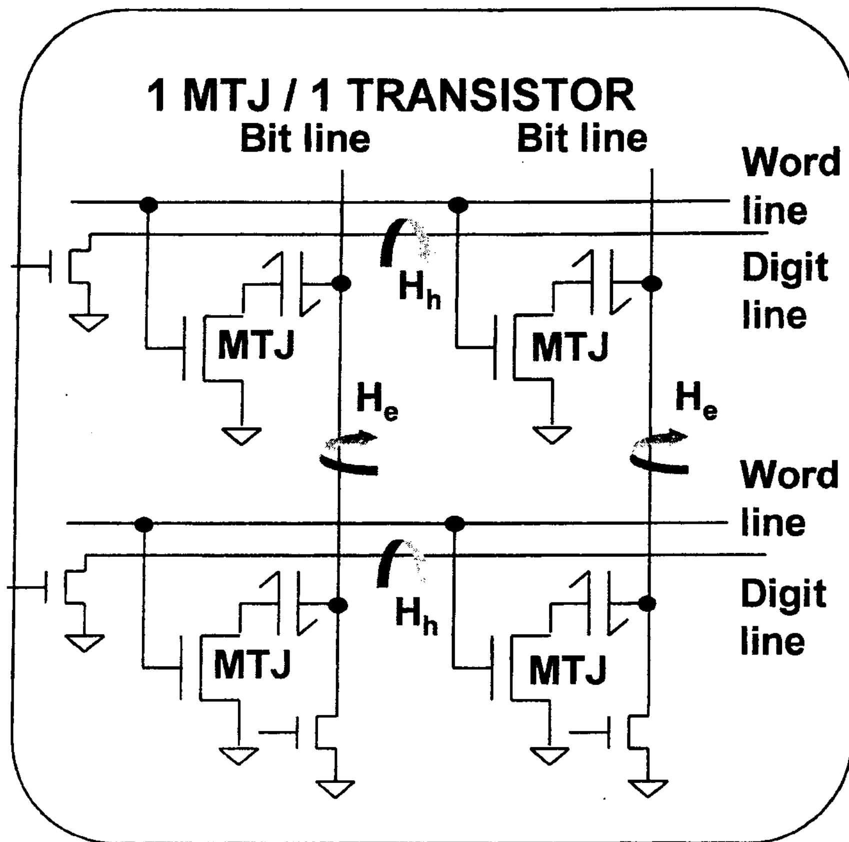
MOTOROLA LABS

Physical Sciences Research Labs

MTJ Memory Cell Architecture

Attributes:

- Nonvolatile
- High Density 8 - 20F^2
- No Refresh
- Nondestructive Read
- Low voltage operation
- Unlimited R/W endurance



Cell is defined by a single MTJ and a transistor

MOTOROLA LABS

Physical Sciences Research Labs

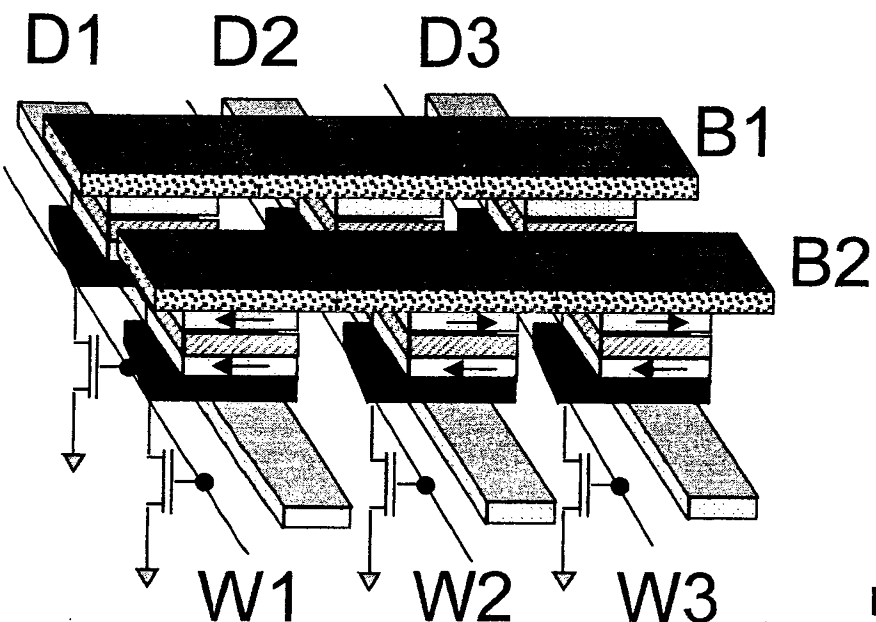
Technology Comparison

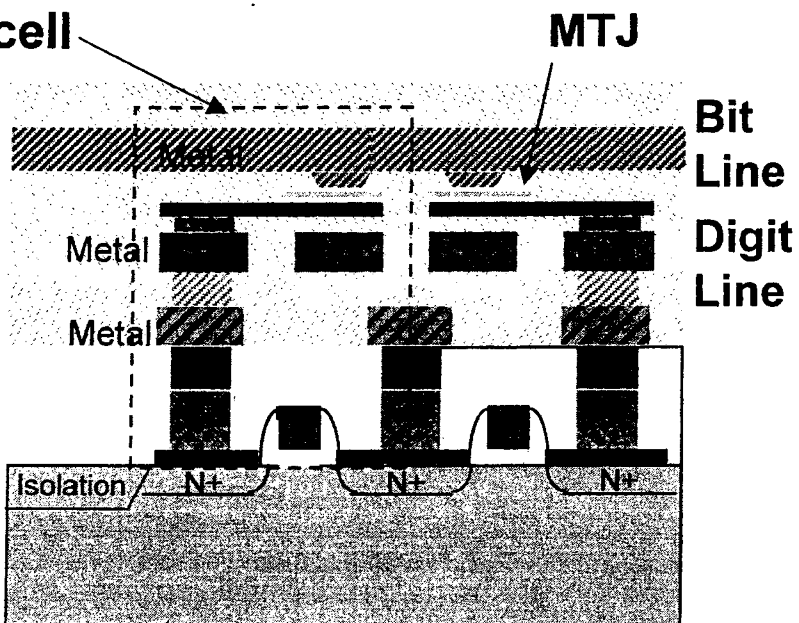
Attribute	*SRAM*	*DRAM*	*FLASH*	*FRAM*	Projected *MRAM*
Read Time	fast	mod.	mod.	mod.	mod.-fast
Write Time	fast	mod.	slow	mod.	mod.-fast
Non-Volatile	no	no	yes	destructive& fatigue	yes
Refresh	NA	ms	NA	NA	NA
Minimum Cell Size	large	small	small	medium	small
Low Voltage	yes	limited	no	limited	yes

MOTOROLA LABS

MTJ Memory Cell Architecture

Cross Point matrix of Bit and Digit lines





Magnetic Tunnel Junction (MTJ) MRAM

MOTOROLA LABS
Physical Sciences Research Labs

MTJ Memory Cell Architecture

State 1

MR (%)

35 30 25 20 15 10 5 0

-50 -30 -10 10 30 50

Easy Axis Fld (Oe)

State 0

Read Mode

Sense Current

Bit Line

NiFe

AlOx

IrMn/ NiFe

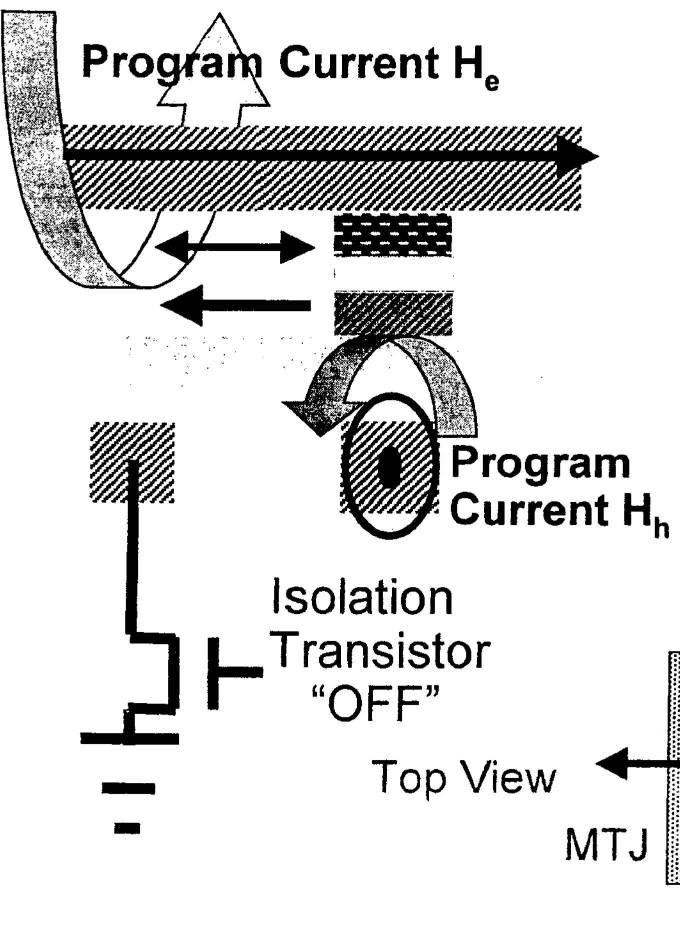
Digit Line

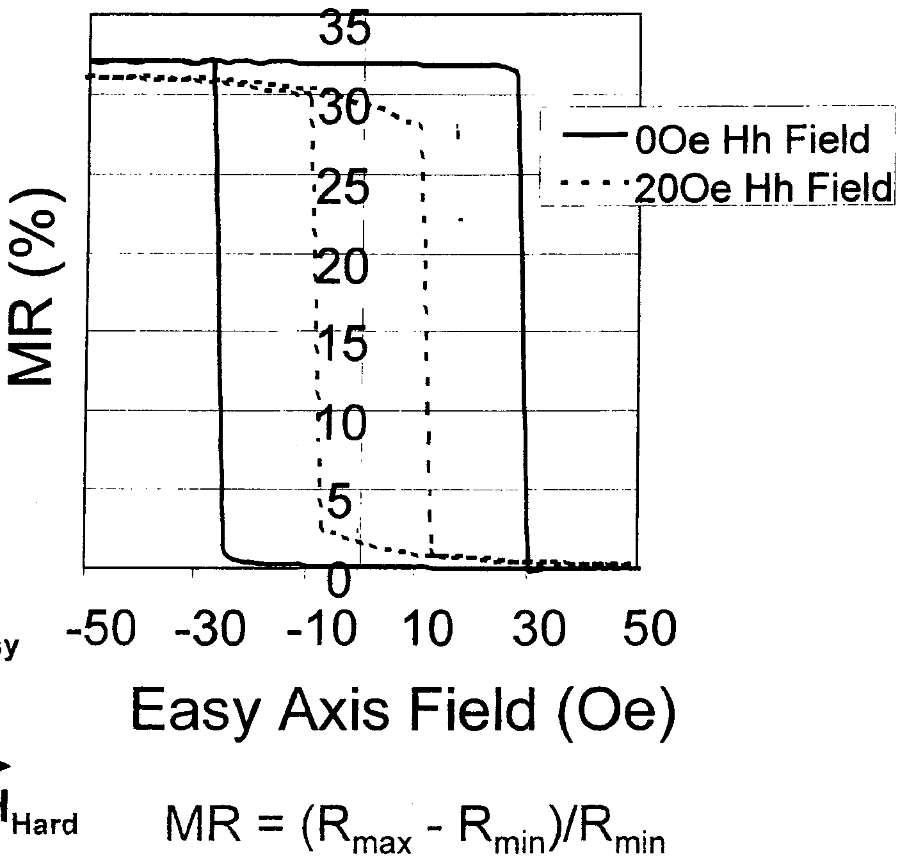
MOTOROLA LABS

Physical Sciences Research Labs

MTJ Hysteresis Loop

Program Mode





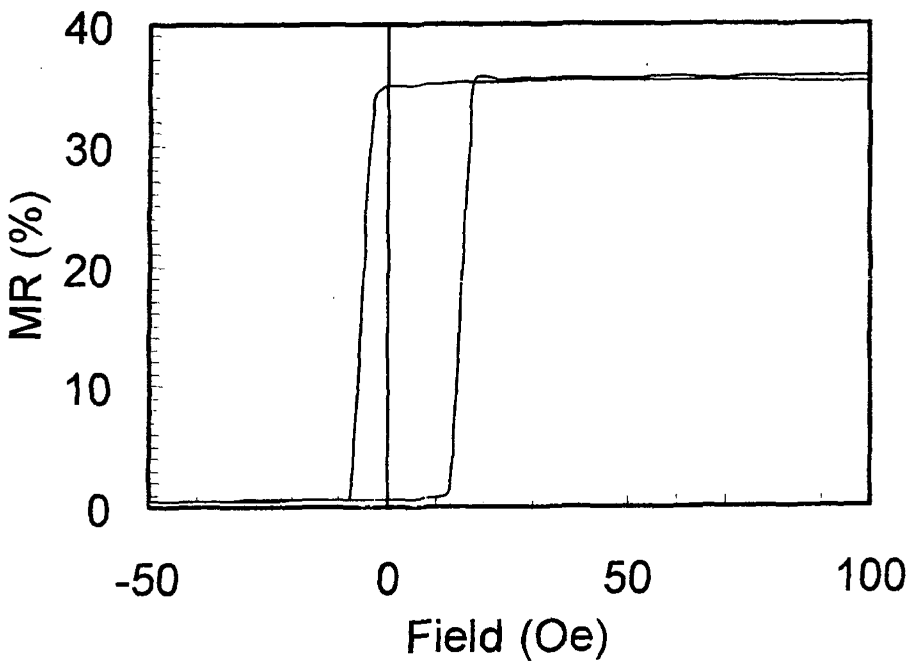
$MR = (R_{max} - R_{min})/R_{min}$

MOTOROLA LABS
Physical Sciences Research Labs

MTJ characteristics

Transmission Electron Micrograph

Magnetoresistance Curve

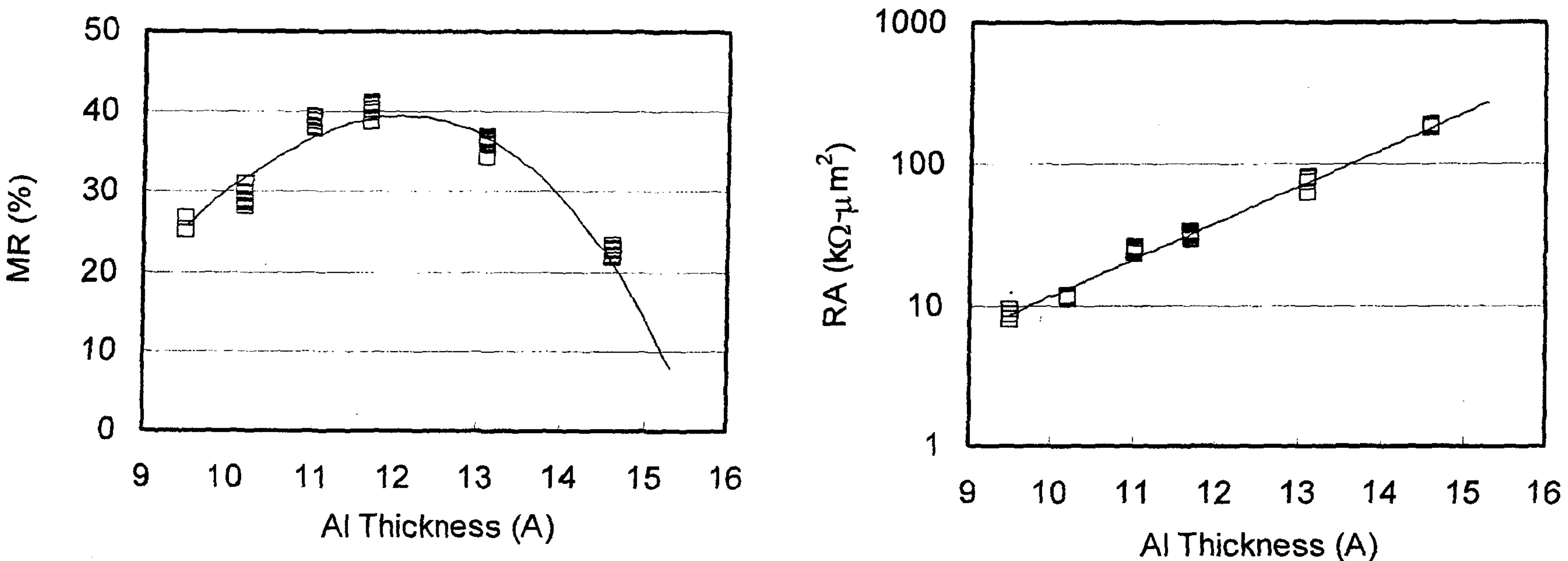


MOTOROLA LABS

Physical Sciences Research Labs

Aluminum Thickness

NiFe/AlOx/NiFe



Maximum MR=40% with d_Al=11–12 Å

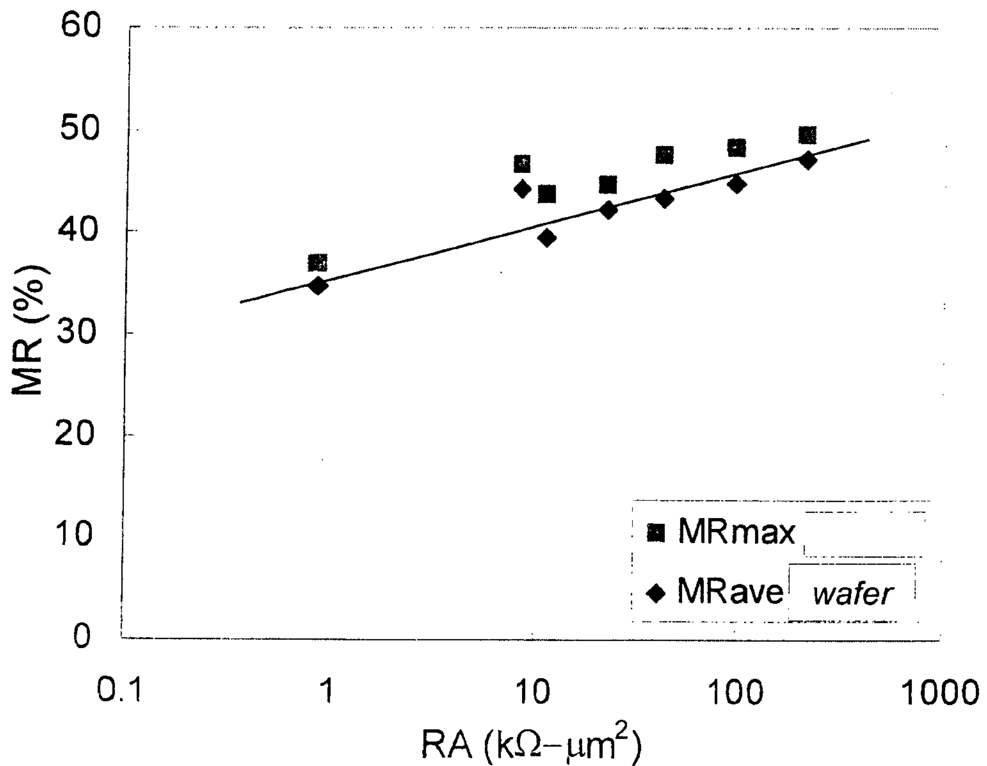
MR>20% for RA=10–100 kΩ-μm²

MOTOROLA LABS

Physical Sciences Research Labs

MR vs. Resistance

CoFe/ AlOx/ NiFe Tunnel Junction

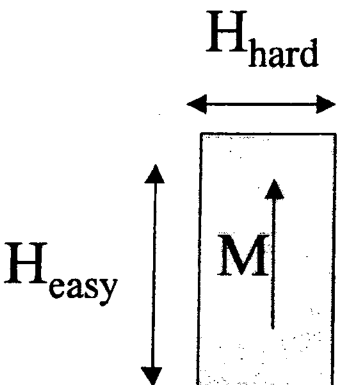


MR average within die

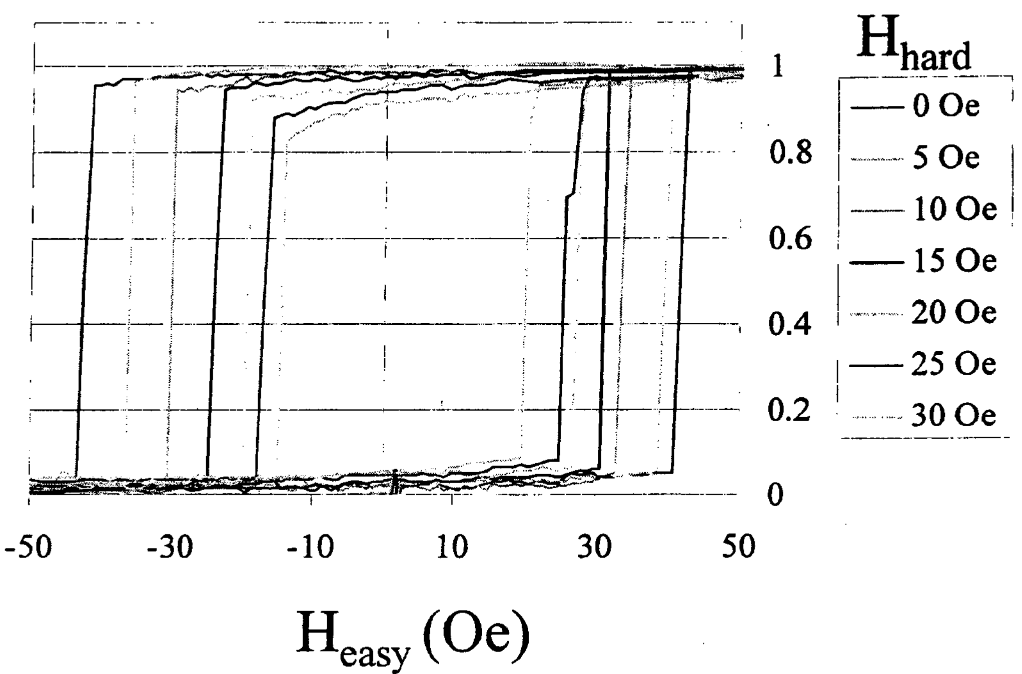
				46.1		
			47.8		47.4	
			43.3	46.0		
48.2		46.7	48.1	45.7	47.9	45.4
44.9	47.5		46.3	48.2	47.7	
	45.2	48.3	44.3	46.9	46.9	
		44.6	35.5	41.8		

Wafer average = 47.2%

MRAM write operation



Quasistatic hysteresis loops



- Shape anisotropy creates energy barrier to reversal

$$E_b \propto N_{eff} M^2$$

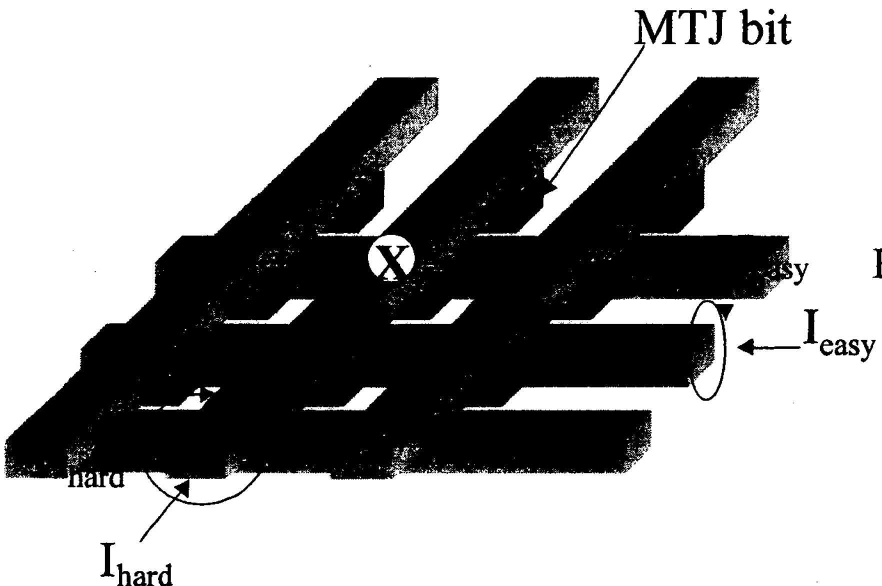
- Hard axis field decreases H_c

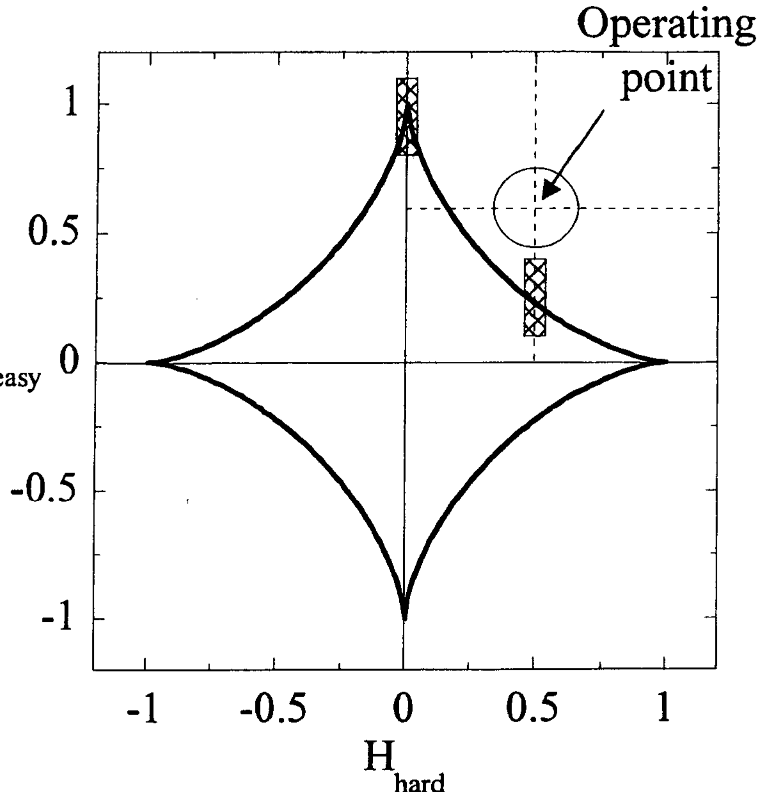
MOTOROLA LABS

Physical Sciences Research Labs

MRAM write operation

Cross-point architecture





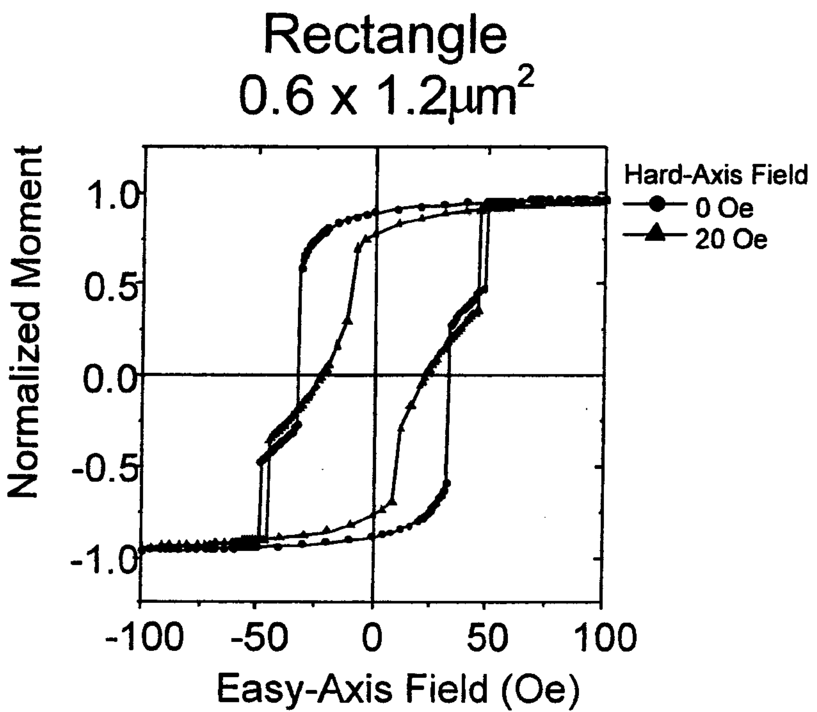
•Need good hard axis response and narrow switching distributions for write selectivity.

MOTOROLA LABS

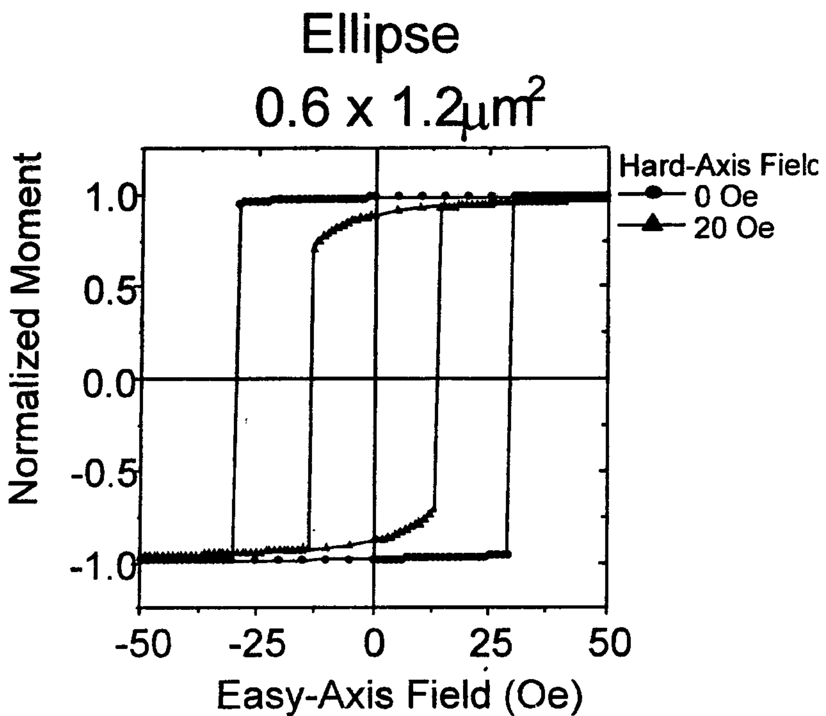
Physical Sciences Research Labs

Micromagnetic Simulation

Rectangle
$0.6 \times 1.2 \mu m^2$



Ellipse
$0.6 \times 1.2 \mu m^2$



MOTOROLA LABS

Physical Sciences Research Labs

Micromagnetic Simulation - Switching Transition

a)

b)

c)

d)

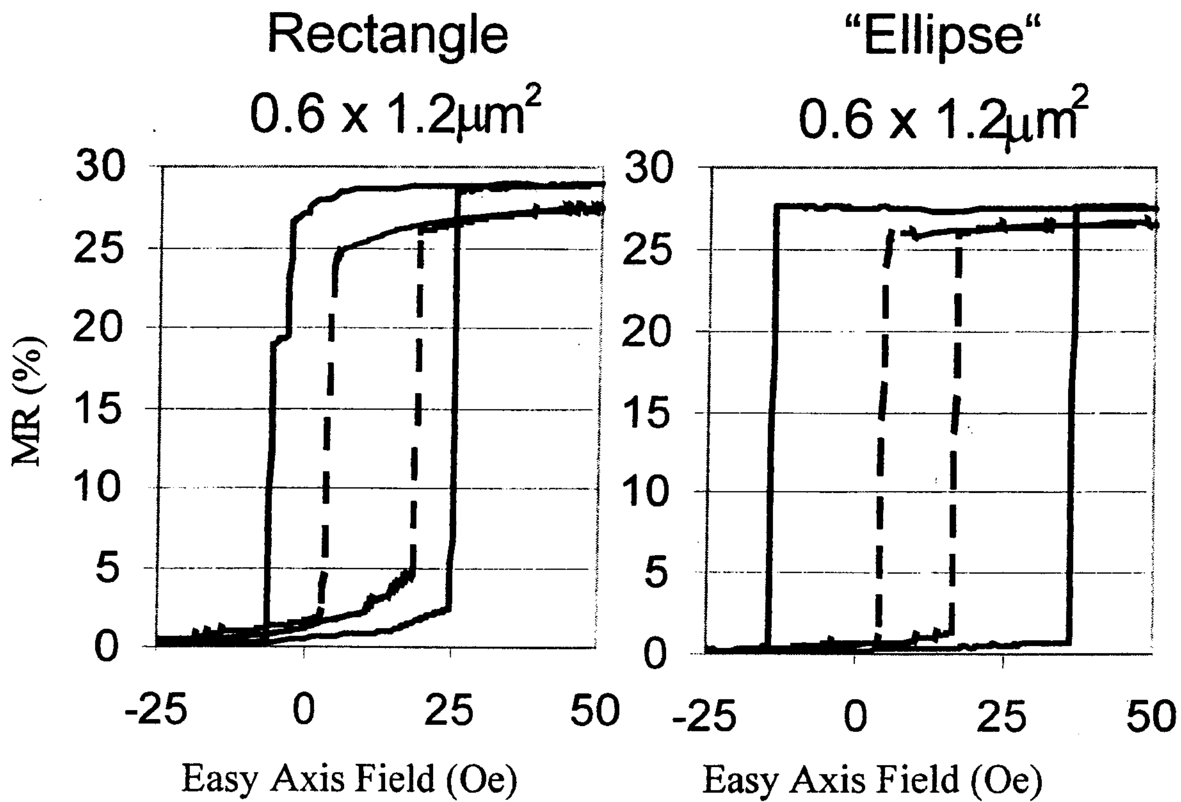
e)

f)

MOTOROLA LABS

Physical Sciences Research Labs

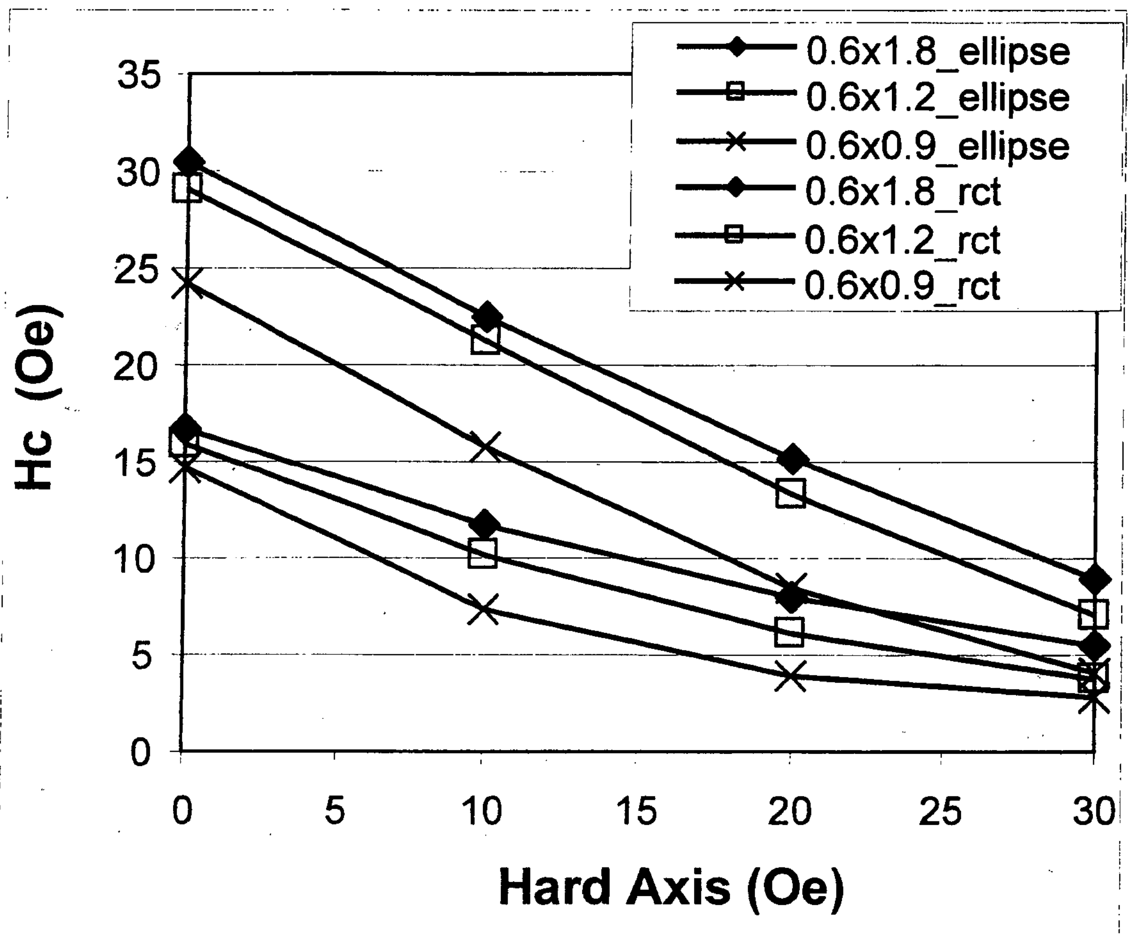
Experimental Electrical data



MOTOROLA LABS

Physical Sciences Research Labs

Switching characteristics of the bits



MOTOROLA LABS

Physical Sciences Research Labs

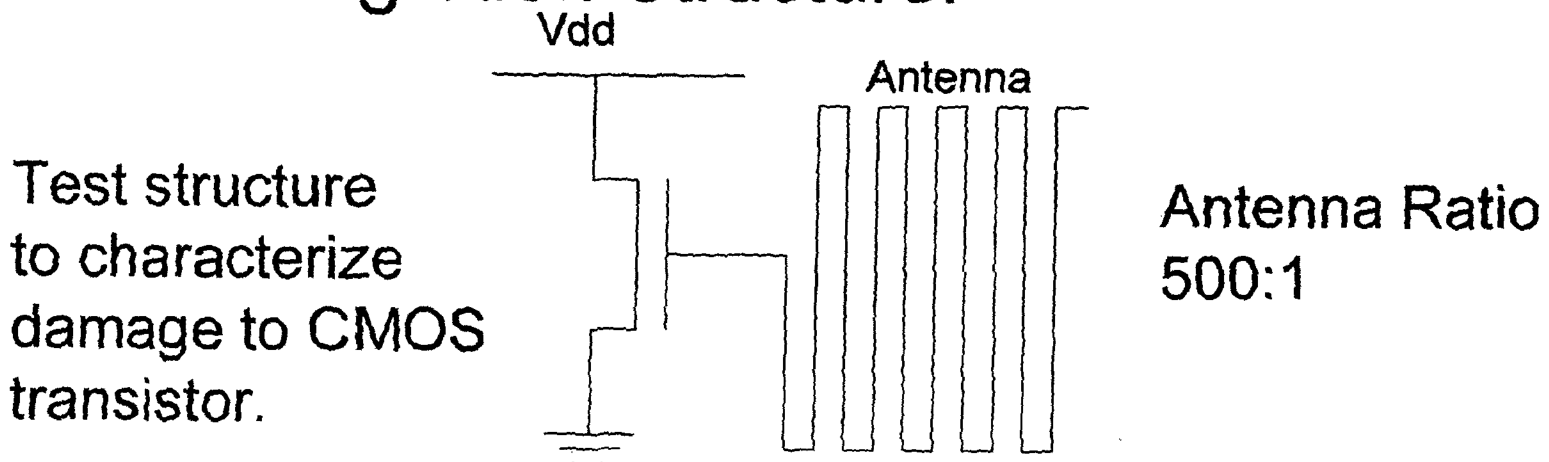
CMOS/MTJ Integration

Challenges to Integration:

- Threshold voltage shift to CMOS transistors
- Surface roughness under MTJ bit
- Switching characteristics

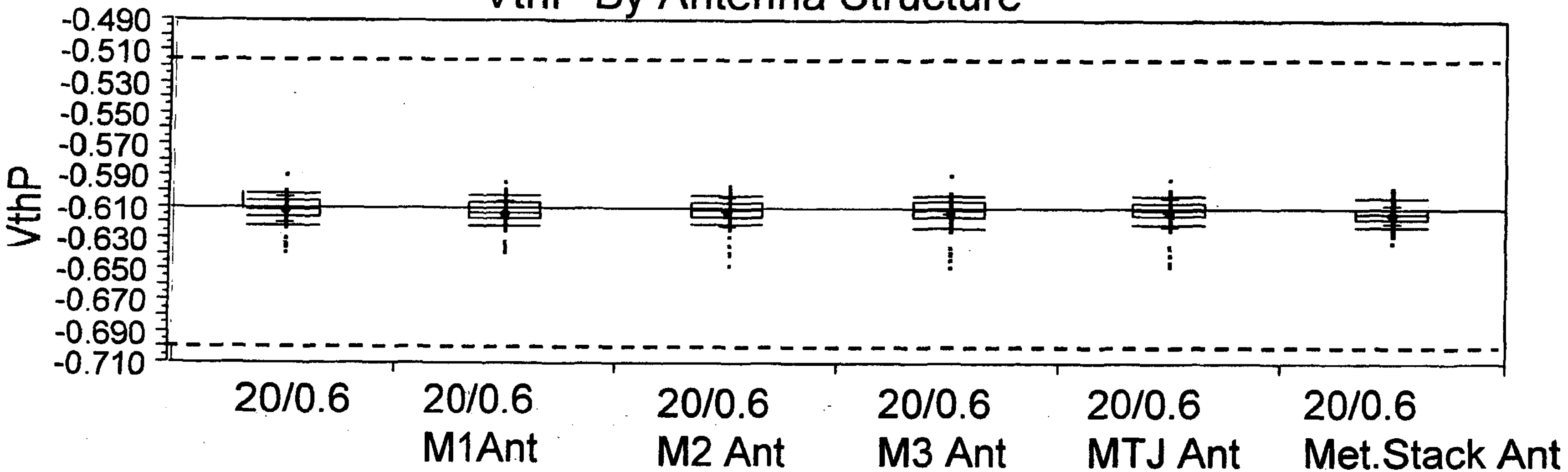
CMOS Integration Structure:

Test structure to characterize damage to CMOS transistor.



Antenna Ratio 500:1

Vt's Post Integration



Means and Std Deviations

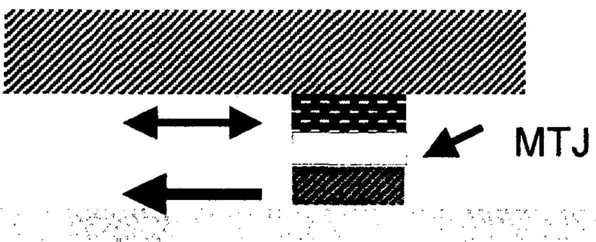
Structure	Mean	Std Dev
20/0.6	-0.60922	0.008856
20/0.6 M1Ant	-0.61095	0.008697
20/0.6 M2 Ant	-0.61011	0.009376
20/0.6 M3 Ant	-0.61047	0.010557
20/0.6 MTJ Ant	-0.61001	0.009450
20/0.6 MStack Ant	-0.61102	0.006926

MOTOROLA LABS

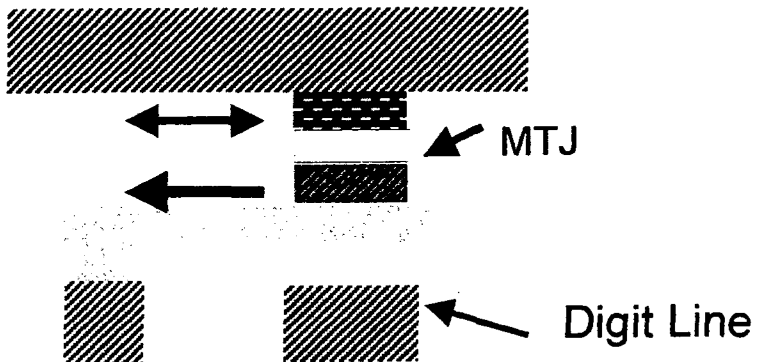
Physical Sciences Research Labs

Roughness induced by Digit Line

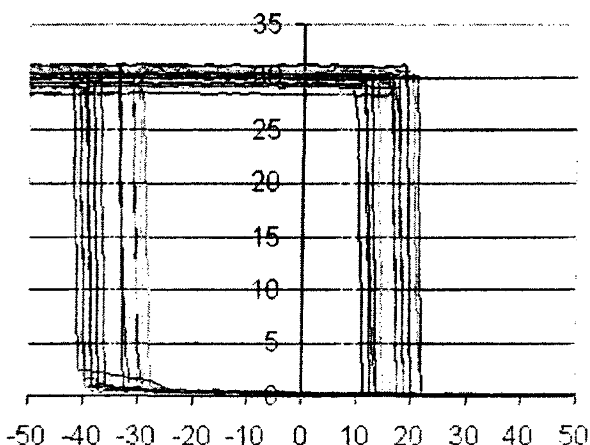
Bits without Digit Line

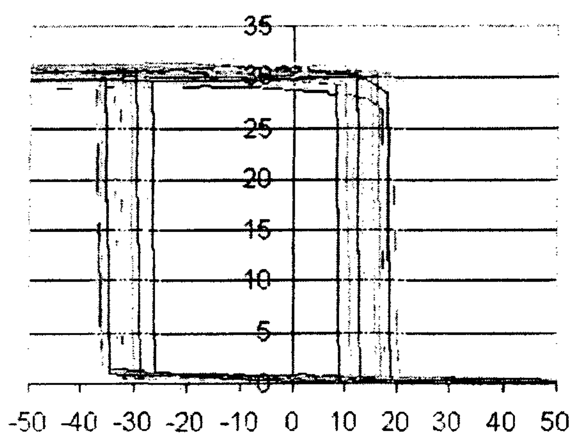


Bits with Digit Line



After Optimization (0.6x1.2μm bits shown)



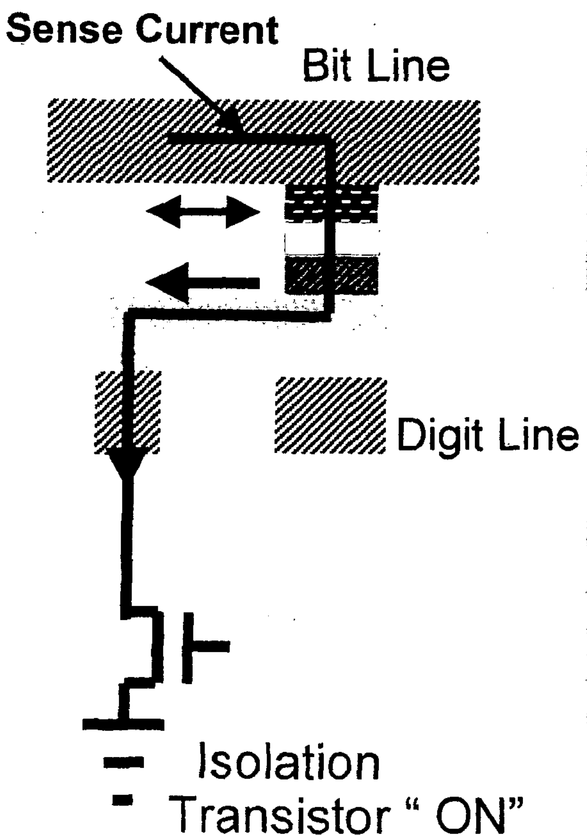


MOTOROLA LABS

Physical Sciences Research Labs

CMOS Integration - 1T/1MTJ Cell

0.6x1.2 μm bits @ 200mV bias with access Transistor



Wafer Map of R-A (kΩ-μm²)

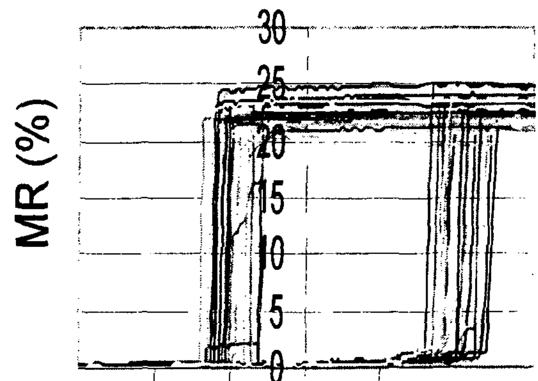
	13	12	12	12	
11	11	9.3	8.4	8.9	11
13	9.7	8.4	7.6	8	9.2
15		6.8	6	7.1	8.9
14	11	8.3	7.6	8	8.7
15	12	11	9.3	9.5	
	18	13	12		

Wafer Map of MR (%)

	23	23	24	22	
22	23	22	22	22	22
23	22	22	21	20	21
21		19	18	21	20
25	23	22	21	22	21
23	24	23	22	22	
	25	22	23		

150 mm wafer

no digit line current

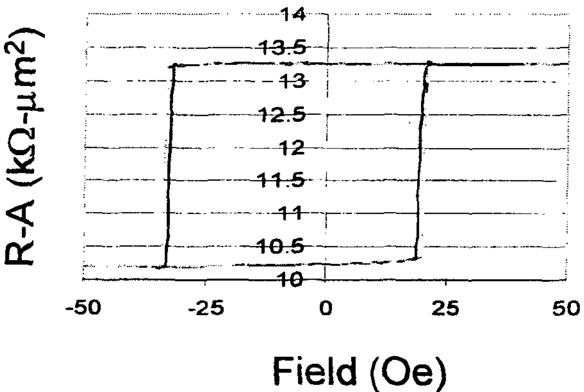


MOTOROLA LABS

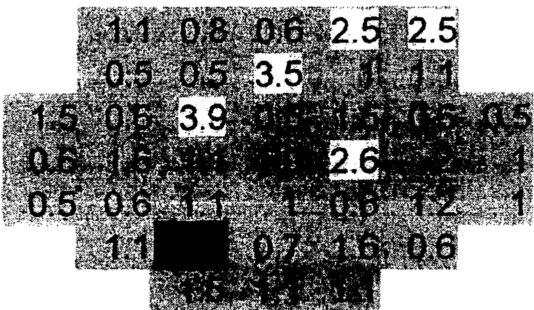
Physical Sciences Research Labs

Uniformity vs. Repeatability

Single 0.6x1.5μm^2 bit from array, repeated 15 times

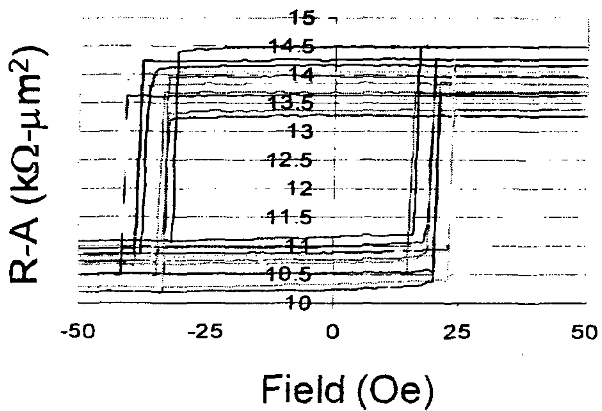


Map of spread in coercivity (Oe)

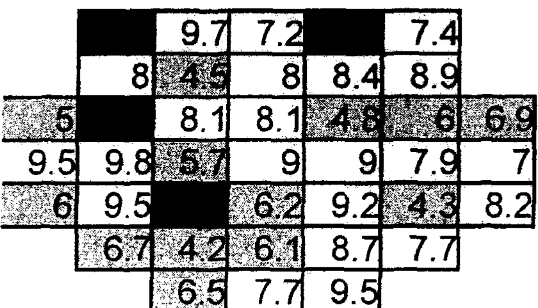


Average 1.2 Oe ± 0.6 Oe

15 - 0.6x1.5μm^2 bits in 1mm x 1.2mm array



Map of spread in coercivity (Oe)



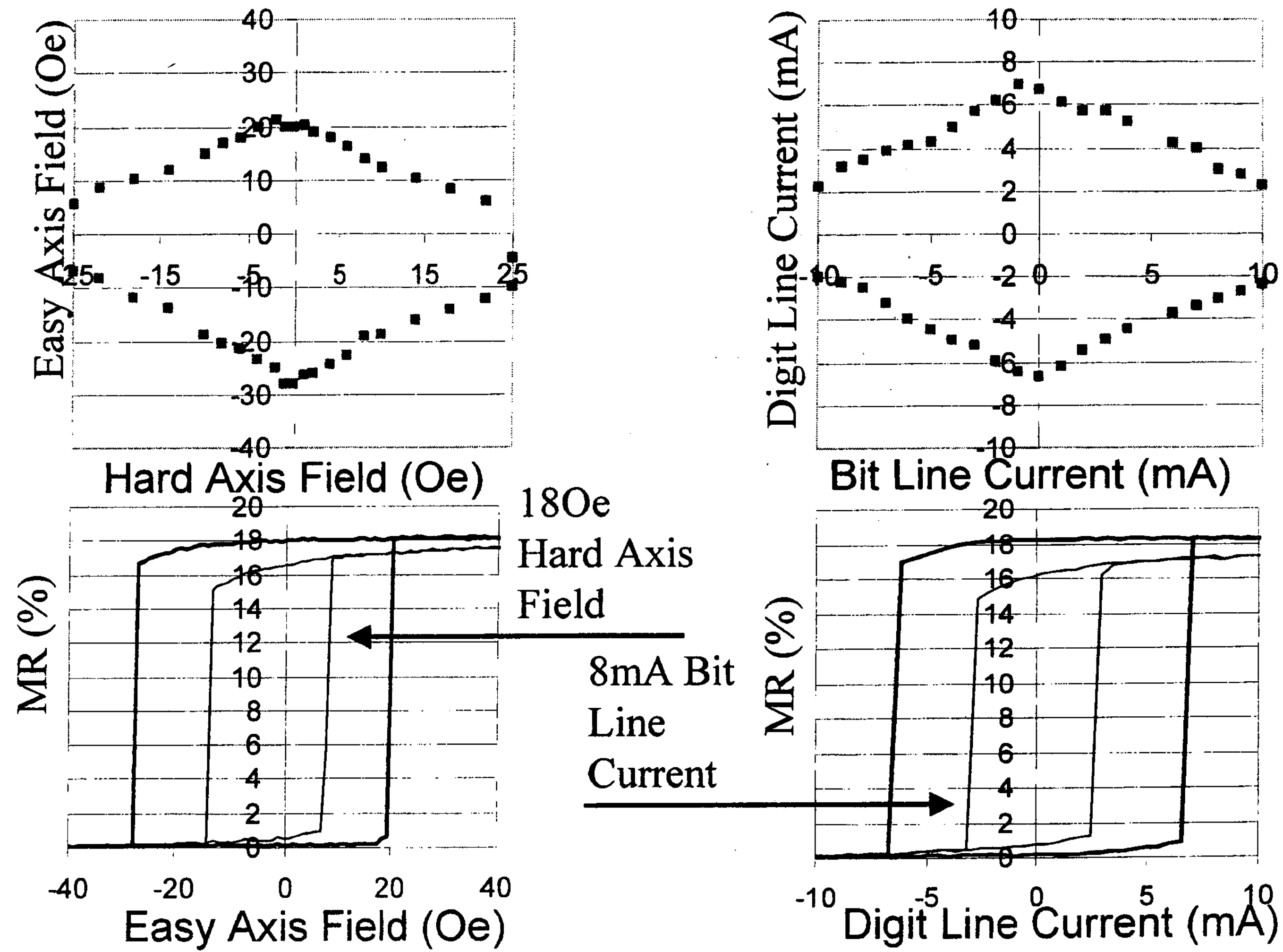
Average 7.5 Oe ± 1.7 Oe

MOTOROLA LABS

Physical Sciences Research Labs

External Field vs. Current Switching

Comparison of switching a 0.6x2.1μm^2 bit with external field versus lines near bit.



MOTOROLA LABS

Physical Sciences Research Labs

MRAM Memory

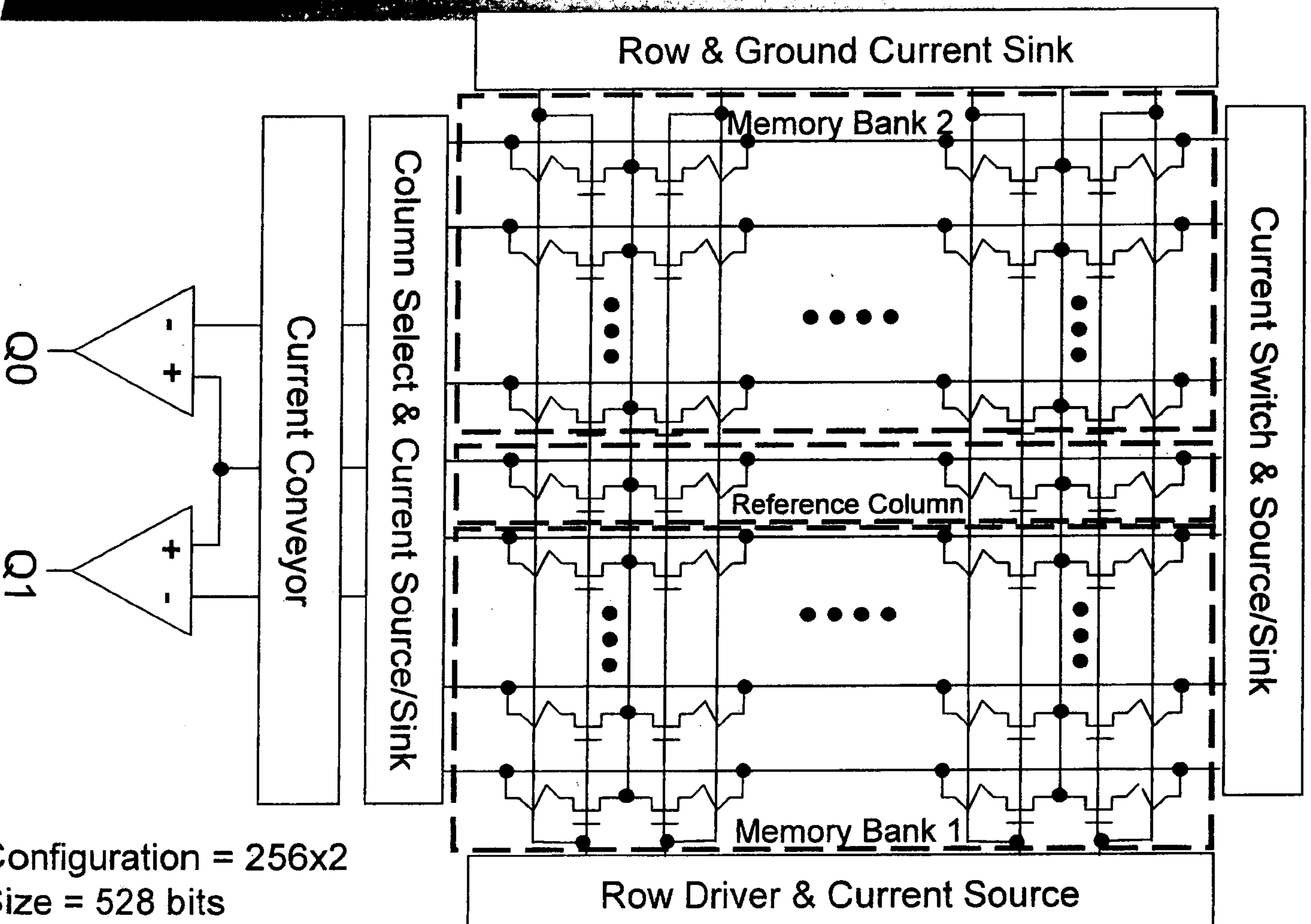
256 x 2 MRAM

- Non-volatile Random Access Memory
- 1 MTJ / 1 Transistor Cell
- $7.1 \mu m^2$ cell area in $0.6 \mu m$ CMOS process
- 16 rows, 32 columns, and 1 reference column
- Current mode read operation
- Reference column allows excellent tracking between target and reference bitline signals and provides a adequate level of Common Mode Rejection (CMR)

MOTOROLA LABS

Physical Sciences Research Labs

512 Array Schematic



Configuration = 256x2
Size = 528 bits

MOTOROLA LABS
Physical Sciences Research Labs

Array Parameters

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	16	16	17	17	16	16	16	17	16	16	17	16	[illegible]	16	17	16
2	16	16	16	16	16	[illegible]	16	16	16	16	16	16	16	17	16	16
3	16	16	16	[illegible]	16	16	[illegible]	17	16	17	17	16	16	16	16	16
4	17	16	[illegible]	16	16	16	16	16	16	17	[illegible]	16	[illegible]	16	16	16
5	[illegible]	16	16	[illegible]	16	16	16	17	16	16	16	16	[illegible]	16	16	16
6	17	16	[illegible]	[illegible]	[illegible]	17	16	16	16	16	16	17	16	16	16	16
7	16	16	16	16	16	16	16	16	16	16	17	16	17	16	17	17
8	[illegible]	[illegible]	16	[illegible]	16	[illegible]	16	16	16	17	16	[illegible]	[illegible]	16	17	17
9	[illegible]	16	16	[illegible]	[illegible]	16	17	16	[illegible]	16	[illegible]	16	16	17	16	16
10	16	16	[illegible]	16	16	16	16	16	16	16	[illegible]	[illegible]	16	[illegible]	16	16
11	16	16	16	[illegible]	16	[illegible]	[illegible]	16	[illegible]	16	16	[illegible]	[illegible]	[illegible]	16	16
12	17	16	17	16	17	17	16	[illegible]	16	16	16	17	16	16	17	16
13	17	16	16	16	16	[illegible]	16	[illegible]	16	16	16	16	16	17	16	16
14	17	16	17	16	16	16	16	16	16	16	16	16	17	16	[illegible]	16
15	16	16	16	16	16	16	[illegible]	16	16	16	16	16	16	[illegible]	16	16
16	16	17	16	16	16	[illegible]	16	16	[illegible]	16	16	17	16	16	16	16

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	19	18	19	19	19	18	18	19	19	19	19	18	19	18	19	18
2	19	18	18	19	18	19	18	18	18	18	18	18	18	19	18	18
3	19	19	18	18	18	18	18	19	18	19	19	19	18	18	18	19
4	20	18	18	18	18	18	19	18	18	19	18	18	18	18	18	18
5	19	18	18	19	18	19	19	19	19	19	18	18	18	18	18	18
6	19	18	18	19	19	19	19	18	19	18	18	19	18	19	19	19
7	18	19	18	18	18	18	18	18	19	18	19	19	19	18	19	19
8	19	18	19	19	18	19	19	19	18	19	18	18	19	18	19	19
9	19	18	18	19	19	18	19	18	19	19	19	18	18	19	18	19
10	18	18	19	19	19	19	18	18	18	18	19	19	18	18	18	18
11	18	18	18	19	18	18	18	18	18	18	18	19	19	18	19	18
12	19	18	19	18	19	19	18	18	18	19	18	19	18	18	19	19
13	19	18	18	18	19	19	18	18	18	19	19	18	18	19	18	18
14	19	18	19	18	19	18	18	19	19	18	18	18	19	18	18	18
15	19	18	18	19	18	18	19	19	19	19	18	18	18	18	18	18
16	19	19	19	18	18	19	18	18	18	18	18	19	18	19	18	19

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
2	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
3	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
4	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
5	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
6	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
7	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
8	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
9	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
10	12	12	12	11	12	12	12	12	12	12	12	12	12	12	12	12
11	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
13	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
14	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
15	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
16	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12

Resistance Distributions for 512 bits

Frequency

140
120
100
80
60
40
20
0

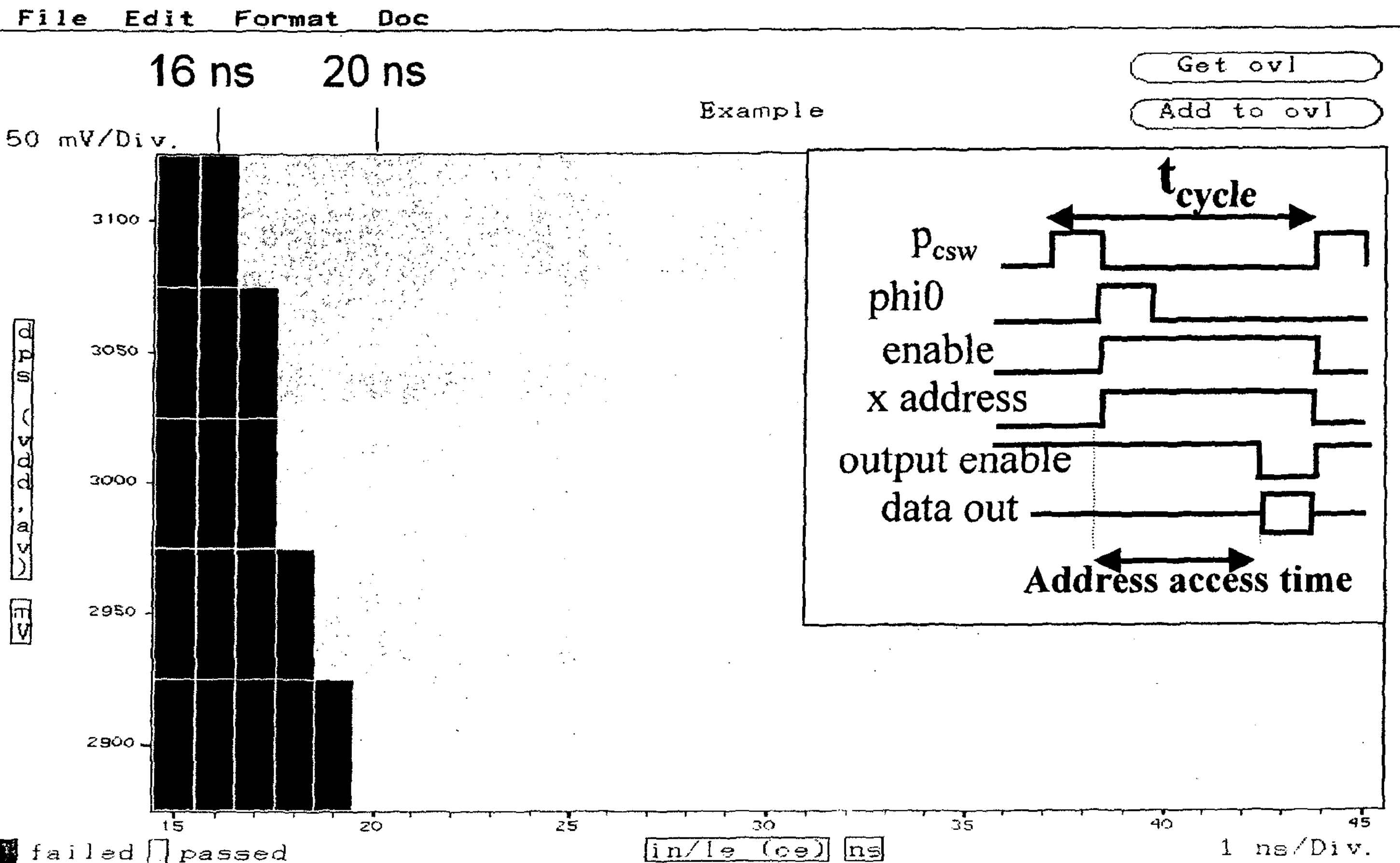
14 15 16 17 18 19 20 21

R (kΩ-μm^2)

Rmin
Rmax

MOTOROLA LABS
Advanced Services Research Labs

Shmoo Plot of t_{access} vs. VDD



MOTOROLA LABS

Physical Sciences Research Labs

Summary

- Demonstrated uniform MR and resistance across 6 inch wafer
- Demonstrated successful integration of MTJ and CMOS
- Measured address access time of 8ns and read cycle time of 18ns for 256x2 arrays at 3.0V using a single transistor and MTJ for a cell

MOTOROLA LABS

Physical Sciences Research Labs