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Critical Cleaning Requirements for Flip Chip Packages

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Abstract:
In traditional electronic packages the die and the substrate are interconnected with fine wire. Wire bonding technology is limited to bond pads around the peripheral of the die. As the demand for I/O increases, there will be limitations with wire bonding technology.

Flip chip technology eliminates the need for wire bonding by redistributing the bond pads over the entire surface of the die. Instead of wires, the die is attached to the substrate utilizing a direct solder connection. Although several steps and processes are eliminated when utilizing flip chip technology, there are several new problems that must be overcome. The main issue is the mismatch in the coefficient of thermal expansion (CTE) of the silicon die and the substrate. This mismatch will cause premature solder joint failure. This issue can be compensated for by the use of an underfill material between the die and the substrate. Underfill helps to extend the working life of the device by providing environmental protection and structural integrity.

Flux residues may interfere with the flow of underfill encapsulants causing gross solder voids and premature failure of the solder connection. Furthermore, flux residues may chemically react with the underfill polymer causing a change in its mechanical and thermal properties.

As flip chip packages decrease in size, cleaning becomes more challenging. While package size continues to decrease, the total number of I/O continue to increase. As the I/O increases, the array density of the package increases and as the array density increases, the pitch decreases. If the pitch is decreasing, the standoff is also decreasing.

This paper will present the keys to successful flip chip cleaning processes. Process parameters such as time, temperature, solvency, and impingement energy required for successful cleaning will be addressed. Flip chip packages will be cleaned and subjected to JEDEC level 3 testing, followed by accelerated stress testing. The devices will then be analyzed using acoustic microscopy and the results and conclusions reported.

Flip Chip Technology:
Flip chip technology eliminates the need for wire bonding by redistributing the bond pads over the entire surface of the die and directly attaching to the substrate. Instead of wires, the die is attached to the substrate utilizing a direct solder connection. In comparison with the traditional wire bonded device, there are several things that differentiate a flip chip device. First, it is possible for the bond pads to be distributed in an array that covers the entire surface of the die instead of a set of peripheral bond pads. Likewise, the corresponding bond pads are redistributed on the substrate. Second, in order for the connection to be made, solder balls are attached to the die bond pads utilizing one of the wafer bumping techniques (i.e. evaporative, electroplated, etc.). These solder balls take the place of the wire. The bumped die is then "flipped" and reflowed to the substrate. It is important to note that when a flip chip die is placed prior to reflow, it is essential that the solder balls line up to the corresponding pad on the substrate. Upon reflow, if the pads and balls are not lined up exactly, the wetting action of the solder will compensate for the misalignment and the die will align. In the flip chip process, the electrical, mechanical and thermal interconnections are all made simultaneously. This eliminates the need for wire bonding, die attach and encapsulation. Finally, there is a definitive cost advantage for high I/O devices using flip chip technology.

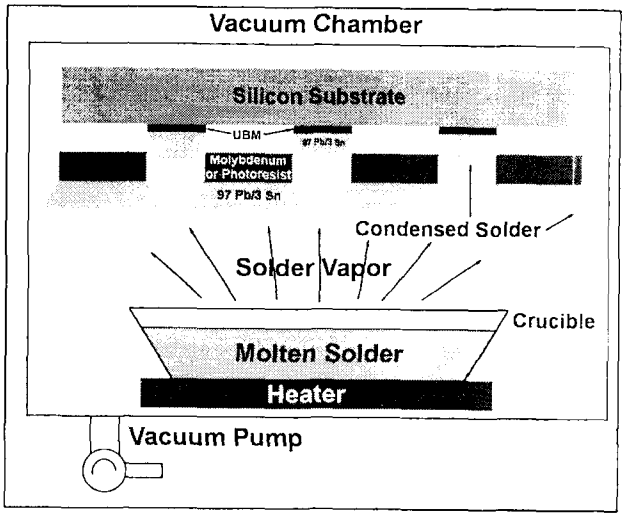


Figure 1: Evaporative Wafer Bumping Technique

Although several steps and processes are eliminated when utilizing flip chip technology, there are several problems that must be overcome. The main issue is the mismatch in the coefficient of thermal expansion (CTE) of the silicon die and the substrate. This mismatch will cause premature solder joint failure resulting in premature failure of the entire package. Adhesion characteristics of the underfill material are formulated to help compensate for the mismatch in the CTE.

In addition to removing the need for wire connections, flip chip technology also has many other benefits. In the flip chip process, the electrical, mechanical and thermal interconnections are all made simultaneously. The limitations of only allowing peripheral bond pads are eliminated in addition to the device size being dramatically reduced. The ability to use the entire die surface allows for higher I/O counts. This fact increases the number of I/O in a package while not effecting the overall size of the package, and in some cases, actually reduces the package size.

Reliability:
Reliability is a key consideration in the selection of a soldered flip chip interconnection system. Both mechanical fatigue and corrosion of the solder joint can significantly affect the performance of a solder-based interconnect system. The solder composition, the substrate, underfill materials, and the severity of the environmental exposure influence the relative kinetics of damage.

While in service temperature fluctuations result in differential thermal expansion between the various components of a flip chip assembly. The expansion mismatch between these components imposes strains, which produce mechanical stresses at the solder joint and at the die surface. These stresses are the driving force for failure mechanisms such as crack growth and interfacial delamination. The assembly stiffness and the inelastic deformation properties of the solder joint determine the magnitude of the stresses. Additional stress caused by temperature and environment influence the rate of degradation.

Underfill is used primarily to improve the reliability of flip chip interconnect systems. Underfill materials fill the gap between the chip and substrate around the solder joints, absorbing the mechanical stresses imposed on the solder joint. High adhesion of the underfill material to the substrate and die is necessary to improve the reliability of the interconnect system. Organic flux residues deposited onto the surfaces of flip chip assemblies during reflow soldering operations have been shown to affect the adhesive properties of underfill materials. Moreover, results of thermal cycle tests and humidity storage show that the reliability of flip chip packages is dramatically reduced by flux/underfill incompatibility. The cure time and temperature of the underfill are significant factors in the selection of an underfill material. Since the underfill process follows the chip-bonding step, cure temperatures lower than the melting point of the solder joint are desirable. From the manufacturing through put standpoint, short cure cycles are generally preferred. The expansion coefficient of the underfill material must match that of the die and substrate as closely as possible. Likewise, good adhesion of the underfill material to the substrate and die improves the reliability of the interconnect system.

Figure 2: Progression of Underfill

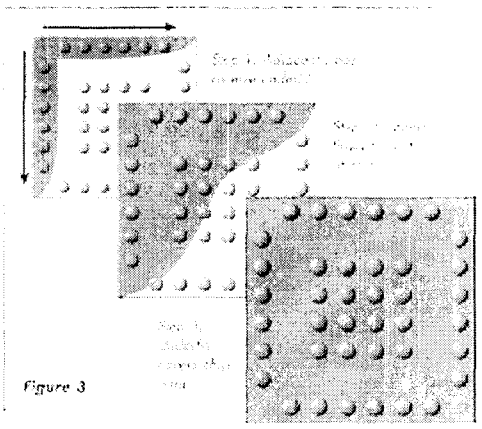


Figure 3

Why Clean?
Flux selection will drive the quality of the solder interconnect as well as the degree of residue left behind. Low solids fluxes leave a small amount of residue but may not always provide the wetting characteristics required for high reliability. Area array devices with high I/O require a high degree of activity from the flux to assure high yields and no cold solder joints. To obtain good activity, the solids content required is typically greater than most low-solids no-clean flux formulations. As a result, flux residues are left behind and must be cleaned.

Solvent cleaning has for years been successfully used in electronics manufacturing as a means of assuring improved product reliability. If the flux residues are not removed there is a potential for degradation of the underfill, including inconsistent flow patterns, the generation of voids during cure, and poor interfacial bond strengths. The proper solvent will eliminate these residues.

Flip Chip Cleaning Issues:

Flip chips pose some of the greatest cleaning challenges. Some of the contributing factors to the challenges are the essence of why flip chips are important to IC packaging. They are better performing and more cost-effective devices. While the package size continues to decrease, the total number of I/O continue to increase. As the I/O increases, the array density of the package increases and as the array density increases, the pitch decreases. If the pitch is decreasing, the standoff is also decreasing. This means that the package is getting smaller, the number of obstacles is increasing and the distance between the substrate and the die is decreasing. The overall miniaturization of the package coupled with the fact that, in some cases, there is more than one die per package and the variation in the raw materials, it is not difficult to understand why there would be challenges with cleaning flip chips.

High I/O devices tend to translate into high array density packages and high array density devices tend to result in a tight pitch. Pitch is the distance from the center of one solder ball to the center of the nearest adjacent solder ball. Industry is predicting that in the next several years, high-density flip chips will be capable of pitches near 50-75 microns and I/O counts exceeding 5000. Together, pitch and array densities are vital aspects to the success of cleaning a flip chip. If a particular flip chip has a very high array density and a tight pitch, not only are there many obstacles in a very small area, but these "trees" obstruct the cleaning medium. The flow of the solvent may become even more impeded from flux residue bridging between one or several solder joints.

On a flip chip device, the pitch also dictates the standoff or the distance between the die and the substrate. As the pitch decreases, so does the standoff. This lower standoff adds to the cleaning challenge in that it makes it more difficult to get cleaning and rinsing medium in and out from under the die. Cleaning will be inadequate if the solvent is unable to penetrate under the die to wet and solvate contaminants. In addition, further problems arise if the cleaning medium is not rinsed completely.

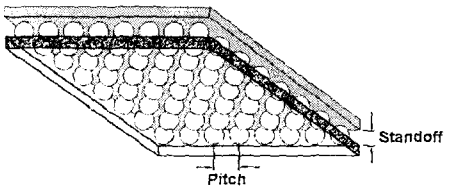


Figure 3:Example of Pitch and Standoff

Raw material variation also becomes a factor in cleaning due to the fact that flip chip is quite immature in relation to other technologies. While flip chip technology was first introduced over 30 years ago, the technology was not ready for high volume manufacturing at that time. Now that there are new innovations in the raw materials used to manufacture flip chips there are rapid shifts in the industry standards. This inconsistency in raw materials can cause possible compatibility issues with the cleaning or rinsing medium. These incompatibilities can be overcome but it is important to realize that these incompatibilities may be present.

One of the current trends in flip chip packaging is the desire for more than one die per substrate (MCMs). This aids in the reduction of cost and boosts performance. In some cases, this does not impact the cleaning effectiveness. The effectiveness is only compromised when the flip chip dies are spaced tightly together. The closer the die move together, the more difficult for the cleaning medium to flow in and out from under one die and immediately flow under another die. This assumes that the previous die does not have large amounts of residue preventing the flow from even reaching subsequent die. The previously mentioned obstacles are only compounded by the addition of multiple die on the same substrate.

Another issue that plagues successful cleaning is the package configuration. That is, in an effort to keep package costs to a minimum, many manufacturers are attempting to use less expensive raw materials. An example of this is the use of organic versus ceramic substrates. Ceramic substrates tend to offer a very rigid backbone to a package. When underfill is applied and cured, the underfill adheres to both the substrate and the die very well assuming there are no flux/underfill incompatibilities that cause poor interfacial adhesion. When using a ceramic substrate, the CTE of the silicon and the ceramic are more closely matched than silicon and organic substrates. Thus, the loss in planarity is much less in a package utilizing ceramic as the substrate. The planarity of any package is essential to it reliability. If a package loses planarity, it can cause premature failure, even die cracking. As mentioned before, efforts to keep costs to a minimum also contribute to the cleaning challenge. Since organic boards are usually lower cost than ceramic, organic boards are desirable. Organic boards have a tendency to warp or lose planarity. In an effort to help compensate for the larger CTE mismatch between the organic board and the silicon, stiffeners are often added to the organic boards. These stiffeners often create a cavity in which the die will sit. The space between the stiffener and the die is kept to a minimum. This cavity adds to the difficulty of not only getting cleaning medium in under the die, but also the rinsing of the cleaning agent.

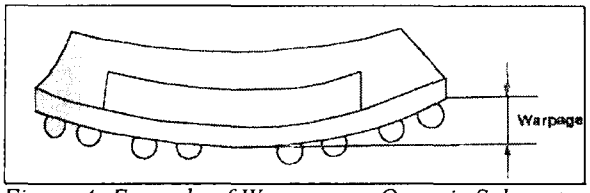


Figure 4: Example of Warpage on Organic Substrate

Keys to Successful Flip Chip Cleaning Processes:
It is to be expected that flip chip packages will continue to decrease in size, I/O counts will continue to rise, array density will increase, the pitch will decrease, the number of die on a substrate will go up and the variation of the raw materials will stabilize. All of these issues add to the ever-increasing challenge involved in cleaning flip chip devices. It is important to understand what will facilitate successful cleaning.

It was initially thought that surface tension and viscosity were vital physical properties to successful flip chip cleaning. While this is a true statement, further investigation would prove that there is a real dichotomy when looking at surface tension. A higher surface tension material aids in the flow of the material under the die. Even though a higher surface tension increases flow, it holds up the chemistry's ability to be easily removed from under the die. While a higher surface tension increases flow, it also decreases the ability for that material to be removed from under the die, so higher is better to a point. The finer details of surface tension still need further investigation. It is safe to say however, that viscosity data was more conclusive. That is, lower viscosity is better. The lower the viscosity the better the flow and the better the medium's ability to penetrate tight spaces. Low viscosity of a material is more important than high surface tension in that the material will flow and penetrate the device at a low viscosity but the converse is not necessarily true.

Viscosity and surface tension are both vital properties to the ability of the chemistry to clean a flip chip device; but once you get chemistry in to clean the contaminated surface, it is essential that the entire cleaning medium be removed. Incomplete rinsing can lead to off gassing which could be catastrophic to the reliability of the flip chip or any device. Therefore, it is essential that the cleaning medium be completely soluble in the rinse medium.

The importance of the four interdependent variables, chemical solvency, temperature, time and impingement energy was initially not clear. After some investigation, it became apparent that of the four variables, temperature is the most important. Generally speaking, as the temperature increases, the surface tension and viscosity both decrease. As stated above, the drop in viscosity is more significant than the decrease in surface tension is detrimental. This decrease in viscosity and increase in energy (thermal energy) by simply raising the temperature can make up for a lack of solvency and impingement energy given enough time, whereas the converse is not true. Time appears to be the next most important of the four variables. Time is required for the cleaning and rinse fluids to penetrate under the die. Close attention must be given to the time and temperature studies when moving from experimental to live processing. Chemical solvency is critical to the removal of flux residues. Even if a low solid, no-clean flux is used during the soldering reflow process, not all fluxes are created equal. Due to these variations in flux types some residues may be better removed in certain cleaning chemistry formulations than others.

Impingement energy is typically centered on an immersion centrifugal process. Attention must be given to rotation velocity and counter current time. The successful cleaning process will evolve from a clear understanding of how these variables interact.

Cleaning Flip Chip Devices:

Several aspects of flip chip flux cleaning have been shown to affect the performance of flip-chip underfill material. Among these are the following:

Cleaning solution chemistry: The cleaning chemistry selection must be a good solvating agent for the soil. Once the soil is solvated and rinsed, it is important that no cleaning chemistry be left under the die. The inability to properly rinse will likewise interact with the flow of underfill encapsulants, which may cause gross solder voids and premature failure of the solder connection.

Flux residue: Flux residues may interfere with the flow of underfill encapsulants causing gross solder voids and premature failure of the solder connection. Furthermore, flux residues may chemically react with the underfill polymer causing a change in its mechanical and thermal properties.

Cleaning solution application technique and process parameters: Flip chip die have a tight pitch, low standoff and dense array of solder bumps, which make post-reflow cleaning of flux residues increasing difficult. Four key cleaning variables (*cleaning solution chemistry, time, temperature and impingement energy*) must be understood to achieve a robust cleaning process.

Rinse solution chemistry: Rinse medium must be soluble with the cleaning solution. Moisture in the form of water or solvent left under the die may be an important factor affecting thermal fatigue failures.

Cleaning chemistry:
The cleaning chemistry must solvate the flux residue under the die. The cleaning chemistry choices used in this study are semi-aqueous blends. Semi-aqueous cleaning is the process of solvent washing followed by water rinsing. The standoff and pitch of the die are important factors to consider when making a cleaning chemistry selection. Solvent factors to consider are surface tension versus temperature, viscosity versus temperature and time to clean versus temperature. Judge the selection of the cleaning chemistry on these parameters. Adding impingement energy will enhance the overall process, but is not enough to be the driving factor when initially selecting the cleaning chemistry.

As the geometry of flip chip devices continues to shrink, it is important to understand the physical properties of the cleaning medium. As earlier stated it was initially assumed that surface tension and viscosity would be key elements to successful cleaning. The initial inquiry was designed to study the effect of temperature on both surface tension and viscosity. One might expect that the surface tension of the cleaning medium would decrease as temperature increased. Generally this is a correct statement, but in several instances, an increase in surface tension was noticed as temperature increased. Viscosity did drop as temperature was increased.

Surface Tension versus Temperature

Temp °F	Ionox FCR	Ionox HC2	Micronox MX2301
72°F	28.4	21.3	30.6
120°F	28.9	25.4	29.9
140°F	28.9	26.8	29.6
170°F	27.6	27.5	29.4

Viscosity versus Temperature

Temp °F	Ionox FCR	Ionox HC2	Micronox MX2301
72°F	7.02	9.06	5.66
100°F	4.98	5.75	3.98
120°F	3.94	4.60	3.28
140°F	2.74	3.31	2.74
170°F	2.11	2.33	1.98

After the surface tension and viscosity were tested, the challenge was to understand the effects that they would have on the cleaning chemistries in a confined space (under the die). The first step was to measure the flow of the cleaning chemistries utilizing the test vehicle shown Figure 5. A known amount of dye-doped chemistry was applied to the leading edge of the test vehicle. The time it took to travel a known distance was tested. This is similar to how underfill flow might be tested. This test was performed in a static condition. It really only tested the capillary flow of the cleaning chemistries but was also a test of surface tension. The chemistry with the highest surface tension traveled the distance the fastest.

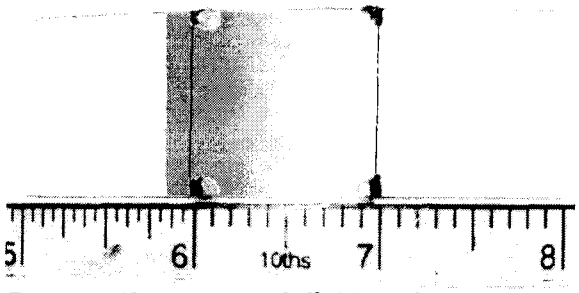


Figure 5: 42 micron standoff: 1"x1" die

Time To Flow Under a 1"x1" Glass Die Using Capillary Penetration:

- The test vehicle was heated to the desired temperature on a hot plate (±2°F).
- Chemistry was applied to one edge of the die.
- The time that it took for the doped chemistry to travel a pre-determined distance was recorded.
- This was repeated at several different temperatures.

The next step was to incorporate viscosity into the test. This was done by adding mechanical agitation to a bath of the cleaning chemistry and measuring the exchange rate of the chemistry under the die. A representation of this test is shown in Figure 6.

Time Required for Chemistry to Replace Existing Chemistry Under Glass Die:

- Chemistry was heated to the desired temperature (±2°F) with constant stirring.
- Chemistry was placed along one edge of the die and allowed to completely underfill the die.
- The entire test vehicle was then immersed in the beaker.
- The time that it took for the chemistry to completely replace the doped chemistry from under the die was measured and the value recorded.

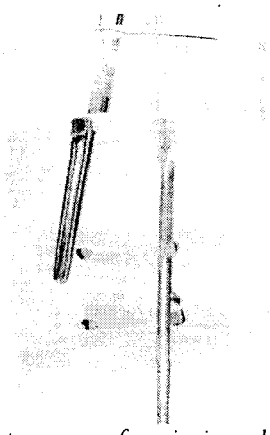


Figure 6: Test process for rinsing chemistry under die

The chemistries with the higher surface tension and lower viscosity exchanged the chemistry more quickly than those chemistries with lower surface tension and lower viscosity. Chemistries with lower viscosity tend to flow better than those with higher viscosity. The surface tensions of these materials seem less important to the flow than the viscosity.

To this point, it was concluded that viscosity was one of the key physical properties to successful cleaning. Further testing would reveal that viscosity is important and the surface tension is important to the rinsing stage of cleaning. The higher the surface tension of a liquid, the more energy required to displace the liquid from the surface of the part. Higher surface tension may enhance initial flow and wetting but will work against the process when rinsing. More important to the rinsing of the chemistry is the solubility of the chemistry in the rinse media. Solubility of the cleaning chemistries was measured using a similar test to that described above.

	Time (sec.) to travel under 2" glass die.			Time (mm:ss) to replace with fresh chemistry under 1" die.		
Chemistry	**72°F**	**140°F**	**170°F**	**72°F**	**140°F**	**170°F**
Ionox FCR	50	20	15	Nt	4:00	2:20
Ionox HC2	90	15	13	Nt	4:10	3:55
Micronox MX2301	17	9	5	Nt	4:00	4:00

* Nt = not tested

In order to reduce the amount of experimental variability, time, temperature and solvency parameters were kept consistent regardless of the configuration. There were two choices in regards to impingement energy, mimic the energy used in an existing centrifugal system or use low impingement energy. The latter was chosen due to the fact that solvency is solely based on the cleaning chemistry with time and temperature being interdependent variables. This meant that if the energy was held constant, the only variables for any given chemistry would be time and temperature. If the energy is low and constant, the other three variables will have to make up for the lack of energy. This will magnify the significance of time and temperature for each chemistry tested. The results of this test data are shown in Figure 7.

Flux Removal as a Function of Time and Temperature:

- Chemistry was heated to the desired temperature (±2°F).
- A test vehicle was completely underfilled with the desired flux and reflowed appropriately.
- The test vehicle was then immersed in the chemistry.
- The test vehicle remained in the chemistry for a pre-determined amount of time.
- The test vehicle was then rinsed utilizing an in-line rinse section.
- The percent flux removal was noted and the values recorded.
- This was repeated at different times and temperatures.

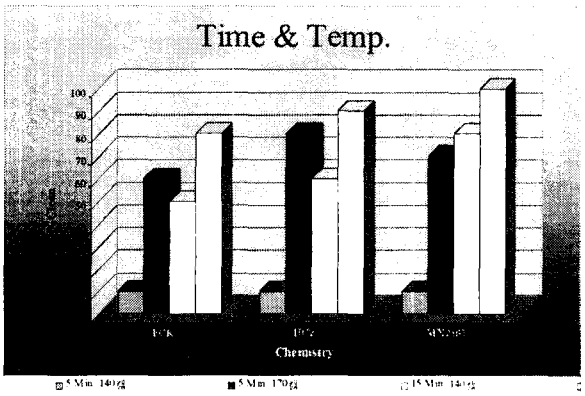


Figure 7: Cleaning effectiveness for FCR, HC2 & MX2301

Blue: Time = 5 minutes, Temperature =150°F
Red: Time = 15 minutes, Temperature = 150°F
Yellow: Time = 5 minutes, Temperature = 170°F
Light blue: Time = 15 minutes, Temperature = 170°F

Impingement Energy:

Cleaning solution application technique and process parameters:

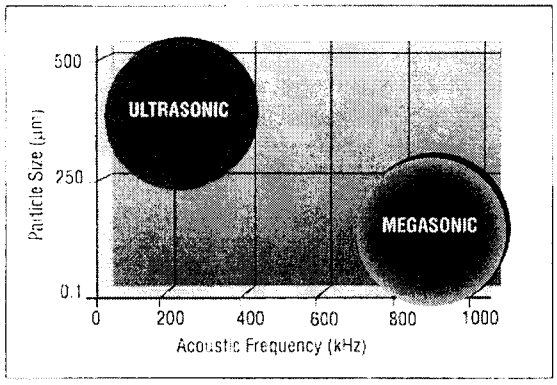
Impingement energy is a key driver toward successful cleaning. Flip chip solder interconnects must be compatible with the impingement energy used. These processes may support either batch or inline processing.

- **Batch Centrifugal:**

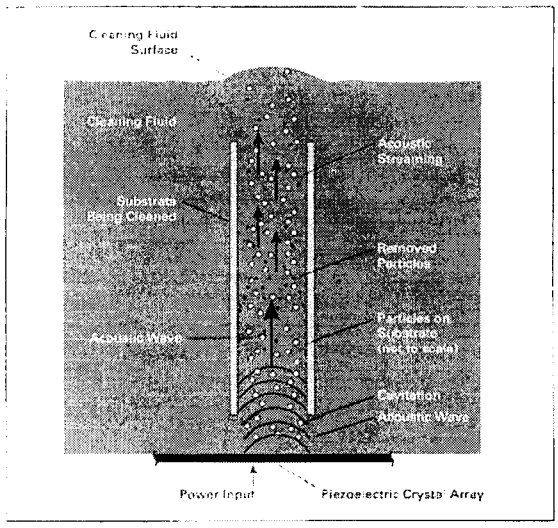
The flip chips rotate in one direction first, then reverse and rotate in the opposite direction. This rotation – reversal action continues for the duration of the wash interval. Following the wash interval, the cleaning solution returns to the reservoir and a rinse interval begins. With the cleaning chamber still sealed, de-ionized water is sprayed across the flip chip assemblies. The centrifugal action allows the rinse water to penetrate under the die. After the rinse interval, the flip chip assemblies continue to rotate while hot air is introduced to speed the drying process. The flow diagram of this process is shown in Figure 8.

♦ **Megasonics:**

Megasonic cleaning uses the piezoelectric effect to enable submicron particle removal from substrates. A ceramic piezoelectric crystal is excited by high frequency (between 700-1000kHz) AC voltage, causing it to vibrate. This vibration generates an acoustic wave. The wave is transmitted through a cleaning fluid, producing controlled-acoustic cavitation. Acoustic cavitation is produced by the pressure variations in sound waves moving through a liquid. As the wave passes across the surface of an object, it causes particles to be removed from the material being cleaned. High frequency ultrasonic waves may be used with either semi-aqueous or vapor phase technologies. See Figure 7.



Particle size vs. frequency for megasonic and ultrasonic cleaning.



An illustration of the megasonic cleaning process.

Figure 8: Megasonics

♦ **Spray in Air:**

This method offers high impingement energy. It is typically used for inline continuous processes, although there are batch processes that use spray in air impingement. The spray headers provide a sheet of spray that deflects into a perpendicular spray upon hitting the surface. This allows impingement under the surface of the flip chip device. The method of cleaning has been shown to be highly effective on surface mount devices.

♦ **Spray under Immersion:**

Spray nozzles are located below the liquid level in the wash tank. The mechanical energy moves the chemistry across the surface of the flip chip assembly. Solvency of the chemistry for the soil, viscosity, surface tension, and temperature determine the length of time required in the wash tank. This method supports both batch and continuous processes.

• **Rinse solution chemistry:**

Viscosity and surface tension are both vital properties to the ability of the chemistry to clean a flip chip device; but once you get chemistry in to clean the contaminated surface, it is essential that that entire cleaning medium be removed. Incomplete rinsing can lead to off gassing which could be catastrophic to the reliability of the flip chip or any device. Therefore, it is essential that the cleaning solvent be completely soluble in the rinse medium. Moisture left under the die may be an important factor affecting thermal fatigue failures.

Time Required To Rinse Chemistry From Under the Test Vehicle:

- ♦ Water was heated to the desired temperature (±2°F) with constant stirring.
- ♦ Chemistry was placed along one edge of the die and allowed to completely underfill the die.
- ♦ The entire test vehicle was then immersed in the beaker.
- ♦ The time that it took for the water to completely remove the chemistry from under the die was taken and the value recorded.
- ♦ This was repeated at several temperatures.

The chemistry that was most soluble in the rinse medium rinsed the fastest. For example, one of the major components in one of the chemistries evaluated was hydrophobic and marginally soluble in water. Thus, an IPA rinse on this material was much more successful than water. If the chemistry was readily soluble in the rinse media, the surface tension seemed to play a role in the effectiveness of the rinse media. Surface tension increases flow, but also increases the difficulty of removing the chemistry from under the die when rinsing. Therefore, complete solubility of the chemistry in the rinse media is essential.

	Time (sec) to rinse chemistry with under 1" die.			Time (sec) to rinse chemistry with IPA under 1" die.	
Chemistry	72°F	140°F	170°F	72°F	140°F
Ionox FCR	645	160	95	540	160
Ionox HC2	750	195	74	850	180
Micronox MX2301	540	165	*Nt	510	180

*Nt = not tested

Process Parameter Observations:
Key to successful flip chip cleaning is an understanding of how the four process variables interact and effect cleaning performance. When cleaning flip chip assemblies, there are many obstacles such as low standoff, dense array and fragile device.

Cleaning Solution Chemistry:
- How soluble is the contaminant in the cleaning chemistry?
- Surface tension – Lower is better to a point
- Viscosity – Lower is better
- Flash point - Higher is better
- Solubility in rinse media – Critical

Temperature:
- Higher is better within chemical limitations
- Viscosity typically drops with increase in temperature
- Surface tension may increase – dichotomy with increase in temperature.

Time:
- The lower the standoff, a longer time required.
- The denser the array, a longer time required.
- The tighter the pitch, a longer time required

Impingement:
- The greater the impingement energy the lower time required.
- Ultrasonic not advised for active chips.
- Megasonic a possibility – test

Flip Chip Cleaning Study:
Cleaning flip chip packages evaluation was performed in the Accel® centrifugal cleaning system (Speedline Accel Corporation) using Kyzen Ionox HC2 and Micronox MX2301 semi-aqueous cleaning chemistries. The Accel® centrifugal cleaning system consists of a cleaning chamber, solvent reservoir, robotic head and microprocessor control system. The flip chip test assemblies were mounted to the robot head using a fixture. The head automatically lowers the assemblies into the cleaning chamber and seals the chamber from the surrounding atmosphere. The cleaning solution is automatically pumped from the storage reservoir into the cleaning chamber, submerging the assemblies. A microprocessor executes a program that rotates the assemblies in the solution. The assemblies rotate in one direction first, then reverse and rotate in the opposite direction. This rotation – reversal action continues for the duration of the wash interval. Following the wash interval, the cleaning solution returns to the reservoir and a rinse interval begins. With the cleaning chamber still sealed, deionized water is sprayed across the flip chip assemblies. The bi-directional centrifugal action aids the rinse water in penetrating under the die. After the rinse interval, the flip chip assemblies continue in their bi-directional rotation while hot air is introduced to speed the drying process. The flow diagram of this process is shown in Figure 9.

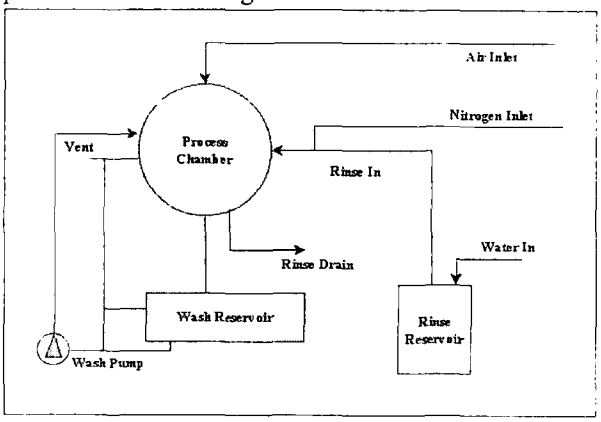


Figure 9: Accel® Process Flow

Underfill Process:
After cleaning, the test assemblies were warmed to 90°C and underfilled using Dexter Hysol® FP4549 High Performance Underfill. Dexter FP4549 is an epoxy based, low stress underfill material for use on semi-rigid and flexible substrate materials with component gaps as low as 20μm. The underfill was cured for 30 minutes at 165°C in a forced air oven and then evaluated for evidence of flow-induced voids, filler striations and incomplete fillets by acoustic microscopy using a Sonoscan Model D-6000 equipped with a 100MHz transducer.

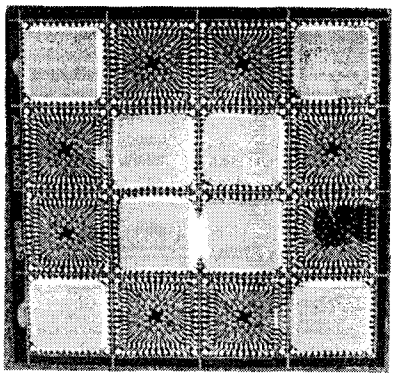


Figure 10: Test Assembly

The parts were then subjected to JEDEC level-3 preconditioning consisting of unbiased environmental soak for 192 hours at 30°C and 60% RH followed by three passes through a reflow process with a peak temperature of 240°C ± 5°C. The assemblies were again evaluated by acoustic microscopy for evidence of delamination and cracks.

Finally, the parts were subjected to pressure cooker accelerated testing at 121°C, 100% RH and 2.2 atmospheres of pressure for 48 hours. The assemblies were again evaluated by acoustic microscopy for evidence of delamination and cracks.

Acoustic microscopy analysis of the flip chip samples did show a small amount of delamination, cracking or voids created as a result of the JEDEC level-3 preconditioning process. This segment of the evaluation, was not determined to create a significant differentiation in performance between the control samples contaminated with flux residue and the samples treated with each of the cleaning processes. Acoustic microscopy analysis of the flip chip assemblies after 48 hours of exposure to pressure cooker conditions, however, shows dramatic stress related delamination at the die-to-underfill interface.

Control flip chip devices assembled using no flux contained neither underfill flow induced failures nor environmental stress related failures. The cleaning processes did not adversely affected the performance of these control (no-flux) flip chip assemblies. It is worth noting that the control assemblies were not initially reflowed prior to underfill.

Flux Formulation	Chemistry	Residue	Activity
Control - No Flux	---	---	---
A - Type A flux	Synthetic	Low	High
B - Type B flux	Synthetic	Low	Low
C - Type C flux	Synthetic	High	Medium

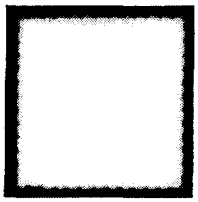
Flip chip devices assembled using Type A flux contained neither underfill flow induced failures nor environmental stress related failures. Cleaning processes utilizing IONOX® HC2 (water rinse) and MICRONOX® MX2301 (water rinse) did not adversely affect the performance of these flip-chip assemblies.

Flip chip devices assembled using Type B flux contained no underfill flow induced striations or voids. However, this flux residue caused environmental stress related delamination failures after JEDEC level-3 preconditioning and exposure to 48 hours of pressure cooker conditions. Cleaning processes utilizing IONOX HC2 (water rinse) completely eliminated the environmental stress related delamination failures. Cleaning processes utilizing MICRONOX MX2301 (water rinse) improved the performance of these assemblies through environmental stress testing; however, they did not completely eliminate all signs of delamination

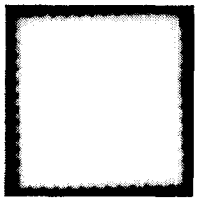
Flip chip devices assembled using Type C flux contained both underfill flow induced striations as well as severe environmental stress related delamination failures. Cleaning processes utilizing IONOX HC2 and MICRONOX MX2301 with water rinse eliminated the underfill flow striations.

Each of the cleaning processes dramatically improved the performance of these devices through environmental stress testing. Kyzen IONOX HC2 and MICRONOX MX2301 processes showed a significant improvement.

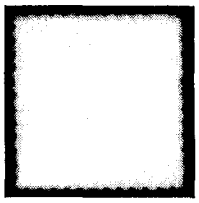
Figures 11 through 14 show acoustic microscopy images of the flip chip test devices for each material combination from initial evaluations after the underfilling operation through each of the environmental stress tests. These images are typical for the set of images gathered for each condition. Bright white areas of the acoustic microscopy images represent areas of delamination or voids. Dark black spots along the edges of each of these images are the peripheral solder bumps. Table 1 is a summation of al l the data collected.Figure 11: Control - No flux



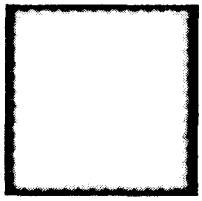
No cleaning, Initial evaluation



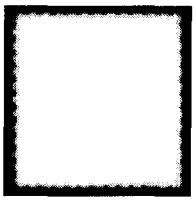
No cleaning, Post JEDEC Level-3



No cleaning, Post 48 Hrs PCT



IONOX HC2, Water Rinse, Initial evaluation



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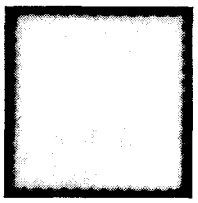
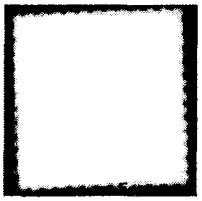
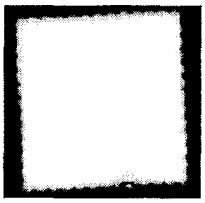


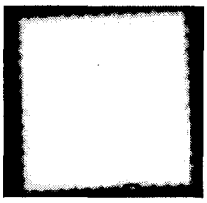
IONOX HC2, Water Rinse, Post 48 Hrs PCT



MICRONOX MX2301, Water Rinse, Initial evaluation

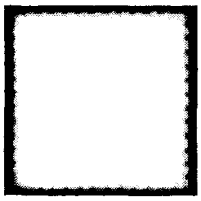


MICRONOX MX2301, Water Rinse, Post JEDEC Level-3

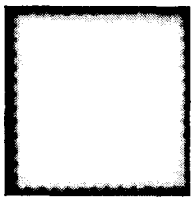


MICRONOX MX2301, Water Rinse, Post 48 Hrs PCT

Figure 12: Type A flux



No cleaning, Initial evaluation



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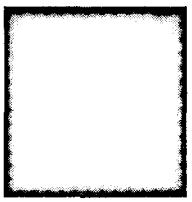

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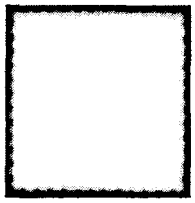
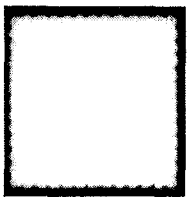
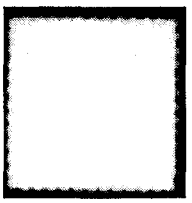


IONOX HC2, Water Rinse, Initial evaluation



IONOX HC2, Water Rinse, Post JEDEC Level-3



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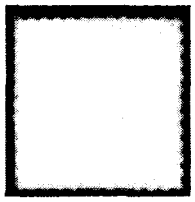
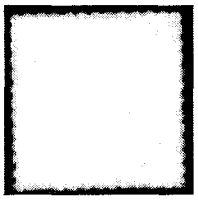
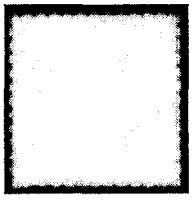


MICRONOX MX2301, Water Rinse, Initial evaluation

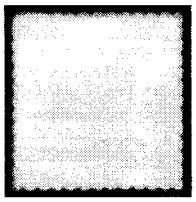


MICRONOX MX2301, Water Rinse, Post JEDEC Level-3



MICRONOX MX2301, Water Rinse, Post 48 Hrs PCT

Figure 13: Type B flux



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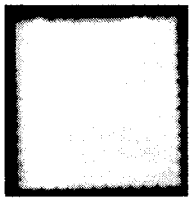

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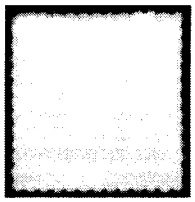

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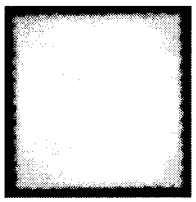
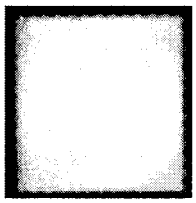
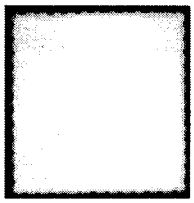


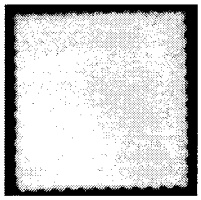
IONOX HC2, Water Rinse, Initial evaluation



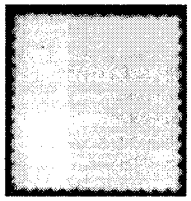
IONOX HC2, Water Rinse, Post JEDEC Level-3



IONOX HC2, Water Rinse, Post 48 Hrs PCT



MICRONOX MX2301, Water Rinse, Initial evaluation



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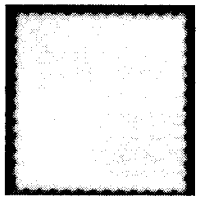
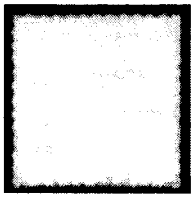
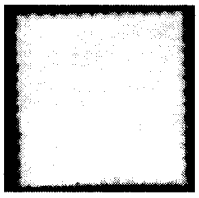


MICRONOX MX2301, Water Rinse, Post 48 Hrs PCT

Figure 14: Type C flux



No cleaning, Initial evaluation



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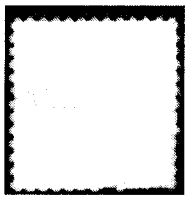

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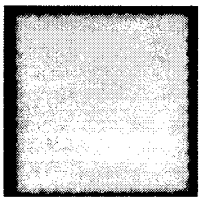
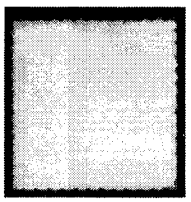
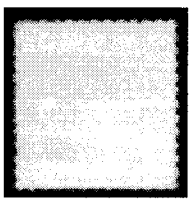


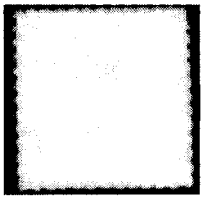
IONOX HC2, Water Rinse, Initial evaluation



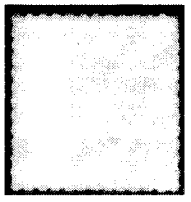
IONOX HC2, Water Rinse, Post JEDEC Level-3



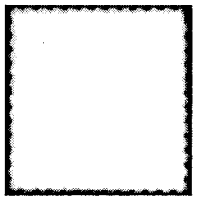
IONOX HC2, Water Rinse, Post 48 Hrs PCT



MICRONOX MX2301, Water Rinse, Initial evaluation



MICRONOX MX2301, Water Rinse, Post JEDEC Level-3



MICRONOX MX2301, Water Rinse, Post 48 Hrs PCT

Summary of Cleaning Results

Flux	Cleaning	Initial Evaluation	Post JEDEC Level-3	Post 48 Hrs PCT
Control – No Flux	Control – No Cleaning	good quality (no voids, no striations)	good quality (no voids, no striations)	Good quality (no voids, no striations)
	IONOX HC2, Water Rinse	good quality (no voids, no striations)	good quality (no voids, no striations)	Good quality (no voids, no striations)
	MICRONOX MX2301, Water Rinse	good quality (no voids, no striations)	good quality (no voids, no striations)	good quality (no voids, no striations)
Type A flux	Control – No Cleaning	good quality (no voids, no striations)	good quality (no voids, no striations)	good quality (no voids, no striations)
	IONOX HC2, Water Rinse	good quality (no voids, no striations)	good quality (no voids, no striations)	good quality (no voids, no striations)
	MICRONOX MX2301, Water Rinse	good quality (no voids, no striations)	good quality (no voids, no striations)	good quality (no voids, no striations)
Type B flux	Control – No Cleaning	good quality (no voids, no striations)	slight delamination	moderate delamination
	IONOX HC2, Water Rinse	good quality (no voids, no striations)	good quality (no voids, no striations)	good quality (no voids, no striations)
	MICRONOX MX2301, Water Rinse	good quality (no voids, no striations)	good quality (no voids, no striations)	small spherical delamination spots
Type C flux	Control – No Cleaning	severe filler striations	severe filler striations	severe delamination
	IONOX HC2, Water Rinse	good quality (no voids, no striations)	good quality (no voids, no striations)	small spherical delamination spots
	MICRONOX MX2301, Water Rinse	good quality (no voids, no striations)	good quality (no voids, no striations)	small spherical delamination spots

Test data indicates that flux residues left under flip chip die effect the flow of underfill materials resulting in striations and voids. Furthermore, if subjected to severe environmental conditioning, Type C flux contaminated flip chip devices may prematurely fail due to interfacial delamination. Control flip chip devices assembled using no flux showed no signs of voids, striations or delamination after environmental testing. It is important to note that the no-flux control devices were not reflowed prior to underfill. These devices were not reflowed prior to cleaning and underfill due to the fact that without flux, the solder will not properly reflow, thus yielding a device that cannot be handled. Test devices assembled using Type A flux showed no indications of voids, striations or delamination after environmental testing. However, test devices assembled using Type B flux and Type C flux contained flow induced failures including voids and severe striations as well as environmental stress related delamination failures. Type A flux provided the most robust flip chip assembly for the test conditions evaluated. Type A flux has very low solids, which results in a very low residual contamination beneath the die. One may ask, therefore, why not select Type A flux or use no-flux in the assembly of these devices to maximize performance. The answer is the soldering assembly yields and solder joint integrity rely on the activity of the flux. Type A flux has lower "fluxing" activity than the other fluxes evaluated. In some cases, this flux may provide inadequate fluxing activity to create high performance solder joints. As stated before, flip chip assemblies with high I/O may require high fluxing activity to ensure complete connections.

Both Type B flux and Type C flux are higher activity fluxes which leave behind higher levels of residue. As a

result, there are voids, flow striations and delamination on control samples in which no cleaning or reflow prior to underfill was performed. Cleaning processes utilizing IONOX HC2 (water rinse) and MICRONOX MX2301 (water rinse) dramatically improved the underfill flow performance and flip chip mechanical stability of test devices assembled using Type B flux and Type C flux without causing negative effects to these devices. These cleaning processes provide ideal surfaces after cleaning for optimal underfill performance beneath a soldered flip chip device, thus eliminating premature failure due to flux residue and extending the life of the device.

Conclusion:

IONOX HC2 and MICRONOX MX2301with a water rinse consistently provided the best surface for bonding. These cleaning processes removed Type A flux and Type B flux post-reflow residues, which provided excellent reliability through JEDEC level-3 preconditioning and 48 hours of PCT exposure. Furthermore, these cleaning processes did not degrade the performance of the devices in any way. Further investigation of the chemistries and processes used in these cleaning procedures will proceed to develop optimal processes for other flux/underfill combinations.

The chemistries used in this evaluation are all semi-aqueous blends designed for use in de-fluxing flip chip, chip scale and micro-BGAs. Removal of flux residues in these applications can be very difficult due to the tacky fluxes that are often used as well as the overall size and space available for removal. These chemistries are specifically designed to solvate these tough-to-remove residues. Likewise, they are designed for use in both inline and batch semi-aqueous cleaning equipment.

Flip chip standoff and pitch must drive the cleaning chemistry selection. If the standoff is below 50 microns, low viscosity and the operating temperature are key. Time must also be considered. Static cleaning tests will give a safe operating window to consider. Impingement sources will open the window. The four process parameters of time, energy, solvency and temperature must all come together in an integrated solution.

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