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CSP + HDI = MCM!

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Abstract: *MCM technology languished throughout most of the 1990's due to high costs resulting from low yields and issues with known good die. During the last five years of the decade new developments in chip scale packages and high density, build up multi-layer printed wiring boards created new opportunities to design and produce ultra miniaturized modules using conventional surface mount manufacturing capabilities. Focus on the miniaturization of substrate based packages such as ball grid arrays (BGAs) resulted in chip scale packages (CSPs) offering many of the benefits of flip chip along with the handling, testing, manufacturing and reliability capabilities of packaged devices. New developments in the PWB industry sought to reduce the size, weight, thickness and cost of high density interconnect (HDI) substrates. Shrinking geometries of vias and new constructions significantly increased the interconnect density available for MCM-L applications. This paper describes the most promising CSP and HDI technologies for portable products, high performance computing and dense multi-chip modules.*

Introduction:

Multi-Chip Module (MCM) packaging for high performance applications dominated these markets throughout the 1970s and 1980s, but during the 1990s growing demand for miniaturization and increased functionality drove interest in MCMs for commercial and consumer products, particularly in the computing and telecommunications arenas. Unfortunately, traditional MCM interconnect substrates and assembly technologies proved too costly for all but the most sophisticated applications.

As market pressures continued to grow, developments in organic build up technologies began to show promise for cost reductions at the substrates level, but product assembly reliability lagged due to coefficient of thermal expansion (CTE) mismatch between silicon die and organic substrates. New assembly solutions came forward employing alternative attachment materials and methods but were not readily accepted due to infrastructure incompatibilities and lack of fundamental reliability experience and understanding.

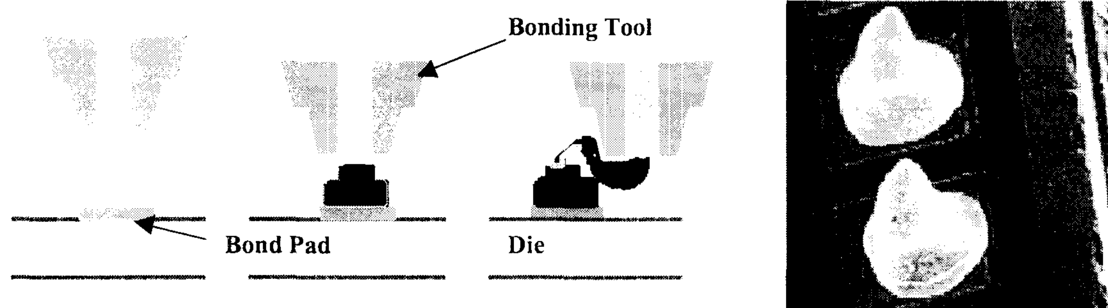
Today two solution directions compete for dominance in miniaturized, high functionality consumer products; bare die on organic high density interconnect (HDI) printed wiring boards (PWBs) versus chip scale packages (CSPs) on either HDI or advanced conventional PWBs. The focus here is to identify key technologies facilitating both solution options and technically differentiate the drivers behind each approach.

Bare Die Solutions:

Alternatives to conventional soldered flip chip or chip and wire assembly of bare die onto organic substrates include conductive adhesive flip chip bumping (ThermoSet Corp.) and stud bump bonding (Matsushita, Fujitsu, PFA, etc.). Both approaches take advantage of the compliance of organic

adhesive formulations to enhance thermal fatigue reliability, but sacrifice connection resistance to an extent (~10-20 milli-Ohms per connection increase over soldered flip chip).

The stud bump bonding (SBB) solution offers significant reduction in bond pad pitch at the die level over soldered flip chip with advanced capabilities approaching 50 micron pitch. SBB employs a wire bonding machine to create the requisite bumps on the die bond pads as shown in Figure 1. Techniques for creating the actual electrical connection include the use of conductive adhesive (Matsushita), thermo-compression bonding (Fujitsu) and mechanical compression (PFA). To date the most widely adopted technique is the conductive adhesive approach used extensively by Matsushita in both MCM and CSP package assembly applications.



Courtesy Matsushita Electric Industries Co., Ltd.

Figure 1. Bump formation using wire bond machine (Stud Bump Bonding).

For low cost "throw away" type consumer products with short product lifetime expectations PFA's mechanical compression technique provides a simple yet effective solution. In this case the die is bumped using a wire bond machine placed onto the organic substrate pre-coated with an underfill composition. Curing of the underfill while maintaining substantial normal pressure on the die results in a mechanical compression connection which relies on the elastic properties of both the substrate and the underfill itself.

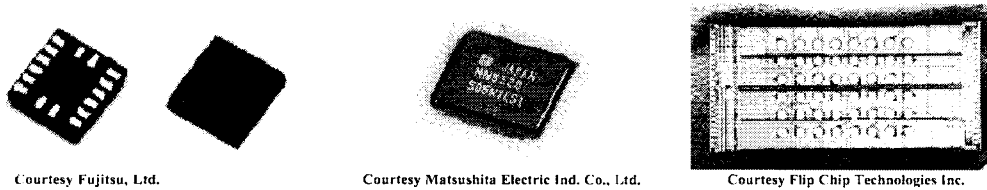
Printed conductive adhesive bump materials, generally silver epoxy based, require a gold under bump metallurgy (UBM) on both the die and the substrate to ensure sound electrical connection. There are three types of bumping material produced. Thermoset bump material may be applied to the wafer, fully cured and then attached to a substrate using a separate conductive adhesive application. This results in a structure similar to the SBB approach. Alternatively a partially cured or B-stage bump material can be applied to the wafer. Once the die are singulated they can be simply placed on the board and the B-stage material fully cured in place. Finally, a thermoplastic bump material may be applied to the wafer and cured then placed onto a pre-heated substrate, which initiates "re-melting" of the bump prior to cooling to finish the attachment.

Although SBB techniques, and conductive adhesive approaches in general, display very high cycles to "failure," the failure mode and mechanism differ substantially from that of conventional soldered electrical connection technologies. As noted

previously, adhesive based flip chip technologies display higher connection resistance than solid metallurgical connections. Failure generally presents itself as gradual resistance increases rather than the open circuit or intermittently open circuit failure mode of solid metal connections. For circuits not sensitive to minor variations in connection resistance this can offer as much as an order of magnitude improvement in reliability. However, linear circuits operating at very low voltages may display anomalous behavior when using these assembly techniques.

The Micro-Package (CSP) Alternative

The advent of micro-packages or chip scale packages (CSPs), especially through the latter half of the 1990s, opened the doors to MCM like densities for most designers. Driven by portable telecommunications applications, these packages now find use not only for memory devices but for many logic parts as well. Early proliferation of CSP technical options stalled markets for a few years, but interposer based solutions found their way into the dominant position by mid 1998 and growth accelerated from then. Many CSPs adapt well to specific applications such as Shellcase for optical devices, but today the most versatile and popular alternatives include wire bonded versions similar to the early Texas Instrument Micro-Star or flip chip styles based on the Motorola SLICC (Slightly Larger than IC Carrier) or JACS (Just About Chip Size) packages. Newer redistribution type CSPs founded on Sandia's work with copper polyimide build up at the wafer level continue to grow rapidly in popularity as thermal fatigue reliability solutions develop. Figure 2 displays examples of some CSPs representing these packages families.



Courtesy Fujitsu, Ltd. Courtesy Matsushita Electric Ind. Co., Ltd. Courtesy Flip Chip Technologies Inc.

Figure 2. Examples of various chip scale packages.

CSPs enable MCM densities using more conventional design and assembly technologies, often even simplifying the assembly process through elimination of mixed technology manufacturing. For example, a conventional chip on board (COB) MCM manufactured on a PWB substrate demands coordination of the wire bond process with solder or adhesive attachment of passive components. Additionally, CSPs generally expand the lead pitch over flip chip implementations greatly easing the routing and layout of the substrate and usually reducing substrate cost compared to more traditional MCMs. Although IC design specifically for flip chip can open the lead pitch as well, CSPs offer this capability for essentially any IC and allow a single IC design to be employed in COB, CSP or conventional leaded package configurations.

Comparable MCM miniaturization can be achieved using CSPs, flip chip or COB. In fact COB usually, though not always, results in the largest footprint of these three choices

due to glob top type encapsulation. Underfill of flip chip devices requires a design footprint area increase of at least 15% and generally 20% or slightly more. CSPs generally occupy a PWB footprint 20% to 25% greater than the die itself making them very competitive with even flip chip MCMs. The height profile of finished MCMs using CSPs generally exceed those manufactured with COB or flip chip assembly, the trade off being simpler testing and trouble shooting of designs as well as pre-qualified assembly reliability.

Substrate Choices

Traditional ceramic multi-layer and thin film MCM substrates work well with both conventional assembly methods and the leading edge bare die and CSP techniques described above. In many cases they can be very cost competitive, particularly when dielectric loss or thermal management issues strongly influence substrate selection. However the available design infrastructure for PWB type substrates permeates the industry and newer HDI technologies provide a wide array of choices for MCM implementation.

For bare die designs materials systems with a tailored CTE approaching 10 ppm/°K or less greatly enhances thermal fatigue resistance. Proper selection of underfill materials for the adhesive based flip chip approaches described earlier does allow their use even with more common materials systems such as bismalemide triazine (BT) or multi-functional epoxies. Older FR-4 epoxy systems are not a good choice except with appropriately characterized CSPs since they do not hold up well to wire bonding temperatures for COB designs and very high strain in flip chip connections results from solder temperature excursions to attach passive components. BT and multi-functional epoxy systems, with their high T_g, show more CTE stability at high temperatures reducing the level of strain introduced despite their CTE's being nearly the same as conventional FR-4 at room temperature. The use of very thin core (< 65 microns) laminates in multi-layer PWB structures results in a higher proportion of glass reinforcement and thus a slightly lowered CTE (~13-15 ppm/°K) and some minor improvement in thermal fatigue reliability. Aramid fiber based products provide one of the most attractive materials solutions with a CTE below 10 ppm/°K, although the current cost penalty tends to limit its application to relatively small and very dense MCMs.

In addition to materials selection, the organic MCM or PWB multi-layer structure also makes a great difference in both the space efficiency and electrical performance of the module. Two basic design options present themselves as depicted in Figure 3, staggered via build ups as on the left and stacked via constructs as on the right.

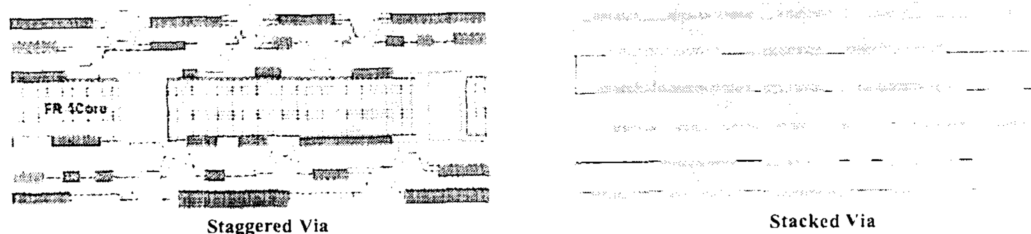
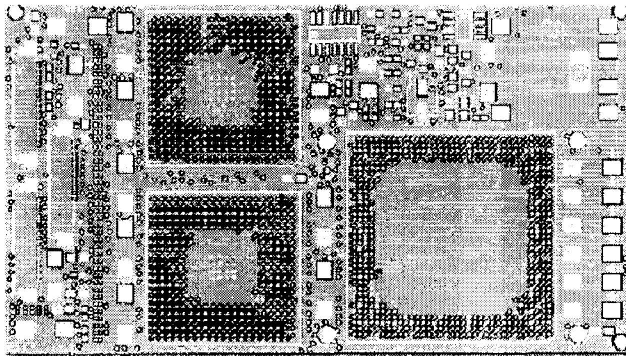
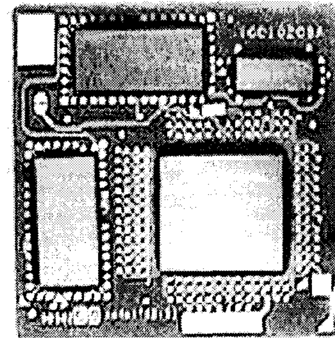


Figure 3. Typical HDI build up structures.

Staggered via systems readily adapt to design using current PWB CAD systems, but sacrifice routing density capacity in comparison to stacked via technologies. When using equivalent line/space and via/pad geometries the routing capacity loss can approach 20% depending on the type of circuit application. Typically staggered via technologies prove sufficient for most CSP implementations of MCM products. For bare die applications, especially using SBB, adhesive bumping or conventional flip chip assembly techniques, stacked via HDI boards offer greater flexibility, ease of assembly and miniaturization. Figure 4 shows examples of two MCMs, one Dycostrate technology based, staggered via CSP implementation and the other a Matsushita ALIVH (any layer inner via hole) stacked via SBB flip chip application.



Dycostrate/PERL µP
(Courtesy HP)



ALIVH SBB µP
(Courtesy Matsushita Electric Ind., Ltd.)

Figure 4. MCM application examples.

Summary and Conclusion

Clearly the combination of leading edge MCM technologies such as organic HDI PWBs with advanced CSP packages and/or adhesive based flip chip techniques makes MCM products available to very broad segments of the electronics industry. Applications in hand held devices of all types, from palm type computers to cellular telephone handsets and pagers, abound. Inroads continue even in higher performance CPU and memory modules as well as high definition, digital television products. But the power of these approaches lies in their accessibility by essentially any designer. The greatest remaining roadblock to widespread adoption is manufacturing capacity, not technology or infrastructure capability.

Introduction of copper (Cu) metallization at the IC level along with renewed interest in Cu ball bonding equipment development will spur further SBB technology advancements. These will include even finer lead pitch capability (the hardness of copper results in less ball deformation or spreading during bump creation), solder assembly capability (protection of the bond pad/bump junction will be necessary, but the Cu bump readily accepts solder) and perhaps even enhanced thermal fatigue resistance. Continued progress in wafer level CSP development reduces cost as well as size and offers greatly improved electrical performance opportunities.

Put together with heavy investments in

advanced HDI interconnect fabrication capacity, both CSP and flip chip assembly will proliferateover the next decade. These leading edge MCM technologies will soon be mainstream manufacturing options for most OEMs.

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