Package Design for Protecting Active Chip Surface from Damage due to a Dicing Saw Blade

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1. Introduction

In general, semiconductor IC chips are formed on a single semiconductor wafer during a batch processing method, which provides great economic benefit and inceases productivity. Individual IC chips are seperated from the wafer during the wafer sawing or dicing step.[1-3] During subsequent assembly processe steps, the edge portions of the individual chips can be very susceptible for mechanical damage due to a saw blade. Defects formed along the chip edges due to the dicing saw blade often provide sources to cause serious reliability problems because the impact due to the rotating saw blade is directly transferred to the semiconductor wafer.[4-5] The degree of damage on the chip edge depends on various factors including saw blade thickness, the revolution speed of the saw blade, the width of scribing area and the package structure. The closer the scribing position of the saw blade on the IC device, the greater the impact of the saw blade to the IC patterns. Therefore, it is necessary to reduce the negative impact of the saw blade while maintaining close proximity of the scribe lines to the IC devices. Various attempts such as the modification of package structure to prevent reliability degradation due to the saw blade were done in the present work.

2. Experimental Procedure

6 inch silicon wafers were initially deposited by thermally grown oxide (SiO_2) to a thickness of 1 ㎛ and then were sputter-deposited by aluminum metal conductors and passivation (SiN).[6-7] The oxide layer mostly covers the whole surface of the semiconductor wafer including scribe regions for dividing the semiconductor chips as well as device regions. Some test specimens were prepared to include discontinuous pattern regions that are formed by partially removing the oxide layer and passivation on the scribe regions. Etching methods used in conventional photolithography processes were employed to remove the pattern layers on the sribing regions during the wafer manufacturing process. [8]

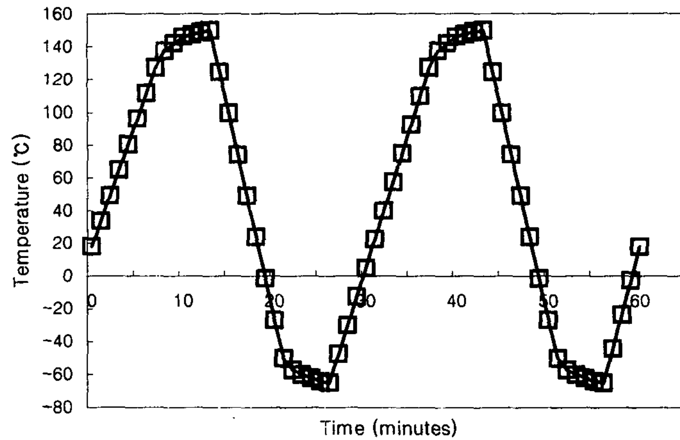

Figure 1. Temperature vs time profiles in the chamber for the thermal cycle tests performed in this work.

In order to study the effect of manipulating the sawing process on the reliability of the IC devices, the thickness of the saw blade was controlled to have five to ten times greater than the total thickness of the pattern layers on the IC devices. Further, the revolution speed of the saw blade was controlled to have a value of from 30000 to 60000 rpm. During scribing with a diamond-pointed saw blade, the wafer was fully cut and therefore was immediately seperated into its individual chips. The size of the seperated dies was 2.0x1.1 cm^2.

Thermal cycling tests were performed to accelerate damage due to the dicing saw blade. Predetermined time to validate reliability was 1000 cycles. For each set of experiments, nominally identical specimens were placed in the thermal cycle chamber, then individual functionally tested after predetermined periods (i.e. 100, 500 and 1000 cycles). Test specimens underwent thermal displacement-induced fatigue at temperature ranges from -65℃ to 150℃ within 30 min time period. See Figure 1. Once any functional failure was found, the corresponding specimens were decapped and examined under an optical microscope (OM) and scanning electron microscope (SEM) to charaterize mechanical damage on the edge portions of the IC chips due to the dicing saw blade.

3. Results and Discussion

Figure 2 is a schematic draw showing the wafer dicing process. This figure illustrates a conventional wafer sawing process step. A wafer, having a number of IC devices formed thereon, is mounted to a wafer ring. An adhesive tape attached to the inactive back surface of

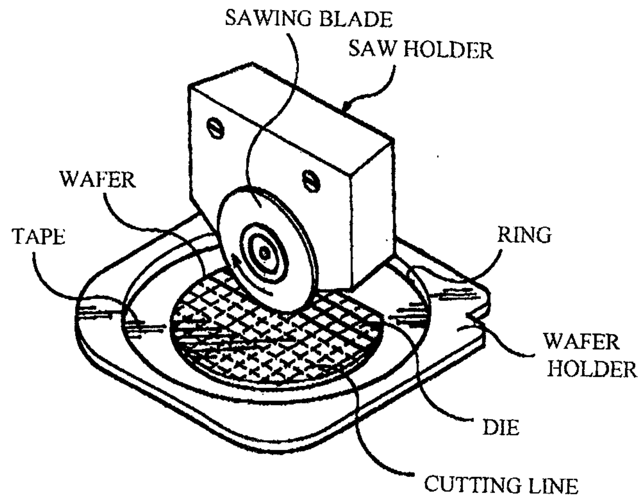

Figure 2. A schematic draw showing the wafer dicing process.

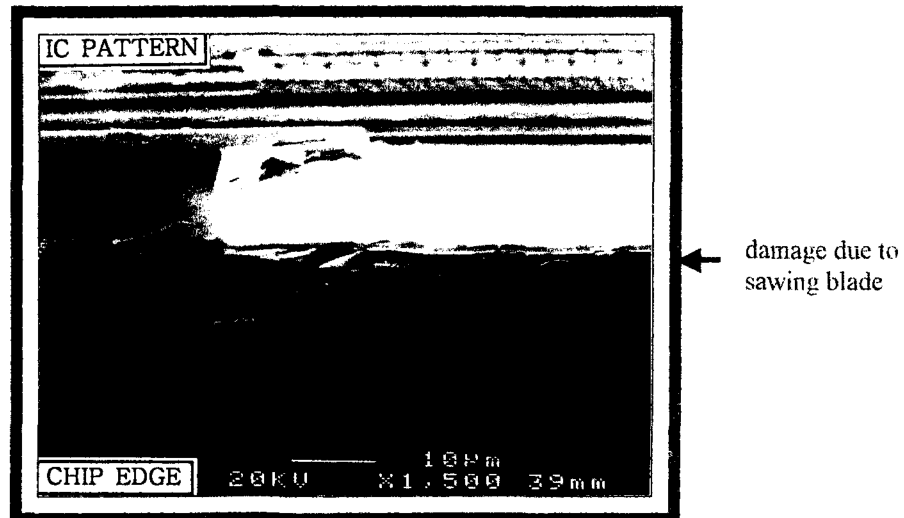

Figure 3. A scanning electron micrograph showing damage due to a dicing saw blade.

the wafer supports the separated chips during subsequent process steps, e.g. a die attaching step. The wafer ring is mounted to a wafer sawing machine and the wafer is scribed along the scribe lines by a saw blade, and thereafter separated along such lines to divide the wafer into individual chips. Thus, when the saw blade passes along the scribe lines, damage due to the rotating saw blade can occur on the edge portion of the individual die. The damage can result from the peeling of the pattern layer from the silicon wafer. The peeling initiated at the chip edge often results in functional errors during thermal cycling tests since the peeling off of the pattern layers on the scribe regions easily advances to the IC devices. Figure 3 is a scanning electron micrograph showing damage due to a dicing saw blade.

Table 1. The effect of sawing process on thermal cycling reliability of the individual chips.

Sawing speed (㎛)	Blade thickness (㎛)	Number of failure
30000	20	1
	25	4
	30	5
45000	20	3
	25	5
	30	6
60000	20	2
	25	5
	30	4

In order to prevent reliability degradation due to the saw blade the thickness of the saw blade and the revolution speed of the saw blade was manipulated. The effect of saw blade thickness and the revolution speed of the saw blade on the thermal cycling reliability of the individual chips is shown in Table 1. These data show that the reduction of saw blade thickness by 30% is not enough to protect the IC patterns completely from the impact due to the dicing saw blade. This method has a weak point because the thinning of the saw blade will lead to productivity reduction because of its fast wear and tear.

It was also found that the enlargement of the scribe regions by 75% obviously improves the thermal cycling reliability of the IC devices. If the scribing position of the saw blade is far away from the IC device, the impact of the saw blade on the IC patterns will be considerably reduced but the number of the seperated IC devices from the single wafer decreases, which results in productivity reduction.

In order to reduce the negative impact of the saw blade while maintaining close proximity of the scribe lines to the IC devices, a portion of pattern layers formed throughout an active surface of the wafer was selectively removed to provide the discontinuous pattern layers on the wafer. Then, the wafer was sawed along the scribing regions where the layers have been partially removed. The thickness of the saw blade was 30 ㎛ and the revolution speed of the saw blade was 30000 rpm. The thermal cycling tests show that no failure was observed at the IC chips,l whose scribing regions have a width of 120 ㎛, even after 1000 cycles. So, we see that to form the discontinuous layer region on the scribe region is a very effective way to avoid reliability degradation due to the saw blade. This is presumably due to that the scribing regions lack the pattern layers that norminally transmit the impact of the saw blade to the device regions during thermal cycling. In this way, a plurality of semiconductor chips can be formed on an active surface of the semiconductor wafer without causing any impact of the saw blade on an IC device. On the other hand, when the width of the scribe region (where the layers are absent) is reduced, failures were still observed.

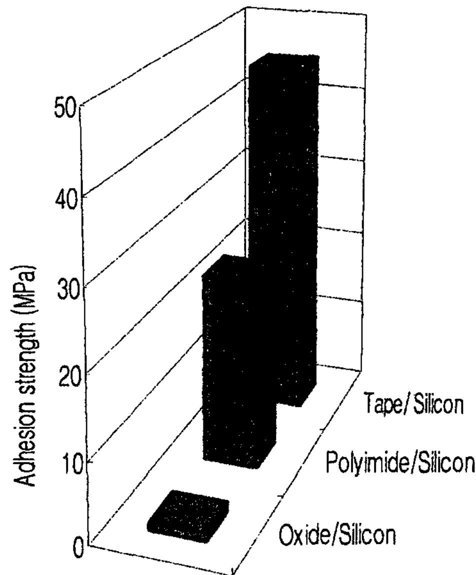

Figure 4. The adhesion strength between various materials and bare silicon.

The polyimide film was coated to extend into a portion of the discontinuous scribe regions in order to protect the IC pattern layers of the device regions from the saw blade. The thermal cycling tests show that in this way, no failure was observed even at the IC chip (whose scribe region has a width of 100 ㎛ or less). This indicates that when the poyimide layer covers a portion of the discontinuous region and directly contacts the bare surface of silicon, it effectively resists chipping as well as peeling due to the saw blade. Indeed, the polyimide was investigated to have a considerably larger adhesion strength with the bare silicon surface, compared with the pattern layers. Figure 4 shows the adhesion strength between various materials and bare silicon. This graph indicates that the adhesion strength of the silicon oxide layer to the bare silicon surface is about 2.4MPa. However, if the polyimide layer was directly coated on the same silicon wafer without the silicon oxide layer, the adhesion strength of the polyimide layer to the silicon surface increased to ten times. It is partially due to that the height of the pattern layers (3 ㎛) formed on the deivce regions is much less than the height of the polyimide layer (10 ㎛). Similarly, an adhesive tape can also be an excellent protective layer on the discontinuous layer regions due to its very high adhesion strength with the bare silicon wafer and the resulting great capacity to absorb the force of the impact due to the saw blade. However, it was investigated in my previous report that close proximity of the tip of an adhesive tape to the chip edges, corresponding to the scribe regions of the semiconductor wafer, can degrade thermal cycling reliability in a plastic package. This is because the high thermal shrinkage of the adhesive tape having a thickness of 25 ㎛ allows to transfer the impact due to the rotating saw blade to the IC pattern during thermal cycling. [7]

Consequently, even though the adhesive tape is an excellent protective layer for protecting damage due to a sawing blade, it can also cause another reliability problem due to its large thermal displacement. So, the best way to protect the pattern layer from damage due to a sawing blade is the formation of the polyimide or very thin adhesive layer on the discontinuous scribe regions of the IC chip.

Acknowledgments

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