Reactive RF Magnetron Sputter Deposited Y_2O_3 Films as a Buffer Layer for a MFIS Transistor

Dong Gun Lim, Bum Sik Jang, Sang Il Moon, and Junsin Yi

Abstract

This paper investigated structural and electrical properties of Y_2O_3 as a buffer layer of single transistor FRAM (ferroelectric RAM). Y_2O_3 buffer layers were deposited at a low substrate temperature below 400℃ and then RTA (rapid thermal anneal) treated. Investigated parameters are substrate temperature, O_2 partial pressure, post-annealing temperature, and suppression of interfacial SiO_2 layer generation. For a well-fabricated sample, we achieved that leakage current density (J_{leak}) in the order of 10^{-7} A/cm^2, breakdown electric field (E_{br}) about 2 MV/cm for Y_2O_3 film. Capacitance versus voltage analysis illustrated dielectric constants of 7.47. We successfully achieved an interface state density of Y_2O_3/Si as low as 8.72x1010 cm^{-2}eV^{-1}. The low interface states were obtained from very low lattice mismatch less than 1.75%.

Key Wards : FRAM, Y_2O_3, RTA, interface state, lattice mismatch

1. INTRODUCTION

The metal-ferroelectric-silicon (MFS) structure is widely studied for nondestructive readout (NDRO) memory devices, but conventional MFS structure has two critical problems [1]. The one that is difficult to obtain ferroelectric films like PZT on Si substrate without interdiffusion of impurities such as Pb, Ti and other elements. Diffusion of Pb or Ti induces increased trap density and Fermi level pinning. The other one is that PZT/Si structure generates nonferroelectric and low dielectric constant layer at the interface. Unintentionally, the interfacial oxide layer causes problems of device instability, capacitance reduction, and increases memory-switching voltage. Because voltage drop across the unwanted interfacial oxide layer is very high, we have to supply the higher input voltage to operate ferroelectric films in write and read mode. In order to solve these problems, the metal-ferroelectric-insulator-silicon (MFIS) structure has been proposed with a buffer layer of high dielectric constant like Y_2O_3. Buffer layer candidate should meet the following requirements of low lattice mismatch, low leakage current, low interface state density, high dielectric constant, chemical stability, and prevention of interdiffusion. Y_2O_3 films were investigated because these materials can meet the prior mentioned requirements [2]. Y_2O_3 takes one of the cubic structure and shows similar lattice constant (a_{Y2O3}=1.060 nm) to silicon (a_{Si2}=1.086 nm) [3]. Generally, crystalline Y_2O_3 films are formed at a high deposition temperature. However, the high process temperature causes a chemical reaction with Si substrate to produce silicide. To avoid silicide formation while keeping good interface

* School of Electrical and Computer Engineering, Sungkyunkwan University
(300 Chunchundong, Jangan-gu, Suwon, Kyunggi-do, 440-746 Korea
FAX : 0331-290-7159, E-mail : dglim@ece.skku.ac.kr)

properties, Y_2O_3 films were deposited at a relatively low temperature below 400℃. Then the samples were post-annealed at 700~900℃ using RTA (rapid thermal anneal) method.

2. EXPERIMENTAL

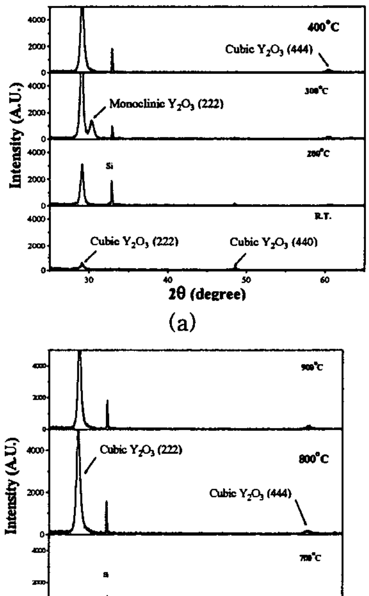
P-type Si (100) wafers with a resistivity ranging from 20 to 40 Ω-cm were used as substrates. Substrates were cleaned in acetone, methanol, and deionized water. Backside ohmic contact was carried out by thick Al deposition and thermal treatment at 550℃ for 30 min. During the backside contact treatment, nitrogen gas was supplied at a rate of 2.5 *lpm*. To remove thin oxide layer that may have formed during backside contact treatment, front surface of Si was dipped to BHF (49% HF:H_2O = 1:10) for 40 seconds. Promptly loading the Si substrate, we created base pressure of low 10-6 torr before the Y_2O_3 thin films growth Y_2O_3 buffer layers were grown by 13.56 MHz rf reactive magnetron sputtering system with a Y metal target of 2-inch diameter. Prior to the buffer layer deposition, we placed an extremely thin Y metal as a seed layer that promote buffer layer deposition and prevent interfacial SiO_2 layer formation.

To optimize process parameters of Y_2O_3 buffer layer, this paper investigates various experimental conditions such as substrate temperature, O_2 partial pressure, post-annealing temperature, and suppression method of interfacial SiO_2 layer generation.

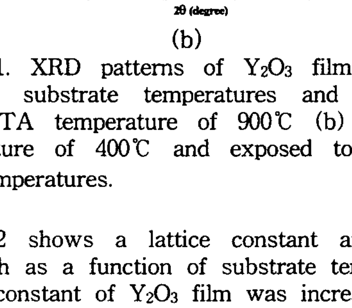
We carried out RTA treatments in an oxygen ambient at 700-900℃ for 120 sec. AFM (atomic forced microscopy) and AES (Auger electron spectroscopy) were employed to examine a surface structure and chemical element analysis of Y_2O_3 on Si. The crystallinities of Y_2O_3 thin films were investigated by X-ray diffractormeter (XRD) of Mac. Science M18XHF-SRA. Leakage current density, breakdown electric field, and current-voltage-temperature(I-V-T) properties were measured using a Keithley 617 multimeter and Fluke 5100B voltage source. Capacitance-voltage (C-V) characteristics were measured using a Boonton 7200 C-V meter at 1 MHz.

3. RESULTS AND DISCUSSIONS

The crystalline structure of the Y_2O_3 film deposited at various conditions such as substrate temperature, post-annealing temperature, and O_2 partial pressure. Fig. 1 shows XRD results on Y2O3 thin films grown at a substrate temperature less than 400℃ and subsequently annealed at 70 0℃, 800℃ and 900℃. The films exhibited a major peak of (222) and weak peaks of (444), (440) planes. As the film growth temperature increased, we observed that the strongly (222) preferred (Fig. 1 (a)). As can be seen from Fig. 1 (a), Y_2O_3 films transformed from amorphous to polycrystalline structure as the post-annealing temperature increased from 700℃ to 800℃ (Fig. 1 (b)). The diffraction peaks of films grown below substrate temperature of 300℃ or O_2 partial pressure of 10 % are consistent with the peak of monoclinic yttrium oxide (Fig. 2 (a)). These results indicate that as the substrate temperature or O_2 partial pressure decrease, the generated Y_2O_3 films have less oxygen content [4, 5]. This oxygen deficiency in the film may have promoted the formation of monoclinic Y_2O_3 phase. Substrate temperature above 400℃ or O2 partial pressure higher than 20 %, the monoclinic structure was disappeared and the cubic Y_2O_3 phase was dominated in XRD spectra.



(a)



(b)

Fig. 1. XRD patterns of Y_2O_3 films for (a) different substrate temperatures and subjected fixed RTA temperature of 900℃ (b) substrate temperature of 400℃ and exposed to different RTA temperatures.

Fig. 2 shows a lattice constant and lattice mismatch as a function of substrate temperature. Lattice constant of Y_2O_3 film was increased from 1.03 nm for RT to 1.06 nm for 400℃. These values equal to two times of Si lattice constant.

Lattice mismatch of Y_2O_3 film was decreased from 5 % RT to 1.75 % after 900℃ RTA treatment.

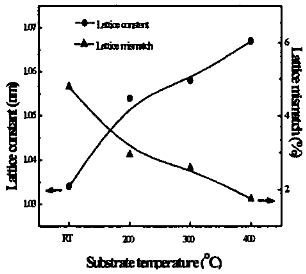
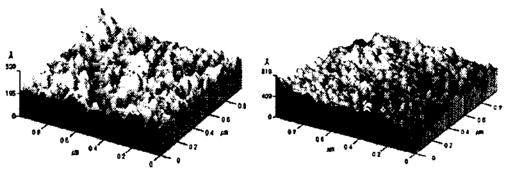


Fig. 2. Lattice constant of Y_2O_3 films and lattice mismatch with Si substrate as a function of substrate temperature.

For an MFIS structure, ferroelectric materials are to be grown on top of buffer layer. Therefore, good surface roughness is an important factor. The surface roughness of the Y_2O_3 films is shown in Fig. 3 for different post-annealing temperature and O_2 partial pressure. With the elevation of the post-annealing temperature, surface roughness was reduced by the relaxation of built-in stresses. As increasing the O_2 partial pressure, surface roughness was increased because excess O_2 may assist the formation of Y_2O_3 cluster phase in the film. The Y_2O_3 films annealed at 900℃ and with 20 % O_2 partial pressure exhibited the best surface roughness characteristics.



(a) (b)

Fig. 3. AFM image of Y_2O_3 films for different O_2 partial pressure (a) 20 % (b) 40%

The I-V characteristics of Y_2O_3 films indicated that RTA improved the leakage current of the films from Jleak in the order of 10^{-6} A/cm^2 to 10^{-8} A/cm^2. The decrease of leakage current characteristics with RTA treatment thought to be resulted from the improvement of crystallinity and stoichiometry. Y_2O_3 film grown at a substrate temperature of 400℃ showed the breakdown electric field higher than 2 MV/cm.

Fig. 4 shows ln(J)-$E^{1/2}$ plot for Y_2O_3 film that was grown at 400℃ and annealed at 900℃. The Y_2O_3 leakage current shows Ohmic behavior was observed at a low electric field region. In a high electric field region, we were able to find a linear relationship of ln(J) $E\propto^{1/2}$. This result indicates that dominant conduction mechanism of Y_2O_3 film is the Schottky emission [6].

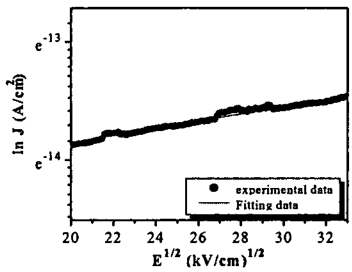


Fig. 4. ln(J) versus $E^{1/2}$ plot for Y_2O_3 film prepared at a substrate temperature of 400℃ and at a post-annealing temperature of .900℃

From the J-V-T result in Fig. 5, we calculated the barrier height of Al/Y_2O_3/ p-type Si capacitor. A basic requirement for the Schottky emission is that a plot of ln(J/T^2) versus 1/T should be a straight line. When ln(J/T^2) is plotted against 1/T, the slope of the straight line is the barrier height. The barrier height was estimated to be about 0.5 eV [7].

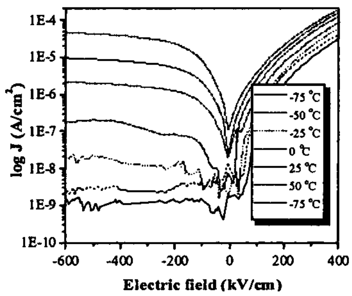


Fig. 5. J-V-T curves of Y_2O_3 film prepared at substrate temperature of 400°C and post-annealing temperature of 900°C.

Fig. 6 shows 1 MHz C-V result of MIS capacitor with Y_2O_3 layer grown at 400℃ and annealed at 900℃. The Y_2O_3 films after RTA anneal treatment exhibited the higher dielectric constant and the lower interface trap density (Dit) than that of as-grown sample due improved chemical stoichiometry and film crystallinity. Dielectric constant was improved from 4.94 without RTA to 7.47 with 900℃ RTA treatment. After RTA treatment at 900℃, Dit between Y_2O_3 and Si calculated as low as 8.72×10^{10} cm^{-2}eV^{-1} in midgap state. This result indicates that interface states between Y_2O_3 and Si are better than that of SiO_2 layer and indirectly indicating that an interfacial SiO_2 generation is successfully suppressed.

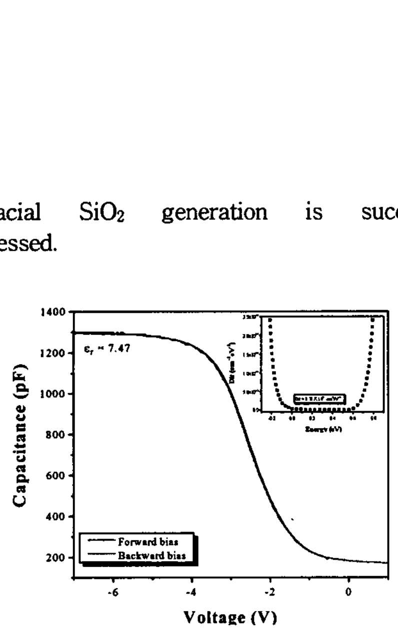


Fig. 6. C-V characteristic of MIS capacitor with Y2O3 layer grown at 400℃ and annealed at 900℃

In order to investigate the existence of interfacial SiO_2 layer between Y_2O_3 and Si, Auger electron spectroscopy (AES) depth profiles was measured. Fig. 7 shows AES depth profile of Y_2O_3 layer grown at 400℃ and annealed at 900℃. AES study on the Y_2O_3 films showed that yttrium and oxygen compositions were formed as an excellent stoichiometric Y_2O_3 film. The carbon contamination may come from oil vapor in the residual gas. AES result clearly shows that any unintentional SiO_2 layer was formed at the interface between Y_2O_3 and Si. We observed that interface transition regions were divided into oxygen-rich and Y-rich regions. However, this transition region is not strongly influence the electrical properties of Y_2O_3 MIS capacitor.

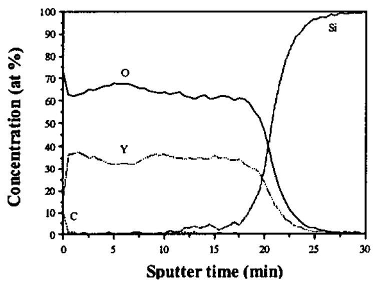


Fig. 7. AES depth profile for Y_2O_3/Si prepared at 400℃ and annealed at 900℃.

CONCLUSIONS

In this paper we investigated a feasibility of Y_2O_3 films as a buffer layer of MFIS ferroelectric transistor. Buffer layers were prepared by two-step processes using a low temperature film growth and subsequent RTA treatment. By employing an ultra thin Y pre-metal layer, unwanted SiO_2 layer generation was successfully suppressed at an interface between the buffer layer and Si substrate. With RTA treatment, we improved the leakage current density of Y_2O_3 films about 2 orders and the Dit as low as 8.72×10^{10} $cm^{-2}eV^{-1}$. Substrate temperature above 400℃ or O_2 partial pressure of 20 %, the monoclinic Y_2O_3 film structure was disappeared and the cubic Y_2O_3 phase was dominated in XRD spectra. And we achieved low lattice mismatch of 1.75 %. We conclude that Y_2O_3 buffer layer for a single transistor FRAM should be grown at 400℃ then RTA treatment at 900℃.

ACKNOWDGEMENT

This work was supported by Institute of Information Technology Assessment. Authors recognize IITA for the valuable financial support on this work.

REFERENCE

[1] S. Imada, S. Shourki, E. Tokumitsu, and H. Ishiwara, Epitaxial Growth of Ferroelecltric $YMnO_3$ Thin Films on Si (111) Substrates by Molecular Beam Epitaxy , Jpn. J. Appl. Phys., Vol 37, pp6497-6501, 1998.

[2] Y. M. Wu and J. T. Lo, Growth of $PbTiO_3$ Thin Film on Si (100) with Y_2O_3 and CeO_2 Buffer Layer , Jpn. J. Appl. Phys., Vol. 37, pp.4943-4948, 1998.

[3] S. Zhang and R Xiao, Yttrium Oxide Films Prepared by Pulsed Laser Deposition , J. Appl. Phys., Vol. 83, No. 7, pp. 3842-3848, 1998.

[4] M. H. Cho, D. H. Ko, K. Jeong, S. W. Whangbo and C. N. Whang, S. C. Choi, and S. J. Cho, Structure Transition of Crystalline Y_2O_3 Film on Si(111) with Substrate Temperature , Thin Solid Films, Vol. 349, pp. 266-269, 1999

[5] M. Y. Grytsiv, V. D. Bondar, and S. I. Chykhrii, Structure of Yttria Thin Films Prepared by Reactive RF Diode Sputtering , Inorganic Materials, Vol. 32, No. 11, pp. 1202-1204, 1996.

[6] S. M. Cho and D. Y. Jeon, Effect of Annealing Conditions on the Leakage Current Characteristics of Ferroelectric PZT Thin Films Grown by Sol-gel Process , Thin Solid Films, Vol. 338, pp.149-154, 1999.

[7] K. Watanabe, A. J. Hartmann, R. N. Lamb, and J. F. Scott, Electronic Characteristic of the $SrBi_2TaO_2$-Pt Junction, J. Appl. Phys., Vol. 84, No. 4, 1998.