셀손실 우선순위 기반의 사용 변수제어의 VLSI구현

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The VLSI Implementation of A Usage Parameter Control based on Cell Loss Priority

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요 약

In this paper, we propose an enhanced usage parameter control algorithm, which is one of the preventive traffic control method in ATM networks and implemented it with VLSI. Proposed algorithm is based on the cell loss priority bit in the ATM cell header. This algorithm can solve the measurement phasing problem in cell conformance testing in ATM networks. Proposed algorithm can minimize the cell loss ratio of high priority cell(CLP = 0) and resolve the burstiness of cells which may be introduced in traffic multiplexing and demultiplexing procedure. The result of performance evaluation shows that the performance of proposed algorithm is better than that of ITU-T usage parameter control algorithm.

1. 서론

To protect an ATM against a malicious user or faulty equipment, the established conn ection has to be monitored. Thus a policing function(in CCITT referred to as Usage Parameter Control) is needed to verify that the transmitted cells do not violate the negotiated traffic contract. Its base algorithm is VSA(Virtual Scheduling Algorithm). A single counter can count upto 65535. If we have the counter reaches its limit.

2. General View

The component supports single User Parameter Control (UPC) on 4 independent UPTOPIA compatible unidirectional links. Links can be operated up to 155Mb/s and load can be as high as 100%. Per link the full range of maximum 64k different connections may be checked for fulfillment of the traffic contract. The result is translated into either pass or discard or tagging of the cell. The component uses a single external dynamic memory which can be optimized in its size depending on the real need of number of connections to be monitored.

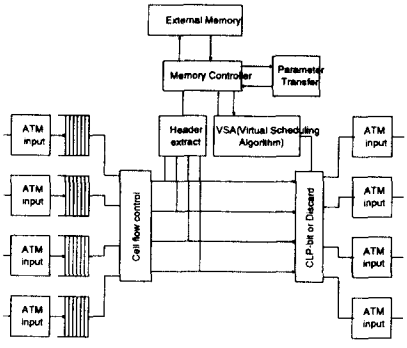

Fig 1. The block diagram of UPC

In addition to UPC an all purpose counter per connection can be triggered by events like passed, discarded or tagged cells. A special counter only mode allows for settings of peak cell rate, cell delay variation, sustainable cell rate and maximum burst size.

3. Module of VSA

An important factor is the minimum rate which can be set. Although a minimum rate of 16Kbits/sec was specified to be sufficient for most application the algorithm has been extended to allow much lower rates as well. The granualarity specifies how accurate a demand for a certain link rate can be met.

header extraction

In both modes the device selects the UPC parameters using up to 16 bits from the header which are extracted by means of a 16 bits. The device allows any bit of the header to be used. In direct mode the device supports 64K VSA(Virtual Scheduling Algorithm) per link. From the header up to 16 bits are extracted. Besides the parameter storage for each link the system uses a 64K lookup table additionally.

Fig 2. the architecture of VSA

4. Number of handled connection

The number of handl ed connections which are supported by the devices depends on the operations on the operation mode. In direct mode the device supports 64k connections for each link giving a total of 256K connections. In table lookup mode the device supports a total of 64K connections.

5. Mode Selection

The device works either in direct or table lookup mode. In both modes the device selects the UPC parameters using up to 8 bits from the header which are extracted by means of a bit mask. The device allows any bit of table lookup mode

6. ATM ports

For the UPC device a clock of 50Mhz must be provided. The clock is used for the VSA and the memory controller.

7. Input ports

The input port of the device is the coupled through a four cell FIFO. The FIFO is used for clock the coupling only and not for rate adaptation.

The start of a cell is marked with the so called cell sync signal which is active during the arrival of the first byte of a cell. As soon as the first byte has entered the device the following 52 bytes are ass umed to belong to the same cell and are stored accordingly.

If during the loading of these 52 bytes another cell sync arrives this signal is ignored. The event is registered in the input status register and can provide and interrupt, signaling that an earl y sync as been detected.

The input port can also notice if there is no cell sync immediately following the last loaded cell byte (late sync detection). Thins is an error when a continuous cell stream should be present. This event can also be registered in the input status register and can also provide an interrupt signal. Systems working with a discontinuous cell stream should simply ignore this status bit.

The device has two registers which reflect the status of the input ports. From each input the following events can be noticed.

Early cell sync, late cell sync, FiFO overflow, missing byte clock.

A FIFO overflow occurs when the input clock is larger than the output clock. The device will discard all arriving cells when the FIFO is full and sets the FIFO full bit.

The input status bits will remain set until cleared by a write from the μprocessor. Clearing a status bit is done by writing a one

Both devices can use up to 16 bits from the cell header. The header bits are selected using four 8 bit header mask registers. Each bit set in a register will cause the corresponding header bit to be used for selecting a bucket. If less then 8 bits are set in the mask, the remaining extracted bits are set to zero. If more then 8 bits are set only the last 8 bits are used.

8. Header extraction

The device uses the VSA to enforce a specified data rate. The parameters will always allow the following features.

In link rate, the only important factor with the link rate is the minimum rate which can be set. Although a mini mum rate of 16Kbits/sec was specified to be sufficient for most application the algorithm has been extended to allow much lower rates as well.

The granularity specifies how accurate a demand for a certain link rate can be met. It also causes the loss of b andwidth as each request must be rounded upwards to the nearest higher rate. This does not mean a loss of 0.778% of the total bandwidth for each connection. It means 0.78% deviation of the requested bandwidth.

9. Parameter settings

The device has a 16 bit counter per channel. The counter can be programmed using decision table which will be explained later. Counting values up to 2^{41}. With a single channel continuous running at 155Mbits/sec it will take about 69 days before the counter reaches it' s maximum value.

10. Conclusion

In this paper, we discussed the coding size for four parameters i.e. TAT, T, τ, and E that are used by VSA and showed that the ATM Peak Cell Rate Granularity supported by the device is relatively accurate. We also described the archit ecture of the device for the implementation of VSA and discussed some issue on the implementation. We exploited the priority encoder to run the algorithm in parallel instead of sequentially, which reduced the operation time to a great extent.

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