2000년도 대한전기학회 하계학술대회 논문집 2000.7.17-20

영전압, 영전류 스위칭 1단 방식 역률 보상 AC/DC 컨버터

강필순, 박성준, 권순재, 김철우
부산대학교, 동명대학, 부경대학교

ZVZCS Single-Stage Power Factor Corrected Converter

Feel-Soon Kang*, Sung-Jun Park**, Soon-Jae Kwon***, Cheul-U Kim*
Pusan National University*, Dong-myong College**, Pukyung National University***

Abstract - Zero-voltage and zero-current switched single-stage approach with high power factor is presented to reduce the switching losses and to achieve sinusoidal, unity power factor input currents. This single-stage approach, which combines a boost converter used as PFC with a half-bridge converter used as dc to dc conversion into one power stage, has a simple structure and low cost. At the same time, since the switches of the proposed converter are designed to be turned on at zero-voltage and off at zero-current, the switching losses could be reduced considerably. Detailed analysis and experimental results are presented on the proposed converter, which is operated at constant switching frequency and in discontinuous conduction mode.

1. Introduction

In the ac to dc converter employing power factor corrected circuit, a traditional two-stage converter is composed of two power conversion stages. Unfortunately, this method has several disadvantages. Such as high cost, complexity in composition and a drop in efficiency due to the double power conversion, and other problems [1][2].

In recent years, to solve these problems, many single-stage power factor corrected converters, which integrate a power factor correction circuitry and a dc to dc converter into one power stage, have been suggested to achieve both power factor correction and power conversion from the ac line to a desired dc output[3][4].

In this paper, a novel zero voltage and zero current switched single-stage PFC scheme with low cost is presented. The advantages of the proposed converter are summarized by three important factors, i.e., the high power factor, the improved efficiency and low cost.

2. The proposed soft-switched single-stage PFC converter

2.1 The proposed converter

The proposed converter is shown in Fig. 1. Thanks to integrate the input boost converter and the output half-bridge converter into one power stage, one diode and one switch could be eliminated. In the size of an overall system, the reduced one could be achieved with a simplified structure.

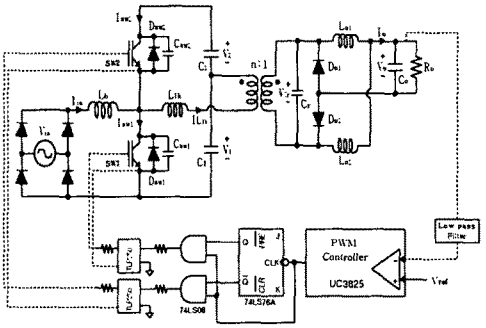

Fig. 1 The proposed converter

To achieve a unity power factor, the input current must be maintained to the input voltage proportionally[5].

In this proposed power factor corrected converter, since the input currents are designed to operate in discontinuous conduction mode, the input current will follow the input voltage without sensing of the input current from AC line. Thus, the additional input current controller is not necessary, i.e. "cost saving" is possible. And also, due to the input current in DCM, ZVS is automatically possible without auxiliary circuits and ZCS is obtained by using the resonance between the leakage inductance and substantial external snubber capacitors.

As a result, the switching loss could be significantly reduced. From these facts, this proposed converter could be manufactured with high power factor, improved efficiency and a simple structure with low cost.

2.2 Operational principle

To explain how the proposed converter works, a half of input cycle is divided into six modes and every mode is explained separately. Key waveforms according to switching signals and input inductor current are shown in Fig. 2 of the next page.

The circuit in each mode is illustrated in Fig. 3 through Fig. 8, and then discussed in depth.

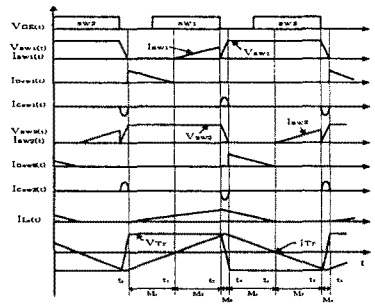

Fig. 2 Key waveforms

Mode 1 [$t_0 < t \leq t_1$]

At the beginning of this mode, t_0, the current through the input inductor, L_b, is null and the voltage across C_{sw1} is null. D_{sw1} is conducting. The input current, I_{in}, will flow through resonant inductor, L_{lk}, can either be a separate inductor or the leakage inductance of the transformer, bulk capacitor, C_1, charging it in a resonant way, and the body diode of switch Sw_1. $I_{L_a}(t)$ is linearly increased and can be expressed as

$$V_{C_{sw1}}(t) = 0 \tag{1}$$

$$I_{L_a}(t) = I_{D_{sw1}}(t) = \frac{V_1 - nV_{Cr}}{L_{lk}}(t - t_0) \tag{2}$$

Also the input current is linearly increased following the equation (3).

$$I_{in}(t) = \frac{V_{in} + nV_{Cr} - V_1}{L}(t - t_0) \tag{3}$$

Where $L = L_b + L_{lk}$

During this mode, the controller will apply a gate signal to the drive circuit of Sw_1; nevertheless, D_{sw1} is still conducting until $I_{L_a}(t)$ becomes zero.

Mode 2 [$t_1 < t \leq t_2$]

At instant, t_1, since capacitor, C_1, resonates with leakage inductance, L_{lk}, the current, I_{L_a}, reverses its direction. As a result, the anti-parallel diode of Sw_1 is reverse-biased, and then the input current will flow through Sw_1. This current, I_{sw1}, can be expressed as the following equation.

$$I_{sw1}(t) = (I_{in} + I_{L_a})(t - t_1) \tag{4}$$

In this mode, $I_{in}(t)$ is still linearly increased and expressed as

$$I_{in}(t) = \frac{V_{in}}{L_b}[(t - t_1) + (t - t_0)] \tag{5}$$

In the secondary of the transformer, because the direction of the primary current is reversed, the diode D_{o1} is turned on and D_{o2} is turned off.

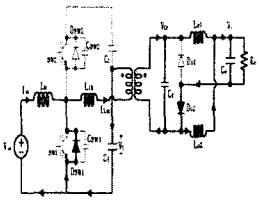

Fig. 3 Mode 1

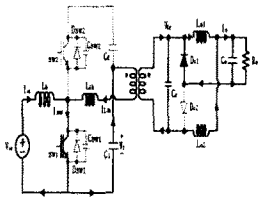

Fig. 4 Mode 2

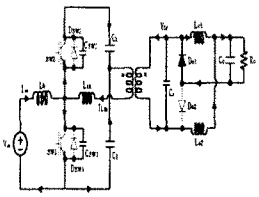

Fig. 5 Mode 3

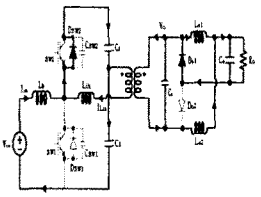

Fig. 6 Mode 4

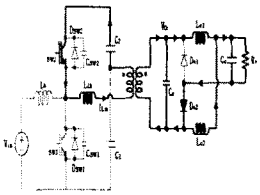

Fig. 7 Mode 5

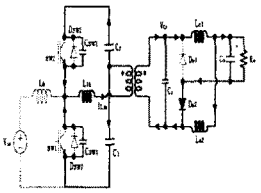

Fig. 8 Mode 6

Mode 3 [$t_2 < t \leq t_3$]

At $t = t_2$, switch, Sw_1 is turned off. During this mode, capacitor C_{sw_1} is being charged in resonant manner, and external capacitor C_{sw_2} is being discharged. In this stage, the input current, I_{in}, starts to decrease. Thanks to the low impedance path through capacitor C_{sw_1} and C_{sw_2}, Sw_1 can be switched off at zero-current.

Mode 4 [$t_3 < t \leq t_4$]

At $t = t_3$, when the capacitor voltage across C_{sw_2} becomes zero, the anti-parallel diode, D_{sw_2}, of Sw_2 is turned on. In this mode, C_2 continues to resonate with leakage inductance, L_{lk}, such as mode 1.

Mode 5 [$t_4 < t \leq t_5$]

At $t = t_4$, as capacitor, C_2, resonates with leakage inductance, L_{lk}, the current, I_{L_a}, inverts its direction. As a result, the anti-parallel diode, D_{sw_2}, of Sw_2 is turned off

and Sw_2 conducts. Until this mode is terminated, the input current, I_{in}, must be zero in order to ensure zero voltage switching. If the input current, I_{in}, flows until this mode, the ZVS is impossible at the next switching time.

Mode 6 [$t_5 < t \leq t_6$]

At $t = t_5$, Sw_2 is turned off. During this mode, capacitor, C_{Sw_2}, is being charged in resonant manner, and C_{Sw_1} is being discharged. This mode terminates at $t = t_6$, when voltage across capacitor, C_{Sw_1}, becomes zero. In this stage, the input current, I_{in}, is completely zero.

2.3 Simulated and Experimental Results

In order to verify the theoretical analysis and the principle of operation of the proposed converter, a 280[W] single-stage PFC converter has been manufactured and experimentalized in the laboratory, using IGBT modules as a switching device.

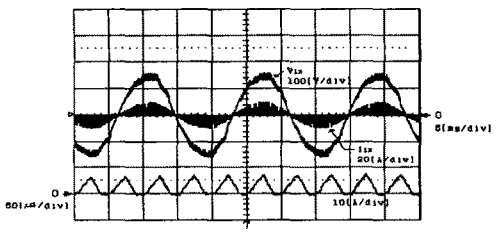

Fig. 9 Input voltage & current

Fig. 9 is experimental waveforms of line voltage, input inductor current. It can be seen that near unity power factor is satisfactorily achieved without any additional input current controllers. These figure show that the envelope of the boost inductor current follows the input line voltage waveform, illustrating a near sinusoidal waveform, and flows with no phase difference to line voltage.

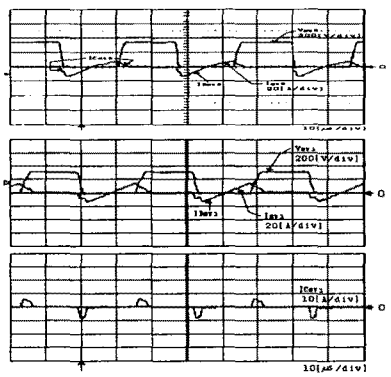

Fig. 10 Voltage & current(switch)

The experimental waveforms for the collect-to-emitter voltage of the switches Sw_1 and Sw_2 with their current are shown in Fig. 10. Fig. 11 shows the graphs of the measured power factor and the FFT results of the input current. The measured power factor is above 0.95 and the efficiency of the proposed converter can be achieved around 86% at the rated condition, i.e. $V_{in} = 100[V_{ac}]$, $P_o = 280[W]$. Fig.11 shows that the proposed converter successfully meets IEC1000-3-2 class-D limits.

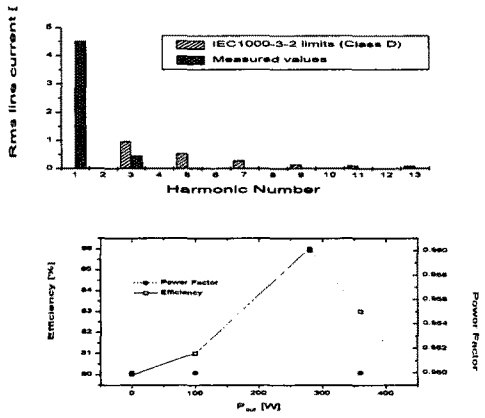

Fig. 11 class D limits/power factor/efficiency

3. Conclusion

In this paper, a novel soft-switched single-stage PFC converter was proposed, and each operation mode was analyzed in depth. From the experimental results, the proposed power factor corrected converter, which has a simple composition and low cost, gives higher power factor, lower harmonic distortion, improved efficiency and lower switching losses. The prototype successfully meets the IEC 1000-3-2 class-D requirements.

In the experiments, the power factor was above 0.95 and the efficiency was about 86% at $V_{in} = 100[V]$ and $P_o = 280[W]$

(reference)

[1]D. M. Divan, G. Venkataramanan, and C. Chen, "A Unity Power Factor Forward Converter", IEEE IAS, pp.666-672, 1992.

[2]M. van der Berg, J. A. Ferreira, "A Family of low EMI, Unity Power Factor Converters", IEEE PESC, vol. II, 1996.

[3]F. S. Kang, S. H. Lee, S. J. Park, C. U. Kim, "A Novel Soft-Switched Single-stage PFC AC to DC Two-Switches Forward Converter," ICMT'99, pp.49-53, Oct. 1999.

[4]A. F. Souza and I. Barbi, "A new ZVS-PWM unity power factor rectifier with reduced conduction losses", IEEE Trans. Power Electron., vol. 10, pp.746-752, 1995.

[5]E. S. Kim and K. Y. Cho, "An improved soft switching PWM FB dc/dc converter for reducing conduction loss", IEEE PESC, pp.651-657, 1996.