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두 단계 열처리 방법으로 결정화된 새로운 구조의 다결정 실리콘 박막 트랜지스터의 제작

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Fabrication of the Two-Step Crystallized Polycrystalline Silicon Thin Film Transistors with the Novel Device Structure

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Abstract - We have fabricated poly-Si TFTs by two-step crystallizaton. Poly-Si films have been prepared by furnace annealing(FA) and rapid thermal annealing(RTA) followed by sebsequent the post-annealing, excimer laser annealing. The measured crystallinity of RTA and FA annealed poly-Si film is 77% and 68.5%,respectively. For two-step annealed poly-Si film, the crystallinity has been drastically to 87.7% and 86.3%. The RMS surface roughness from AFM results have been improved from 56.3Å to 33.5Å after post annealing. The measured transfer characteristics of the two-step annealed poly-Si TFTs have been improved significantly for the both FA-ELA and RTA-ELA. Leakage currents of two-step annealed poly-Si TFTs are lower than that of the devices by FA and RTA. From these results, we can describe the fact that the intra-grain defects has been cured drastically by the post-annealing.

1. Introduction

Polycrystalline silicon has received increasing attention because of its wide range of applicability in large area of electronics, such as thin film transistor, solar cell and image sensor. Especially polycrystalline silicon thin film transistor(poly-Si TFTs) is act as pixel switching elements and as driving elements in active matrix liquid crystal display(AMLCDs). Poly-Si TFTs is superior to amorphous silicon TFTs (a-Si TFTs) in achieving high carrier mobility and fast response time. However, one of the serious fatal problem is the larger leakage current compared with that of a-Si TFTs. additionally, the trap-assisted field emission and thermionic field emission in the depletion region near the drain electrode are regarded as the most reasonable mechanism of the poly-Si TFTs

In poly-Si TFTs, grain boundaries and intra-grain defects exert a profound on the characteristics of poly-Si TFTs and degrade carrier transport. In other words, the characteristics of poly-Si TFTs are strongly influenced by the properties of active layer. therefore, the poly-Si film with large grain and lightly intra-grain defects is needed for improvement of electrical characteristics. In this work we are evaluate the effects of the two-step annealing method on the grain structure and electrical characteristics of poly-Si film and poly-Si TFTs. two-step annealing was reduced significantly the intra-grain defects of the furnace annealed poly-Si films while maintaining the large grain and grain structure.

2. Device Fabrication

1000Å-thick amorphous silicon films deposited on 5000Å oxidized Si wafer by LPCVD. Deposition conditions are 0.3 Torr of operating pressure, 60sccm of SiH_4 flow rate. The films were annealed in the different method. One group was crystallized by conventional furnace annealing at 600 °C for 24h in N_2 ambient and followed by subsequent XeCl excimer laser annealing(FA-ELA). The other group was crystallized by rapid thermal annealing at 850 °C for 1 min in N_2 ambient, and followed by the same method(RTA-ELA). XeCl excimer laser operating at a wavelength of 308nm with full width at half maximum pulse of 35ns used for the recrystallization process (two-step annealing). An optical homogenizer was used to transform the incident bi-Gaussian beam into a 0.6×0.6mm flattop profile with ± 5% energy variation. The samples are irradiated with one shot, where the energy density was varied from 400mJ/cm^2 to 470mJ/cm^2 with 98% overlap in N2 ambient. Amorphous Si was also subjected only to FA or RTA for comparison.

In order to characterize the structure properties of the annealed poly-Si films, UV reflectance spectrum method, atomic force measurement(AFM), field emission scanning electron micrograph(FE-SEM) and transmission electron micrograph(TEM) have been investigated.

Poly-Si patterning was defined by the photolithography process in a reactive ion-etching(RIE) reactor with chlorine as the etchant gas. After definition of silicon islands, the gate dielectric layer, which thickness varies from 1000Å to 3000Å, is deposited by PECVD of Tetra-Ethyl-Oxysilicate(TEOS) source gas at 390 °C. The gate dielectric layer was patterned by RIE to form the step-like structure and this structure can act as the offset mask. The

thickness of gate dielectric layer beyond the desired offset region was varied from 1000Å to 2000Å. Since the doping concentration can be controlled by the thickness of gate dielectric film, the offset region can be defined beneath the thick gate oxide layer during doping process. After definition of gate dielectric layer, the poly-Si is deposited by LPCVD as the gate electrode. The poly-Si gate, which is deposited in the amorphous phase using SiH_4 as a reactant gas at 550° C and crystallized by the RTA at 850° C. Then, heavily doped electrodes are defined by phosphorus ion implantation. In this electrode definition, the offset region is also formed by self-aligned process. The n^+ ion implantation is performed by implanting $5\times10^{15}/cm^2$ of phosphorus at 45keV. 5000Å-thick interlayer oxide film is deposited by PECVD using TEOS, and contact holes are opened and 10000Å-thick Al(with 1% Si) film was deposited by sputter. The devices are then sintered at 450 °C for 30min in N_2 ambient. The cross-section view of the poly-Si TFTs are shown in Fig.1

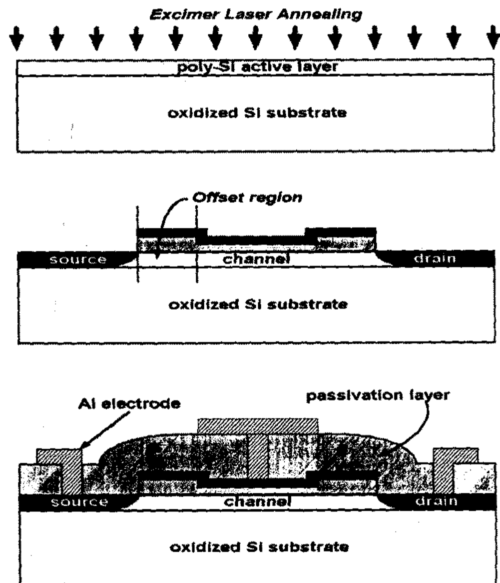
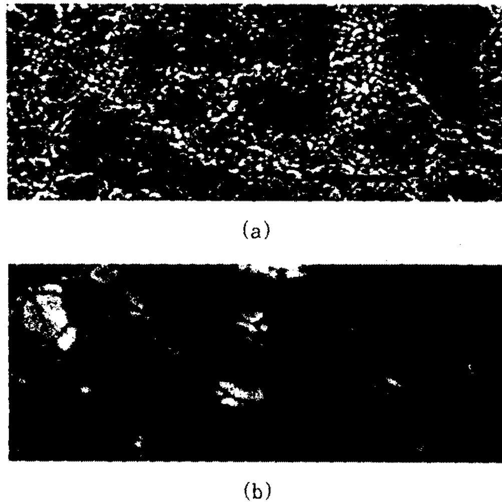


Fig. 1 The cross-sectional process flow of the SLD offset poly-Si TFTs

3. Results and Discussion

Fig.2 shows the FE-SEM image of FA poly-Si film annealed at 600° C for 24hr, and the two-step annealed poly-Si film by ELA. As shown in Fig. 2, pre-annealing poly-Si film has intra-grain defect heavily, while for the two-step annealed poly-Si film, intra-grain defects inside the grains are considerably removed comparable with those FA poly-Si film. For the FA and two-step annealed poly-Si film, the average grain size is about 2100Å and 2000Å, respectively.

The relationship between the crystallinity and the laser energy density bas been investigated by the UV reflectance spectrum and TEM, Fig. 3. Fig. 4 is the measured surface crystallinity by UV reflectance spectrum and transmission electron diffraction(TED) patterns.



(a)

(b)

Fig. 2. FE-SEM images for pre-annealed poly-Si film and two-step annealed poly-Si film with excimer laser annealing at 470mJ/cm^2

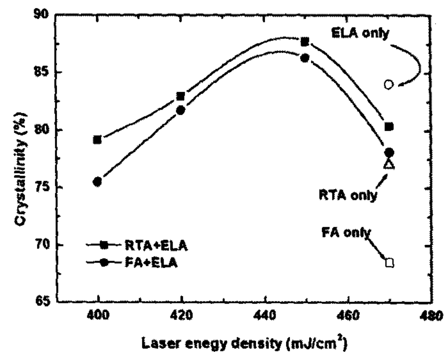


Fig. 3 The crystallinity as a function of laser energy density and annealing technique, such as RTA-ELA, FA-ELA, RTA only, FA only, and ELA only.

The crystallinity of the two-step annealed poly-Si film improves compared to the one-step annealed poly-Si film as shown in Fig. 3, especially the annealing technique effect on crystallinity remarkably in FA-ELA case. It can be explained by the fact that the post-annealing reduced the intra-grain defects significantly during melting the film as can be seen the FE-SEM image in Fig. 2. But, the crystallinity behavior of the poly-Si film above 450mJ/cm^2 is a little different compared to the regime. For energy fluence above 450 mJ/cm^2, we have found that the surface roughness of

the film increase due to surface damage produced by high laser energy. It can be explained by the fact that surface damage makes the UV light scattering, thus the measured crystallinity may decrease in this regime. From AFM experimental, we could observe the fact that the surface roughness for RTA-ELA at 450mJ/cm^2 and 470mJ/cm^2 is 32.5 Å and 38.2Å respectively. However, we found that the crystallinity behavior from TED patterns is different than that from UV reflectance as shown in Fig. 4. The crystallinity behavior also has been improved in high-energy regime at 470mJ/cm^2. Thus, as the laser energy is increased, the crystallinity behavior also is getting better and better for both FA-ELA and RTA-ELA case. As the above structural properties, we have chosen the energy density of the 470mJ/cm^2 as optimal annealing condition.

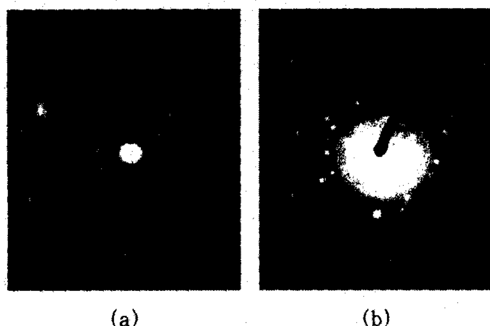


Fig.4 TED pattern image of RTA-ELA poly-Si film at 450mJ/cm^2 (a) and 470mJ/cm^2 (b).

We have investigated electrical characteristics of the fabricated SLD offset poly-Si TFTs. Also, we have simulated the characteristics using 2-D device simulator (SILVACO®ATLAS). The measured transfer characteristics of the proposed SLD offset poly-Si TFTs at V_D=5V and V_D=10V are shown in Fig. 5 and Fig. 6, respectively.

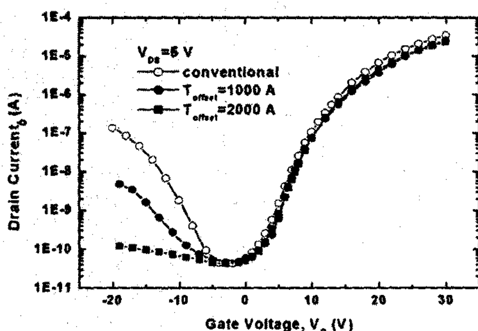


Fig. 5. The transfer characteristics of the proposed SLD offset poly-Si TFTs at V_D=5V.

The leakage current of the novel TFTs is lower by the magnitude of three orders than of conventional non-offset devices at V_G = -20 V while the ON state current are almost same compared to conventional TFTs. This lower leakage current of the novel TFT than that of conventional devices may be due to the more effective suppression of carrier emission via trap states, which is mainly caused by the remarkable reduction of lateral and vertical electric field as can be observed in Figure 7. On the other hand, the ON state current of the proposed SLD offset devices is more significantly improved than that of conventional offset TFT because the series resistance is decreased considerably by the additionally induced electrons in the offset region.

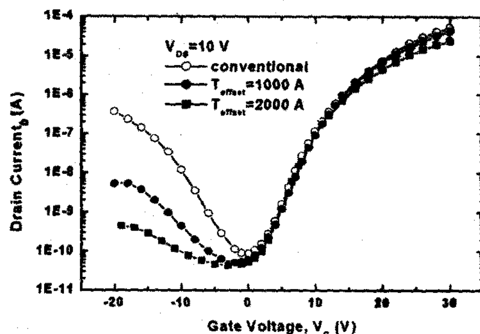


Fig. 6. The transfer characteristics of the proposed SLD offset poly-Si TFTs at V_D=10V.

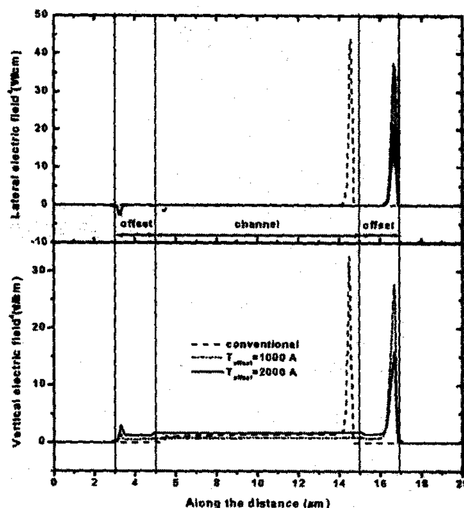


Fig. 7 Lateral and vertical electric fields strength as the function of T_{offset} thickness at OFF state(V_G=-20V, V_D=10V)

Fig. 8 is the simulated electron concentration of the proposed devices under ON and OFF states. It can be explained by the fact that

electrons can be induced by the positive bias of the extended gate electrode over the offset region. Owing to the decrease of series resistance by the remarkable increase of electron density in the offset region, the ON state current of the proposed device may be increased significantly with that of conventional devices. We have summarized the measured device parameters of the proposed SLD offset poly-Si TFTs and conventional devices in Table I.

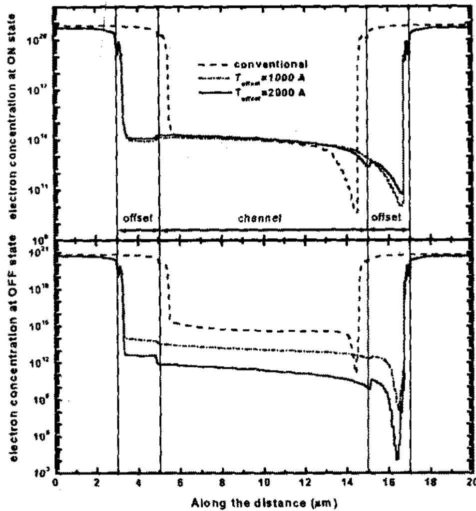


Fig. 8 The electron concentration along the channel at the ON state(V_G=30V, V_D=10V, top figure) and OFF state(V_G=-20V, V_D=10V, bottom figure)

Table. 1 Summary of device parameter of the proposed SLD offset poly-Si TFT and conventional structure device

V_D	Offset length	V_{th}(V)	I_{ON} (10^{-5})	I_{OFF} (10^{-9})	I_{min} (10^{-11})	$I_{ON/OFF}$ (10^4)
5V	0Å	7.12	3.44	135.2	4.22	0.25
	1000Å	7.47	2.46	4.74	4.62	5.19
	2000Å	7.64	2.34	0.12	4.16	19.18
10V	0Å	6.91	5.31	362.4	8.97	0.15
	1000Å	7.13	4.21	5.31	5.13	7.93
	2000Å	7.36	2.41	0.43	4.28	5.55

4. Conclusion

We have proposed the novel device structure, which is called step-like-drain (SLD) offset poly-Si TFTs. The proposed poly-Si TFT has the novel gate insulator structure, which makes the offset region and the additional extended gate electrodes. These gate electrodes could control the conductance of this offset region. The active layers of proposed device have been crystallized by two-step annealing with 470 mJ/cm^2 energy density.

In the measured transfer characteristics of the proposed SLD offset poly-Si TFTs, the leakage current of the novel TFTs is lower by the magnitude of three orders than of conventional non-offset devices at V_G=-20V while the ON state current are almost same compared to conventional TFTs. This lower leakage current of the novel TFT than that of conventional devices may be due to the more effective suppression of carrier emission via trap states, which is mainly caused by the remarkable reduction of lateral and vertical electric field. As results, the proposed devices are applicable for large area AMLCD by employing the offset drain region with additional gate region.

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