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Accurate CMOS-based square root extractor

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Abstract

In this article, an integrable circuit technique for implementing square root extractor for analog signal processing is described. The realization method makes use of the characteristic of MOS translinear principle. The proposed scheme achieves a wide dynamic range, wide-band capability and high accuracy. Simulation results demonstrating the performance of the proposed scheme are also presented.

1. Introduction

A square root extractor is a useful circuit building block used in analog measurement and instrumentation. For example, it can be used to linearize a signal from a differential pressure flow meter or to calculate the RMS value of an arbitrary waveform [1]. In the past, one fundamental approach to realize a square-root function is based on the use of an operational amplifier (op-amp) together with a bipolar transistor to form a log and anti-log amplifier [2]. This approach provides the logarithmic principle to realize a square root function. Another approach is based on the use of op-amps, analog switches and resistor-capacitor time constant. However, the frequency performance achieved by these approaches is limited by the narrow bandwidth of an op-amp topology. Alternatively, an approach based on the characteristic of the translinear configuration of bipolar junction transistors, which is suitable for implementing in monolithic integrated circuit form, has been shown to realize a square root function [3]. The advantage of this technique is a wide bandwidth due to the circuit operating in current mode. In addition, two approaches have been reported on the realization of a square root function using MOS transistors. The first approach is based on the use of weak inverted MOS transistors [4]. This approach obtains low power consumption and low voltage operation. In contrast, the accuracy and the frequency performance are limited by the small transconductance value of the weak inverted MOS transistors restriction [5]. The second approach is based on the use of the second generation current conveyor (CCII) connected with non-saturated MOS transistors and op-amp [6]. The high-frequency limitation of this approach is due to the finite gain bandwidth product of the op-amp and parasitic capacitances of the non-saturated MOS transistors. The purpose of this article is to propose a CMOS integrated circuit technique for the realization of an accurate square root extractor. The resulting performances of the square root extractor have wide bandwidth and high accuracy.

2. Circuit description

The proposed CMOS-based square root extractor is shown in figure 1. Assuming that all transistors are well matched and operate in their saturation regions. The operation of the circuit can be explained as follow. The unity gain current mirror formed by M_3 and M_4 forces equal current in the transistors M_1 and M_2. This operation drives the gate-source voltages of the transistors M_1 and M_2 to equal, $V_{GS1} = V_{GS2}$, and consequently, forces the voltage at node A to follow the input voltage v_{in} with the voltage gain equal 1 [7]. Then the signal current i_{in} can be stated as

$$i_{in} = \frac{v_{in} - V_{GS1} + V_{GS2}}{R} = \frac{v_{in}}{R} \qquad (1)$$

Where R is a given resistance connected at node A. The resistor R converts the input signal voltage to the signal current i_{in}, and the transistor M_5 formed as a current follower transfers the signal current i_{in} to unity gain current mirror M_6 - M_7. The current mirror M_8 - M_{10} provides only positive current to flow through it to limit the negative current. The unity gain current mirrors M_8 - M_9 and M_{11} - M_{12} force the signal current i_{in} to the transistor M_{14} and the current source I_4 provides the bias current of transistor M_{15}. When the signal current i_{in} is applied to the transistor M_{14}, then the relationship of the drain current of the transistors M_{14} and M_{16}, I_{D14} and I_{D16}, respectively, and the signal current i_{in}, can be expressed as

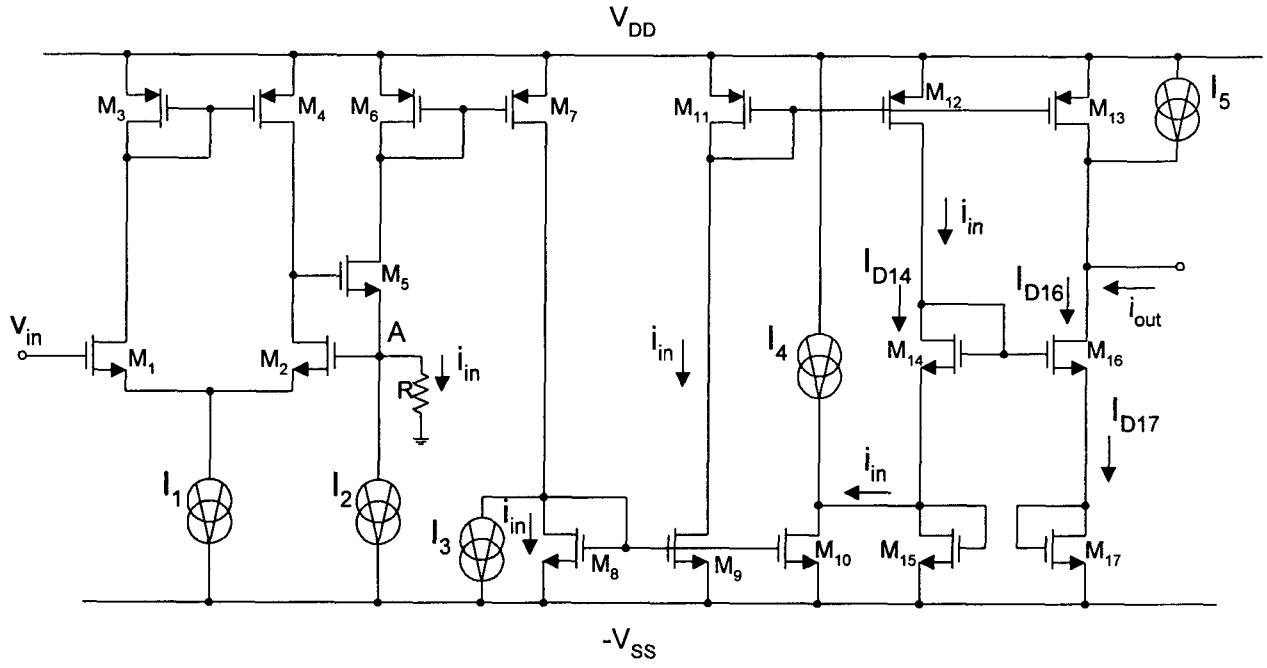

Figure 1. The proposed circuit

$$I_{D16} = \frac{i_{in}}{4} + \frac{\sqrt{I_4}\sqrt{i_{in}}}{2} + \frac{I_4}{4} \qquad (2)$$

Where I_{Di} is the drain current of the transistor M_i. The current mirror formed by M_{11} and M_{13}, which has current gain equal to 1/4, forces the current $i_{in}/4$ into an output node, and the current source $I_5 = I_4/4$ provides an elimination of the output current offset. Then the output current i_{out} becomes

$$i_{out} = \frac{\sqrt{I_4}\sqrt{i_{in}}}{2} = \sqrt{\frac{I_4}{4R}}\sqrt{v_{in}} \quad ; v_{in} > 0$$
$$= K\sqrt{v_{in}} \qquad (3)$$

where $K = (I_4/4R)^{1/2}$. From Eq. (3), it is evident that the output current i_{out} is a square root of the input signal voltage v_{in}, with the transconductance gain equal to $(I_4 / 4R)^{1/2}$

3. Simulation results

The performance of the proposed circuit in figure 1 was observed using the PSPICE analogue simulation program. The MOSIS 2.0μm CMOS process parameters were used for the circuit simulation. The ratio of channel widths and lengths (W/L) of the devices used are shown in table 1. The bias currents $I_1 = I_2 = I_3$, I_4 and I_5 are set to 300μA, 100μA and 25μA, respectively, $V_{DD} = V_{SS} = 5V$. and R = 100kΩ. Figure 2 shows the simulated DC transfer characteristic for the input signal voltage v_{in}, which is varied from 0V to 10V. Figure 3 shows the transient response of the output current waveform for 10kHz triangular wave input waveform of peak amplitude 10V. The high frequency performance of the proposed scheme is shown in figure 4. It should be noted that the bandwidth about 100MHz is observed.

Transistors	W/L
M1-M4, M6-M12	20μm/2μm
M5	100μm /2μm
M13	5μm /2μm
M14-M17	10μm /2μm

Table 1 the ratio of channel widths and lengths of the MOS transistors

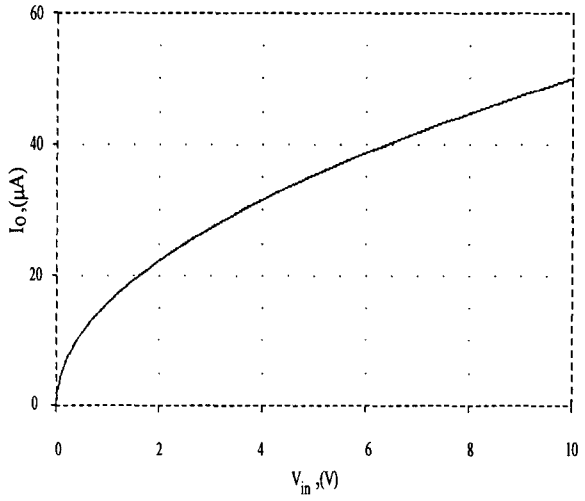

Figure 2. DC transfer characteristic

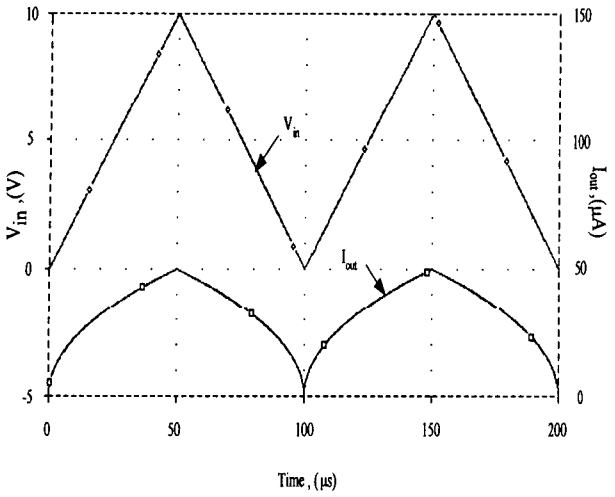

Figure 3. Simulated transient response for 10kHz triangular wave input waveform

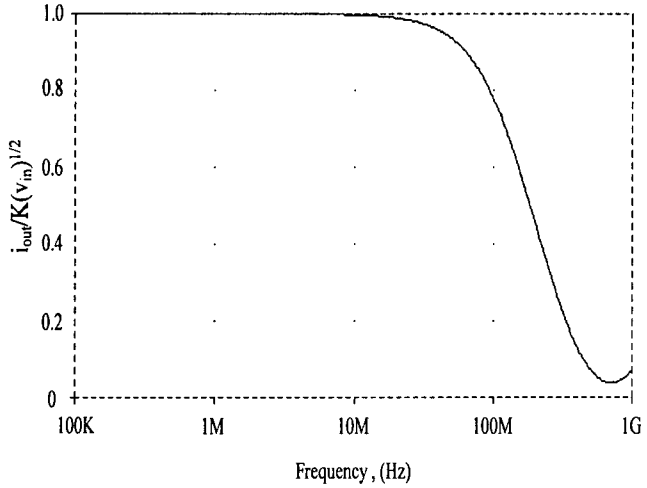

Figure 4. Frequency response of the proposed scheme

4. Conclusion

In this article, an alternative scheme suitable for fabrication using CMOS technology for the realization of a square root extractor has been presented. The simulation results have shown that the circuit performance is highly accurate and has wide-band capability.

5. Acknowledgments

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