Integrated 3-D Microstructures for RF Applications
(Invited)

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Abstract

In this paper we report new integration technology developed for three-dimensional metallic microstructures in an arbitrary shape. We have developed the two fabrication methods: Multi-Exposure and Single-Development (MESD) and Sacrificial Metallic Mold (SMM) techniques. Three-dimensional photoresist mold can be formed by the MESD method while unlimited number of structural levels can be realized by the SMM technique. Using these two techniques we have fabricated solenoid inductors and levitated spiral inductors for RF applications. We have achieved peak Q-factors over 40 in the 2-10GHz range, the highest number among the inductors reported to date. Finally, we propose "On-Chip Passives" as a post IC process for monolithic integration of inductors, tunable capacitors, microwave switches, transmission lines, and mixers and filters toward future single-chip transceiver integration.

I. Introduction

A completely-integrated transceiver-on-a-chip has been one of the ultimate goals in wireless communications for low cost, small size, and low power consumption. However, RF passive components (hereafter, passives) have been blocking the path since monolithic RF passives usually require large area and show poor device performance such as low quality-factors (Q's). They usually have been implemented as expensive, off-chip components. To overcome this problem, we have proposed a new concept, "On-Circuit Passives" (OCP). In this integrated microchip, inductors, capacitors, and other RF passives are implemented over an RF circuit as a levitated structure to eliminate area requirement for passives and parasitic effects related to the substrate. A simple post-IC micromachining technique has been utilized to realize the OCP concept. The OCP concept and the fabrication process will be discussed in detail. We have focused especially on the monolithic inductor technology in this work, while other RF passives on a circuit have been briefly addressed as well.

II. High-Aspect-Ratio Photolithography

Recently, miniaturization of electrical and mechanical devices in three-dimensional macro worlds has been of particular importance in IC and MEMS areas for the benefits of integration, cost, and performance. Among various non-conventional three-dimensional micromachining techniques, a plating-through-mask [1] has been acknowledged as one of the most IC-compatible and promising methods since it consists of only lithography and electroplating [2-9].

We have developed a novel two-step baking process to achieve high-aspect-ratios in UV photolithography with a conventional positive thick photoresist. We report high-aspect-ratio (>10:1) results in a single coated 91μm-thick photoresist AZ9262, which was introduced by Hoechst at SPIE in 1996. From extensive experiments, we improved the aspect ratio by minimum exposure, diluted development, reabsorption of sufficient water before exposure, and especially by extended and effective soft bake in two steps [10-11]. First, the baking is performed at an intermediate temperature in a forced convection oven for hours to evaporate large amounts of solvent. Second, the photoresist is heat-treated at an elevated temperature on an air-gapped hotplate with cover for minutes to enhance aspect ratios [12]. The reason for this improvement has been studied based on the photochemical process of the DNQ/novolac-type positive photoresist [13-15]. Using this two-step baking, we have obtained lines of 7.6μm-wide at the bottom in a single coated 91μm-thick photoresist. (aspect ratio of 12). Figure 1 shows the SEM photographs of the patterned thick photoresist AZ9262 having high aspect-ratios.

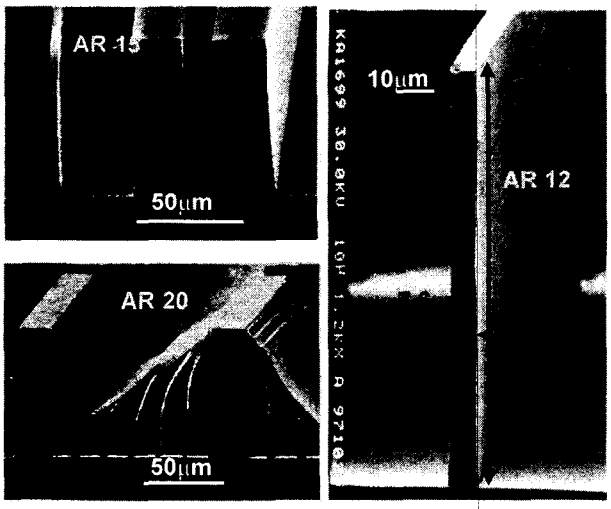

Figure 1: SEM photographs of thick photoresist AZ9262 with high aspect ratio.

III. 3-D Microstructure Process

In the formation of photoresists, great care must be taken to eliminate or minimize the exposure depth dependence. A sufficient amount of exposure is usually applied to the photoresist to make sure the photoresist bottom is developed. However, three-dimensional structure can be obtained in the photoresist by intentionally applying the depth control by Multi-Exposure and Single-Development (MESD) technique.

1. Multi-Exposure and Single-Development (MESD)

Single-step fabrication of electroplated air bridges is possible by forming the 3D photoresist mold with a Multi-Exposure and Single Development method (MESD)[12, 16-17]. In the MESD method it is important to control photoresist thickness. Figure 2 shows the experimentally-obtained exposure time vs. development characteristics of the 90μm-thick AZ9262 photoresist. One can easily observe that the photoresist thickness of shallowly-exposed areas, after the full development of deeply-exposed areas, remained constant with further development; i.e., it is saturated to a certain thickness. Also, the final thickness monotonically decreased with increasing exposure time. Figure 3 shows process sequence of the MESD. During the MESD procedure, multiple exposures with different photomasks are performed to respective depths in the thick photoresist. Then, the latent three-dimensional image of the exposed or unexposed volume in the photoresist is obtained by the following single development. The photoresist tone (positive or negative) determines the region (exposed and unexposed) to be remained after the deveopment. Figure 4 shows patterned photoresist and various structures using MESD.

2. Sacrificial Metallic Mold (SMM)

A monolithic integration method for 3-D electroplated microstructures of unlimited number of levels has been developed using unique planarization with a Sacrificial Metallic Mold (SMM). Contrary to the conventional electroplating mold of photoresist or polyimide, sacrificial metal layer can be used for the sacrificial layer, a planarizaiton layer, and a seed layer for the next-level electroplating as well. From this, three dimensional structures can be integrated in unlimited number of levels.

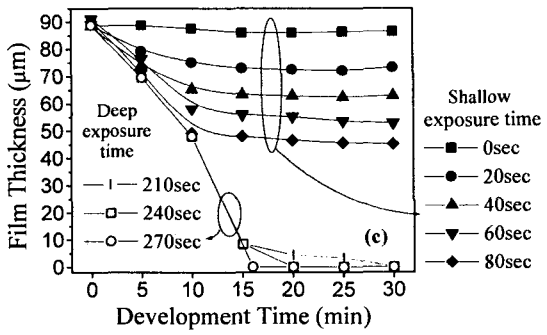

Figure 2: The expose time vs. development characteristics of the 90μm-thick photoresist

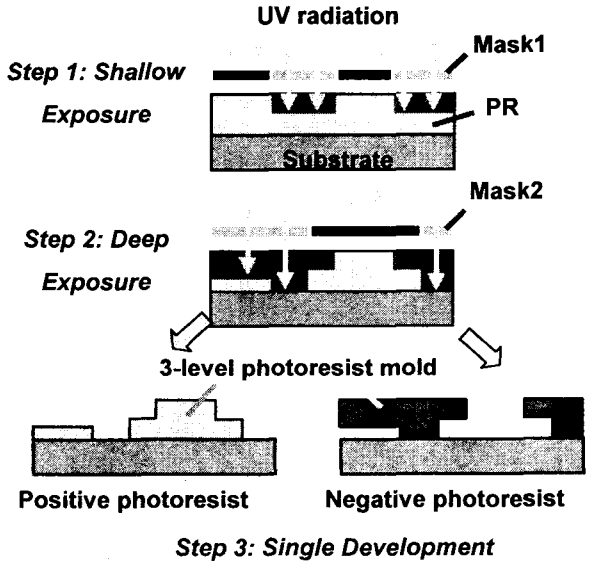

Figure 3: Process sequence of MESD.

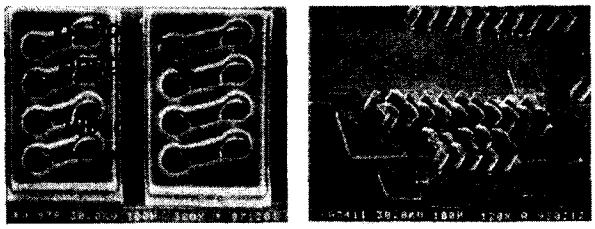

Figure 4: Patterned photoresist and various structures.

Figure 5 shows the various structures using SMM [16, 18].

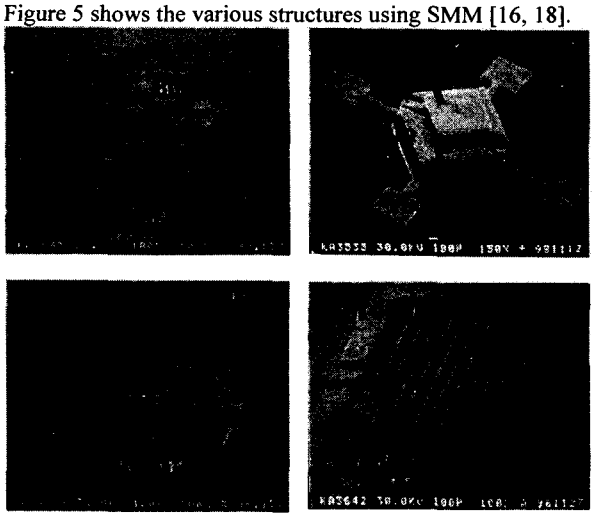

Figure 5: Various structures fabricated using SMM.

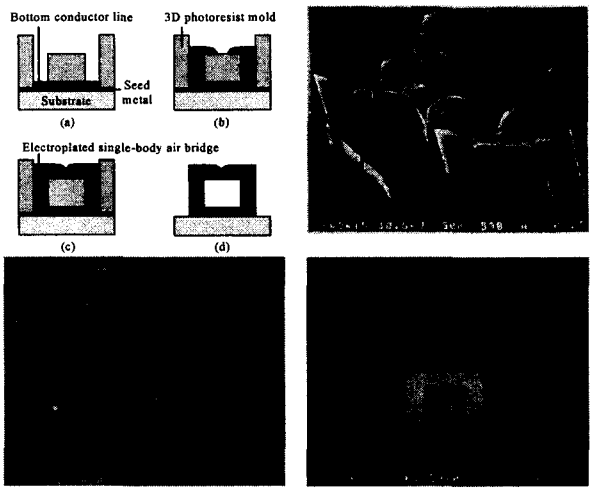

Figure 6: Fabrication process and integrated solenoid inductors.

IV. Integrated Inductors

An inductor, which converts electrical energy into magnetic energy, or vice versa, is one of the key components in electronics and magnetics. It can produce, detect, and store magnetic fields and has been used in many electrical and magnetic applications. Among various inductors, Radio Frequency (RF) inductors are still a topic of active research for monolithic integration. Researchers mainly have suffered from low quality-factors (Q's) of the monolithic RF inductors in the 5~20 range to date, which are still well below typical peak Q's of off-chip components in the ~100 range. However, the off-chip passives require a hybrid process and additional area in a board-level package, and associated parasitics make it difficult to design RF systems accurately.

1. Solenoid Inductors

Solenoid inductors have several advantages over spiral inductors. Bottom conductor lines only occupy areas on the surface, so that both the size and stray capacitance can be small; a high inductance can be achieved by merely increasing the number of turns with a relatively small increase in area occupation; and a simple analytical equation can be used to estimate or design the inductance as long as the solenoid is much longer than its radius. One of the aims of this work is to develop a simple, highly adaptable, and IC-compatible monolithic process for the fabrication of solenoid inductors. Figure 6 shows fabrication process for solenoid inductors and fabrication results. Figure 7 compares the performances of two identical on-Si and on-glass inductors. We observed higher inductance than expected in all cases and good proportionality between the inductance and the number of turns. From the former observation, it can be speculated that there is a negligible magnetic flux leakage between the turns. These experimental results indicate that higher inductance and Q-factors can be easily realized with optimization efforts.

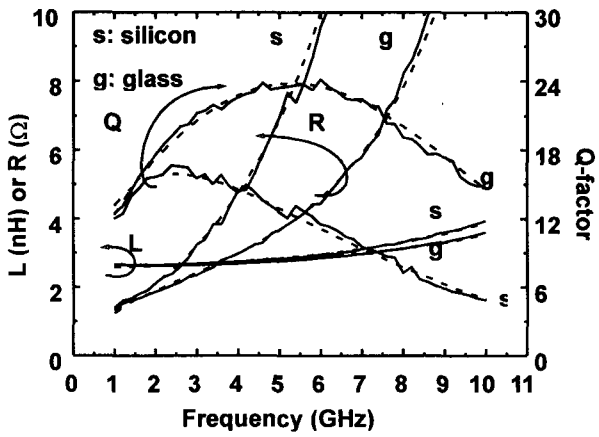

Figure 7: Comparison of identical inductor on Si and glass.

2. Levitated Inductors

Most areas in various RFIC are occupied by huge spiral inductors and big capacitors since inductor Q is roughly proportional to the area of the inductor, and the inductor should be a hollow type preventing eddy current loss in the center turns [19-20]. If area-consuming passives can be levitated from the substrate by several tens of microns, we can make a smaller RFIC by eliminating the areas for passives and greatly improve the RF performance of the passives by removing parasitic effects related to the substrate [21].

This simple concept of the "On-Circuit Passives" is clearly picturized in figure 8. Figure 8 (a) shows a monolithic spiral inductor levitated right on an RF circuit. Figure 8 (b) shows other RF on-circuit passives including a levitated Metal-Insulator-Metal (MIM) capacitor, a levitated micro-switch, and a transmission line. Advantages of these on-circuit RF passives are clearly small area occupation, less parasitic effects related to the substrate resulting in high Q,

low signal loss, and a high signal bandwidth.

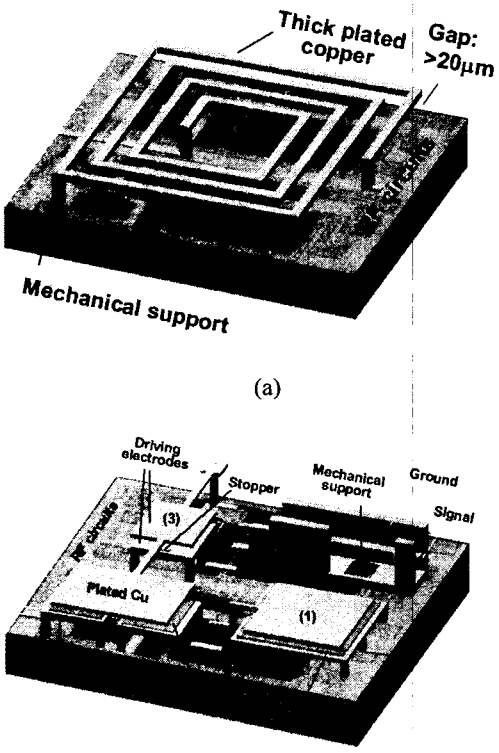

Figure 8: Proposed integration concept of (a) an inductor levitated on RF circuits and (b) other passives.

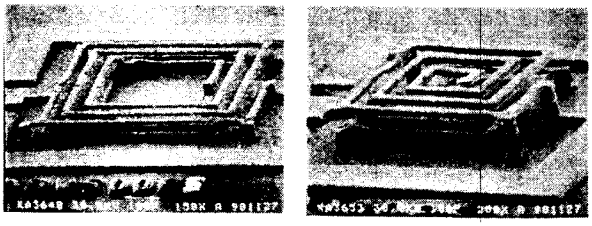

Figure 9: Levitated spiral inductors.

Figure 9 shows SEM photographs of the fabricated spiral inductors levitated from the substrate. Figure 10 compares the inductance vs. peak-Q performance of the levitated inductors with that of other inductors reported to date. The levitated inductors fabricated by the SMM method have shown the highest Qs.

V. Conclusions

In this paper, three-dimensional integrated inductors have been proposed and fabricated using the proposed three-dimensional microfabrication methods. The solenoid inductor has been presented using the Multi-Exposure and Single Development (MESD) method and electroplating, and the levitated spiral inductors have been realized using the Sacrificial Metallic Mold (SMM) method. The process of these two three-dimensional microfabrication methods are

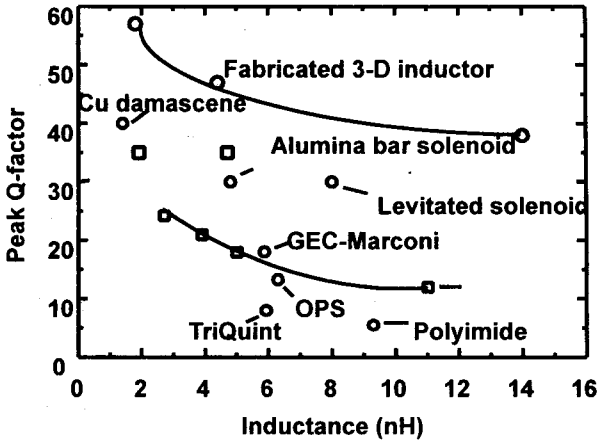

Figure 10: Comparison of the inductance vs. peak-Q performance of the levitated inductors with that of other inductors reported to date.

very simple and IC-compatible, and the performance of the fabricated inductors shows excellent results compared with other advanced integrated RF inductors. "On-Circuit Passives" concept has been proposed and we believe that the proposed fabrication process can be used for realizing a true transceiver single-chip in the near future.

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