Roadmap toward 2010
for high density/low cost semiconductor packaging

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ABSTRACT

A bare chip packaging technology by an encapsulated flip chip bonding on a build-up printed circuit board has emerged in 1991. Since then, it enabled a high density and low cost semiconductor packaging such as a direct chip bonding on mother board and high density surface mount components, such as BGA and CSP. This technology can respond to various requirements from applications and is considered to take over a main role of semiconductor packaging in the next decade.

SEMICONDUCTOR CHIP TREND

The most important element of a bare chip packaging technology is the chip itself. Semiconductor Industry Association (SIA) issues the semiconductor trend in every three years. The last edition was issued in May 1999[Sematech,1999]. It defines product areas such as Low cost, Handheld, Cost/Performance, High performance, Harsh and Memory, and indicates parameters trend from 1997 through 2011. Fig.1 shows a clock speed requirement. Except an extremely high speed limited area, a chip global clock frequency will increase from a several hundred MHz to 3 GHz and a off-chip clock frequency is basically under the same requirement. Fig.2 shows a chip size requirement. The size of memory chip will increase significantly and reached to 1000 mm^3. It is explained that the density does not

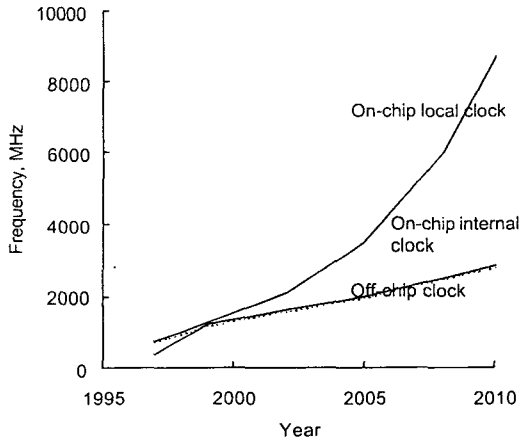

Fig. 1 Clock speed

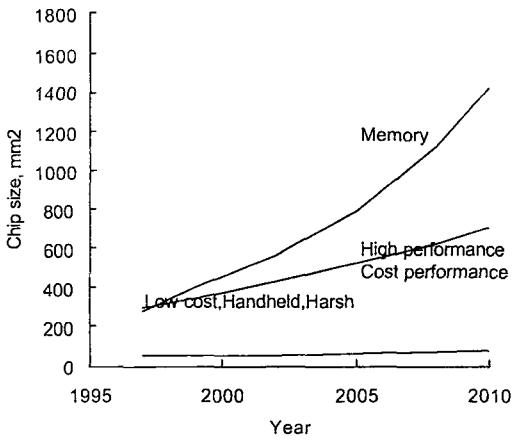

Fig. 2 Chip size

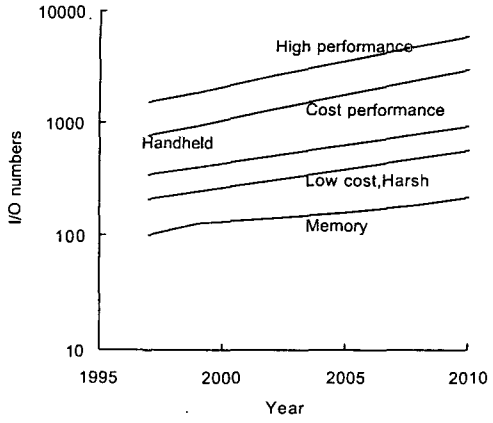

Fig. 3 I/O numbers

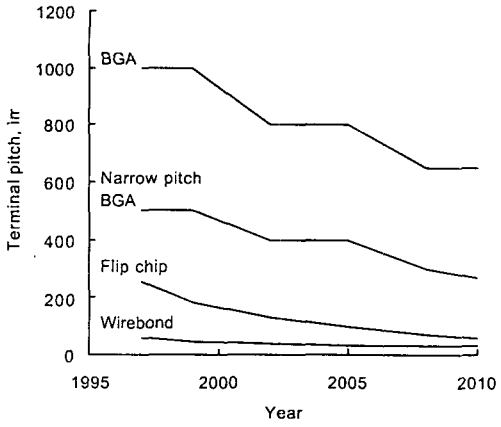

Fig. 4 Terminal pitch

satisfy the increase of memory requirement. Over 30 mm square chip has to be packaged. Fig.3 shows an I/O count requirement. It will increase from 1500 to over 4000 for a high density chip. Fig.4 shows a resulted pad pitch requirement. Wire bond pitch is not improved significantly and flip chip bonding which is to be a main joint technology will be improved by pitch and reaches to the same level with wire bonding today around a year 2010. Requirements for a flip chip carrier are also shown such as pad size, line width and lines space with assuming solutions by PCB technology and other thin film technologies.

The wire bonding technology has come to the end of progress due to the following reasons. I/O number per chip is limited since it utilizes only the peripheral area. FIG.5 shows corners of chips with flip chip design and wire bonding design. Flip chip has area array bumps with 250 μm and wire bonding chip has 125 μm peripheral bonding pad. If the size of the chip is 10 mm square, 1600 terminals can be placed in the area array and 300 in the peripheral area. In reverse, the size of 300 termials chip by area array is only less than a 5 mm square by today's chip density. Wire bonidng technology can provide only too low I/O number for high density requirement and too large chip than required for low density requirement. The next is a high resistance of the wiring conductor. Aluminum wiring in a chip has quite high resistance, a few ohms through a few hundred ohms due to its small geometry. In any part of the wire bonding chip, the electrical connection has to come in

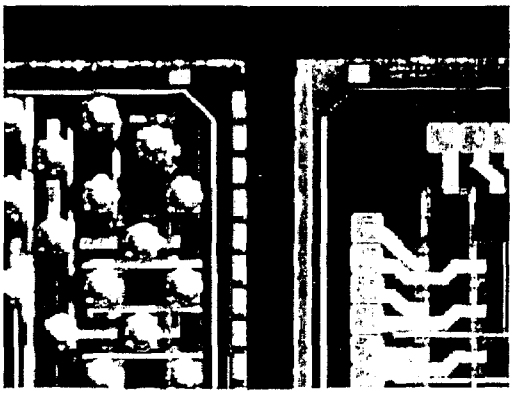

Fig. 5 Chip design comparison

from the peripheral I/O area and has to have a long trek through this high resitance conductor. It causes heavy attenuation and lose signal integrity due to a noise. In the mean time, the terminal can be placed where it is optimum in the area array design. In addition, when the signal goes out from the chip, there must be a return current to the point. It is required longer loop in a wire boniding chip due to the limited I/O numbers and location than flip chip in which the return point can be provided most close to the out-going point. As these reasons, wire bonding chip already has un-resolvable issues for the electrical perfromance and the chip cost.

FLIP CHIP JOINT TECHNOLOGY

As indicated in SIA roadmap, the joint technology for a chip bonding will shift from a wire bonding to a flip chip bonding due to the density and electrical property reasons. Fig.5 shows various types of encapsulated flip chip bonding. New issues and publications are least in 1998 compared with 1996 and 1997 when most of these in the figure emerged. It is considered that the encapsulated flip chip bonding technology is now getting into a practical implementation phase.

There are two major groups in the encapsulated flip chip bonding technology. One is a solder joint technology group which is shown in the upper side of figure and the other shown in the lower side is a compression contact technology group. Solder joint technologies are divided further to two categories. One is a type of reflowing chip bump formed by a solder and join to the carrier pad directly shown as (a) and the other is a type of providing solder bump on the carrier pad with reflowing it to join to the chip bump. The latter type has two kinds of chip bump which are solder shown as (b) and gold shown as (c). The compression contact type is explained to utilize a shrinkage stress of resin encapsulant. There are two types in this group. One is a type of compressing the chip bump to carrier pad directly for the contact as (d) and the other is a type of pinching conductive particles in conductive paste or an-isotropic film as (e). Basically, the solder joint type has a low initial joint resistance and the resistance change in a thermal cycle is low. Since the compression

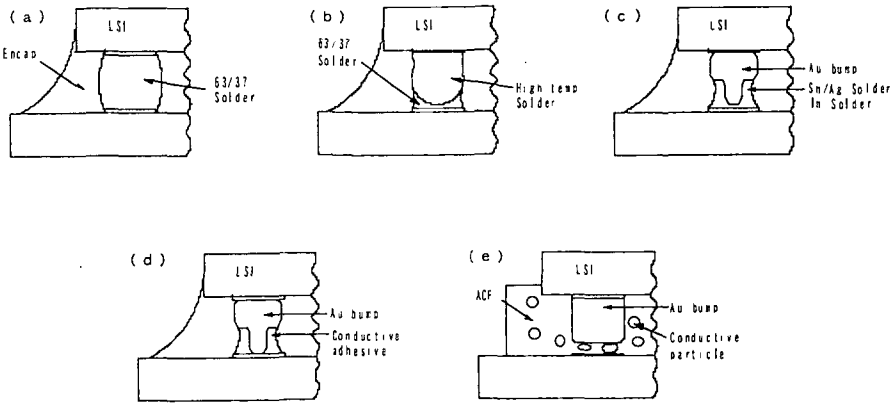

Fig. 6 Flip chip technologies

contact type has a relatively high initial resistance and the variation by temperature is wide, it is mostly used in consumer products range.

The key points of flip chip joint technology today are barrier metal reliability by its diffusion and lead free solder requirement. Except gold stud by ultrasonic ball bonding, solder deposition and gold or solder plating to form chip bump require barrier metal layer which interface the bump to chip mechanically and electrically. The vendor availability of this technique is still low and results high bumping cost per chip. Lead free is required from Year 2000 in Japan by a few volunteered consumer product makers. Though it is not a target set regally, the suppliers are forced to move the direction. Though there is no direct lead free target regally, the industrial waste dump yard is strictly limited for the waste contains lead from Year 2001 in Japan. For general components, SnAg is a primary candidate of lead free. For encapsulated flip chip joint, the candidates are wider since it can utilize far low strength material since the structure has significantly low stress condition.

BUILD UP PCB TECHNOLOGY

Table 1 describes a list of publications or announcement in industry magazines or academy in 1998. Compared with 1996 and 1997, most of products were listed in the catalogue of Japan Printed Circuit Association show and the new announcement is few. This technology is also considered to be into an implementation phase. However, the application using multi chip packaging that is a fundamental utilization of build-up PCB does not reach to a significant number. Table 2 shows a design rule roadmap of typical build up PCB in the market [Yasu lab.-IBM Japan, 1999]. As the structure of build up PCB, most of via formation technique have been emerged. The basic techniques for photo process and laser process are established. Via hole size which is a primary parameter of build-up PCB design is now at 80 to 100 μm range and keeps shrinking. A dielectric thickness which is a primary factor of via hole size is now reducing from 40 μm to 30 μm In the past, PCB industry has not practiced process control of manufacturing line as it was done in semiconductor because a conventional PCB has mechanical processes for a half of the key pro-

Table 1 Buildup PCB in Japan

PRODUCTS	MAKER	DIELECTRIC MATERIAL	BASE MATERIAL	DIELECTRIC THICKNESS	VIA PROCESS	VIA DIA.	VIA LAND	LINE/ SPACE	REFERENCE
CLAVIS	CMK	EPOXY FILM	FR4/FR5	40	LASER/PLATE	125/100	300	100/100	JPCA,1998
AAP/10	IBIDEN	EPOXY	GLASS EPOX	60	PHOTO/PLATE	100/100	275	150/150	JPCA, 1998 Takahashi, et al 1998
SLC	IBM JAPAN	EPOXY LIQUID	FR4/FR5	40	PHOTO/PLATE	70/60	90	25/35	JPCA,1998
FUJITSU BUILD UP	FUJITSU								JPCA,1998
ALIVH	MATSUSHITA	ALAMID-EPOXY		100	LASER/PASTE	150/150	300	50/50	JPCA, 1998 Kawakita et al. 1998 Mitamura et al. 1998 Tachibana et al. 1998
MEIKO BUILD UP	MEIKO	EPOXY LIQUID	FR4/FR5/BT	50	LASER/PLATE	150/100	275	50/50	JPCA, 1998
MITSUBISHI BUILD UP	MITSUBISHI			60	LASER/PLATE	100/100	250	75/75	JPCA, 1998
DV MULTI	NEC	EPOXY	FR4, etc.	40	PHOTO/PLATE	70/70	150	60/60	JPCA, 1998
ADVANCED PHOTO MULT	SHARP	EPOXY	PLYIMIDE/FR	40	PHOTO/PLATE	150/100	300	75/75	JPCA, 1998
MFS	SHINKO ELEC	POLYIMIDE		60	LASER/PLATE	100/50	150	40/40	JPCA, 1998
SHINKO BUILD UP	SHINKO ELEC.		FR4/HHR	35	LASER/PLATE	50/40	150	50/50	JPCA, 1998
B^{2}IT	TOSHIBA	FR4,BT		30	SILVER PASTE	150/150	200	100/100	JPCA, 1998 Takeda et al. 1998
VIL	VICTOR	EPOXY LIQUID		40	LASER/PLATE	100/60	200	50/50	JPCA, 1998

Table 2 Buildup PCB roadmap

Parameter	1999		2000	2001	2003	2006	2009
VPSG (Via Per Square Grid *1)	16	20	29	34	36	51	75
Photo via μm	100	80	60	50	40	30	20
Photo via land μm	150	120	95	80	70	55	36
Dielec. thickness μm	40	30				25	20
LPG (Line Per Grid *2)	13	17	25	32	46	56	64
Global line pitch μm	200	150	100	80	55	45	40
Global line width μm	75	50	40	30	25	20	20
FCA site escape line pitch μm	140	100	55	45	40	30	22
FCA site escape line width μm	65	40	25	20	20	15	10
Line thickness μm	18	12		10		8	6
Layers	1 + 1 ~ 4 + 4						

cesses such as lamination and drilling. Since the main parts of build up PCB are all chemical processes except in the case of laser drilling which is still a mechanical process, the process control is a key know-how to achieve high density and low cost products. The current dielectric epoxy resin property is enough for the reliability but the productivity (not the material cost but property stability in the production line) has to be improved. Utilization of low cost PCB infrastructure for high density products, which was the market place of ceramic carriers, requires more control to the material pot life and property variation in in-process queues.

BARE CHIP STANDARD

Activities currently on-going are mainly to establish a quality assurance for bare chip on distribution which is generally called as Known-Good-Die (KGD). One is in Electronic Industry Association Japan (EIAJ) organized viewing from the semiconductor manufacturing side and the other is in Japan Institute of Electronics Packaging (JIEP) organized viewing from the user side. The standard will be issued within 1999. In the report of open committee meeting of JIEP in November 1998, it is described that the bare chip is already in distribution by an individual contract basis. The standardization is expected to generalize this situation for public users and the circulation will be accelerated. The main barrier of KGD distribution has been a burn-in of chip. Wafer level burn-in has been developed and required equipment is emerging in the market. Overall situation is shifting to eliminate this barrier soon. The next step of standardization after KGD will be a geometry commonality, particularly the joint pattern. At the stage of chip design shift from wire bonding to flip chip bonding, the joint pattern shall be standardized. Eventually, an every user can utilize bare chip just as an ultimate surface mount component. At the final stage of this infrastructure shift, an application system is designed on bare chip attach on PCB package which consists of semiconductor chips, passive chip components, mostly capacitors, and PCB.

SUMMARY

- Requirements for semiconductor chip packaging are indicated in SIA roadmap. The requirements for joint and carrier are defined.
- A wire bonding technology is coming to the end of progress due to the limited electrical performance and density. A flip chip bonding will take the place to meet the requirement.
- Requirements for high density and low cost combination will become stronger and a multiple bare chips packaging on buildup PCB will satisfy the requirements.
- PCB technology roadmap has been re-established by connecting system-semiconductor-biuldup PCB requiremens and solutions.
- A standardization of semiconductor chip quality and geometry will be made for bare chip usage as an ultimate stage of surface mount technology.
- An application system will be structured on build up PCB package with chips and a few chip compoents.

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