Current semiconductor Packaging in Japan

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Abstract

General trend in electronics industry towards multimedia in the 21 century is presented here. All equipments require fast graphic processing together with thin and lightweight assembly technology. In Japan, CSP was developed and applied to mobile equipments for several years, and recently stacked die assembly technology is being developed. In addition, so-called flip chip technology is also being developed and which is applied to MCP and MCM little by little these days. Here current packaging technology in Japan is presented including above.

1. Assembly trends in Electronic Equipment

It is required to have better electric characteristics in package together with the body size these days. This is mainly because of the requirements from the necessity of high-speed graphic processing in multi-media equipment. As it is shown in Table1, big change will occur in every field in the 21 century. Especially digital equipment will become dominant in every field replacing analog one. Those equipments deal a lot of information in a short time as it is shown in Fig.1. Based upon the trend of those equipment semiconductor is going to be designed to integrate circuit as many as possible in one LSI. This is because of easier approach to optimize electrical characteristics of interface between each functional block compare to conventional assembly technology using individual package on motherboard. If the interface of each device is designed using current assembly technology, various kinds of noises such as simultaneous switching noise, cross talk, and ringing will occur at higher frequencies above 100MHz as it is shown in Fig.2. In another word, it seems to be difficult to stabilize these electrical characteristics, system LSI is thought to be the only solution. The assembly trend is shown in Fig.3. Package size have been becoming smaller and smaller to make assembly size small and light for mobile equipment. This happens to give good electrical performance at the same time. The reason is that the smaller lead
or trace length gives smaller inductance, capacitance and resistance.

In the mobile equipment, package changes from QFP to CSP for its small, thin and lightweight.

Next technology will be MCM/MCP with

small system and in the future 3 dimensional assembly technology will be developed and introduced in this area.

2. Chip size/Scale Package

It past almost 5 years since CSP have been developed and used for mobile equipment. Digital equipment such as digital camera, digital video recorder, phone, personal digital assistance, notebook computer increased very much these 5 years, and CSP is mainly used for these equipment.

There have been developed various kinds of CSPs as it is shown in Fig.4. The most common CSP is the miniaturized BGA whose structure is the same as BGA, and which uses tape as a substrate and wire bonding technology for interconnection. The size of this structure is a little bit larger than the chip size, because the bonding area is required around the chip. This package is applied to low pin-count devices such as memories, microprocessors, and ASICs.

μBGA^{TM} is developed by Tessera and this structure has an elastomer in between chip and substrate, which absorbs thermal stress caused by the thermal mismatch from silicon and printed wiring board. Then this type of package shows good solder joint reliability. The interconnection between interposer and chip is performed by single point bonding. This package is applied to memory devices first. Recently it is considered to use this package for high-speed memory devices because whose interconnection length is short and then shows good electrical performance.

For high pincount devices, miniaturized TBGA(Tape BGA) is developed. The structure is the same as the TBGA, and the process is almost the same as TCP(Tape Carrier Package). This package can withstand fine pad pitch and therefore suitable for high pincount devices such as ASICs.

These days flip chip technology is going to be applied for interconnection between chip and interposer. Ceramic substrate is also used for CSPs, and the interconnection technology is both wire bonding and flip chip technology. This package is used for small die size and small pincount, because thermal mismatch between ceramic and printed wiring board is larger than other packages.

The size benefit compared to QFP (Quad Flat Package) is shown in Fig.5 and the electrical characteristics compared to other package is shown in Fig.6. It is confirmed that CSP shows the best electrical performance.

Recently there has been developed wafer level CSP, which is processed in wafer stage as it, is shown in Fig.7. The benefit of this process is that assembly process at the back end can be omitted, then it has a potential of lowering cost and production period.

* μBGA^{TM} is a Trade Mark of Tessera

3. Approaches to System on a Package

Multi-chip assembly technology has been developed for many years, but is not applied widely from various reasons. Requirement for high density assembly technology of the DRAM modules become more and more strong for personal computers. Then TCP (Tape Carrier Package) technology is applied to DRAM as it is shown in Fig.8. As the DRAM chip is large, encapsulation material

and process is improved, and as the bonding pad is inline on the center of the chip, bonding process is also improved. Thin TCP is stacked on the module substrate and make it possible to realize double density memory on board compare to conventional TSOP. Assembly process is also improved to mount fragile memory TCP. This will be the first stacking technology in mass production.

Recently combining this stack technology and thinning process, more chips can be stacked as it is shown in Fig.9. Here thinning process is improved very much in combination with dicing process. This process is realized by dicing first before back grinding.

Fig.10 shows stacked chips in a conventional TSOP. Here each chip is assembled in normal process and the two leads are stacked before being molded in one package. Laser is used for connecting leads. This package is very convenient for users to handle with, and is also used for memory modules.

Another type of multi-chip application is shown in Fig.11. Technology itself is the same as the BGA but this realizes bite wide memory. Here the design of the board is important to achieve high-speed multi bit buses to optimize device interface. As long wiring is introduced because memory chip is center padded, molding technology for minimizing wire sweep has been developed.

Flash memory and SRAM are used for mobile phones these days. CSPs have been commonly used in mobile phones, but many flash memories and SRAMs are used in one phones theses day, then it is required to make it weigh lighter and its body size smaller. In this situation, stacked CSP is developed. Here wire bonding of low loop height is developed modifying reverse bonding technology, and thin die down to 150 μ m is introduced. This will be the standard package in this area.

4. Flip Chip Technology

Flip chip technology is investigated for CSP, BGA and MCM/MCP as an interconnection technology. Various kind of flip chip technologies developed before is summarized in Fig.13. Not only a metal interconnection but other new technology is also developed these days. Solder bump requires UBM (Under Bump Metallization) because the bonding pad of the chip is aluminum and solder cannot adhere aluminum directly, then which require wafer process. Gold bump is formed by either plating or wire bumping and the former requires UBM. Then gold wire bumping method is easily introduced by back-end. Various kinds of assembly technologies of the flip chip are proposed as it is shown in Fig.13. Reflow soldering is more popular but gold bump can not be assembled with eutectic solder because the diffusion of the gold and tin is too fast to form fragile intermetallic compound. Tin rich solder showed a little bit slow diffusion and shows better results. Gold bump with silver paste method is also developed.

Anisotropic conductive film is also used for attaching gold bump for MCM these days. Each method have the restriction of bump pitch and different reliability, then each technology is used for different way depending upon the requirement from the application.

Flip chip technology cannot be applied without other technology listed in Fig.14. KGD(Known Good Die) technology, fine pitch printed wiring board technology, fine pitch interconnection technology and under-filling

technology are the key issues to be improved. Most serious problem among them is the KGD issue. This technology has been developed for many years but still very expensive and not so popular in the industry.

Example of flip chip or CSP is shown in Fig.15. Bumps are arranged in area array, and the rerouting trace connects original bonding pad and the bump. Chip surface is passivated by thick passivation film.

Socket for fine pitch CSP and flip chip is also developed as it is shown in Fig.16. This can be achieved by developing sheet contactor with 2-metal polyimide tape and elastomer.

It is focused that production amount of bare chips will increase in the 21 century as it is shown in fig.17. Especially flip chip will increase dominantly among them. Package evolution is shown in Fig.18. New technology such as BGA, CSP and flip chip is focused to increase rapidly in the 21 century but conventional surface mount type package will remain as a major package at least in 5 years.

5. Future Assembly technology

Multi media equipment's requires graphic processing at a high speed and system circuit is becoming bigger and bigger. The conventional assembly technology can not perform well at this area because data transmission rate is too low compared to system LSI. System requires many memory chips with microprocessor, data transmission between memory array and microprocessor restrict performance of the system. Therefore improving electrical performance of interconnection is the key issue in the future.

Then focusing on near future COC(Chip on Chip)technology as shown in Fig.20 will be important.

Table1 Trend 0f Electrical Equipment in 21 Century

Equipment	Trend
Home appliances	◆Analog to Digital TV ◆Merge TV with PC ◆Interactive Communication (Merge PC with Phone) ◆Analog to Digital Audio (CD—ROM, MD, MP-3 etc..) ◆Video to Digital Disk (DVD) ◆LAN
Communication Appliances	◆Phone to Data Exchange ◆Mobil Phone (Analog to Digital) ◆Electrical Cable to Optical Fiber ◆Multi-functional Phone, Dual Phone etc..
Automobile	◆Navigation System ◆ITS and LAN ◆Electrical Control (Air Bag、Anti skid Break、Automatic Transmission etc..)
Infrastructure	◆Server(Big Capacity, High Speed) ◆Infrastructure of Net Work ◆Analog to Digital Equipment
Computers (PC)	◆To Net Working System ◆To Multi-functional Mobile Equipment

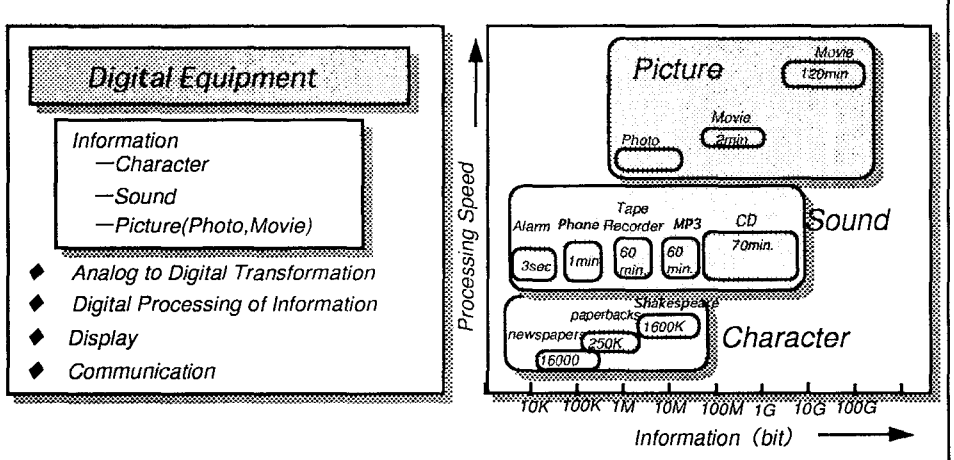

Fig.1 Digital Processing ot the Information

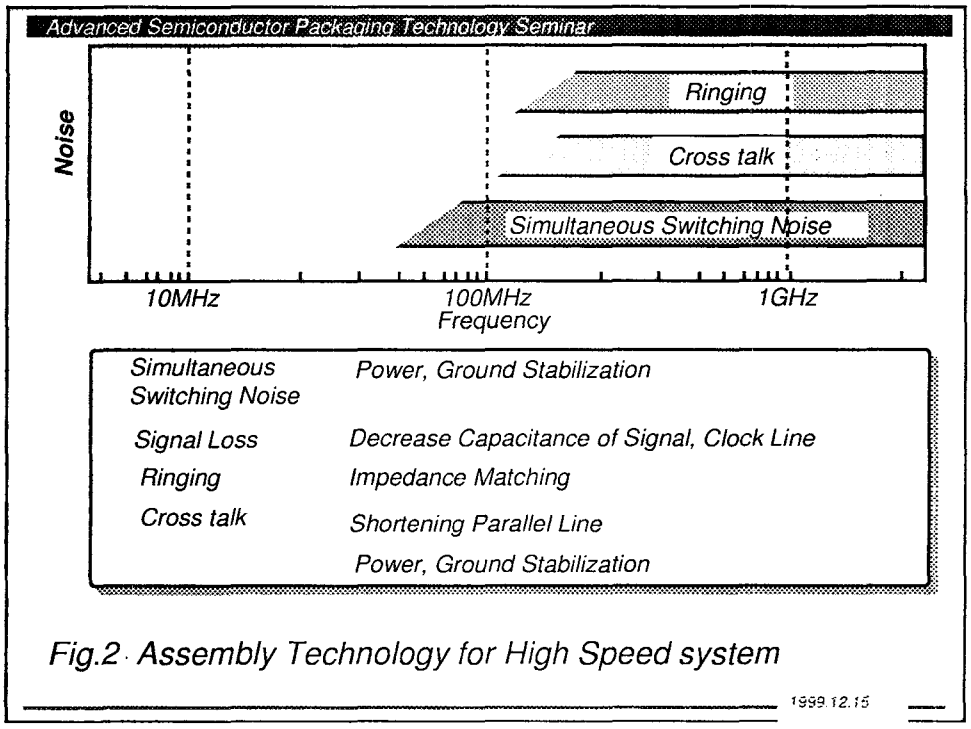

Fig.2 Assembly Technology for High Speed system

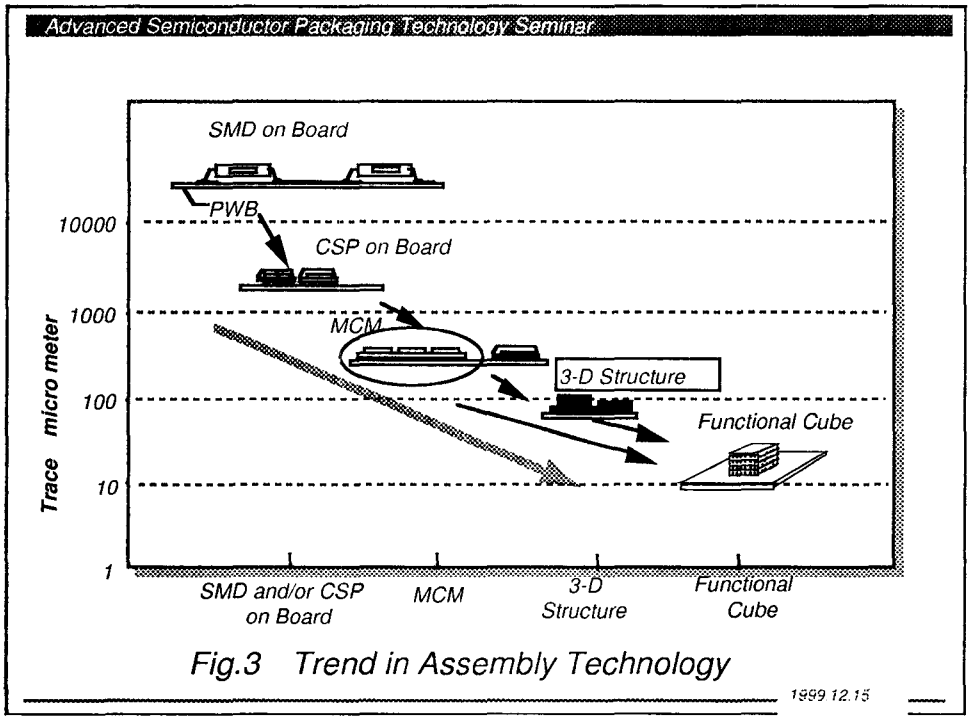

Fig.3 Trend in Assembly Technology

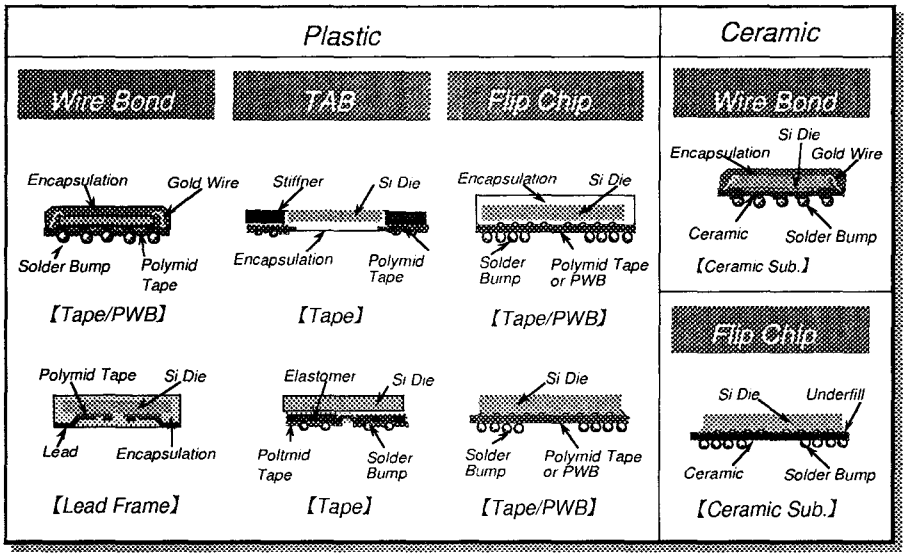

Fig.4 Various Kinds of CSPs

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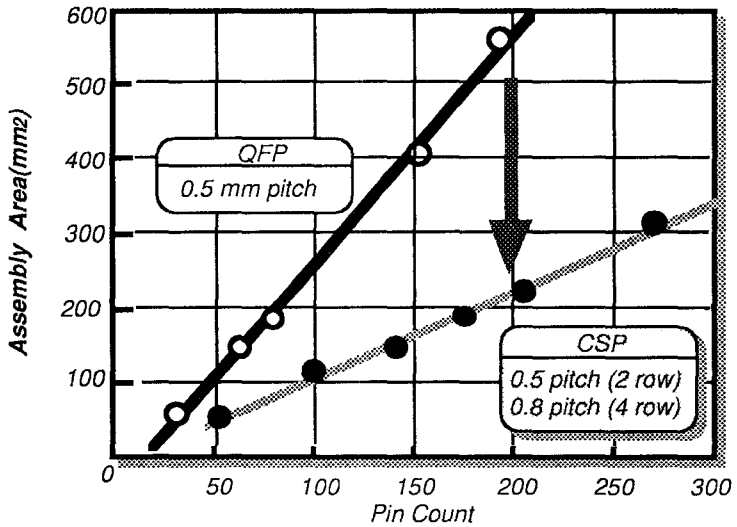

Fig.5 Small Assembly Area of CSPs

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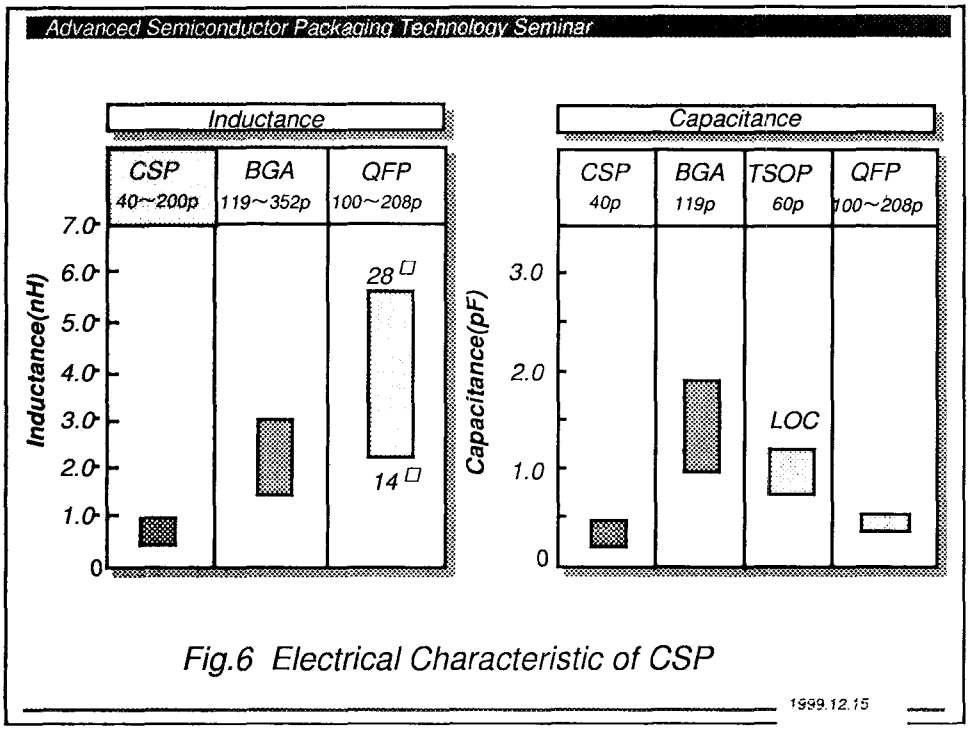

Fig.6 Electrical Characteristic of CSP

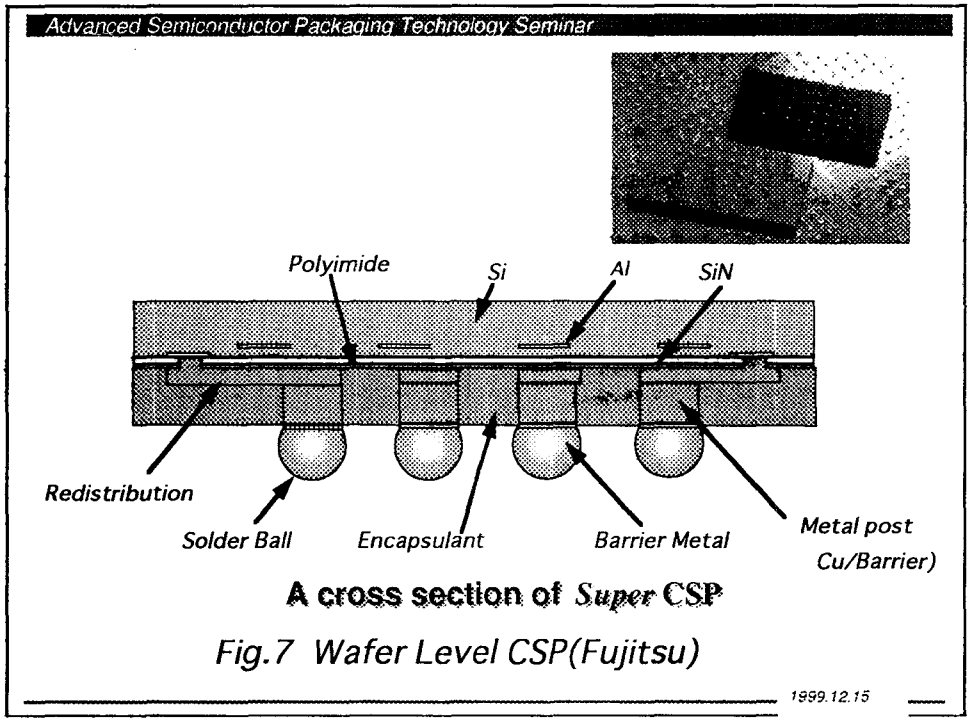

Fig.7 Wafer Level CSP(Fujitsu)

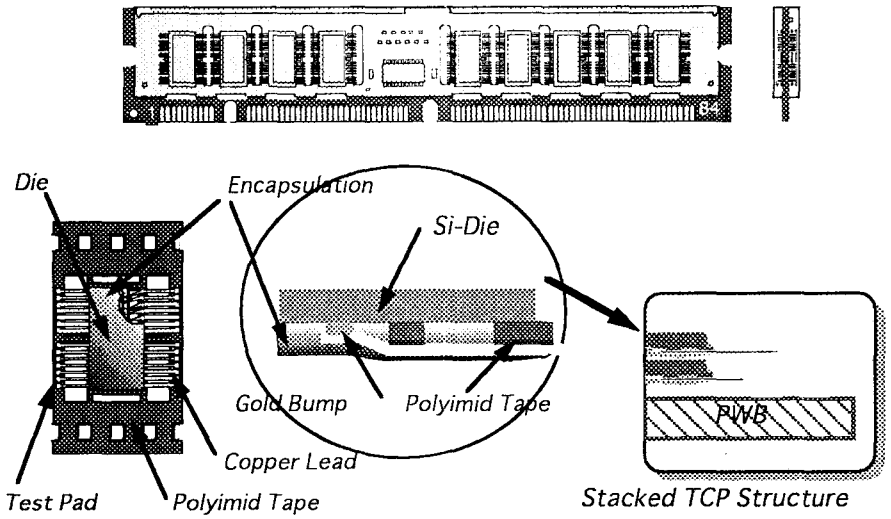

Fig.8 Stacked TCP(3-D) Module

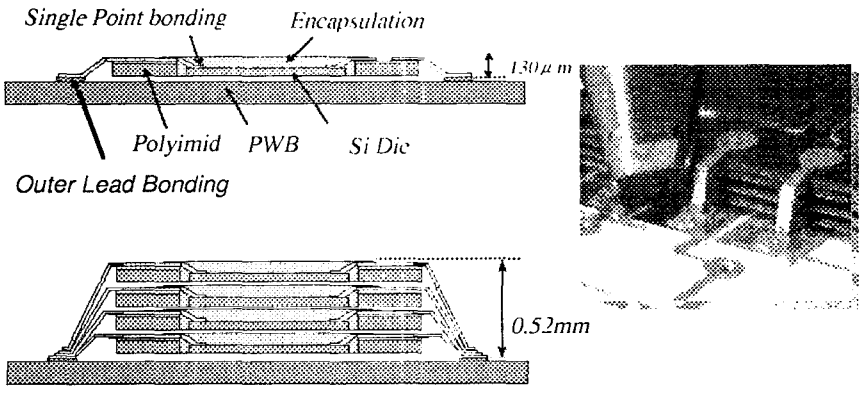

Fig.9 Paper Thin Package(Toshiba)

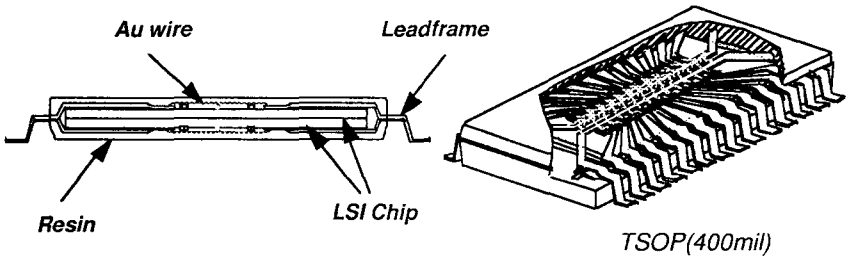

Fig.10 Structure of Double Density Package (DDP)

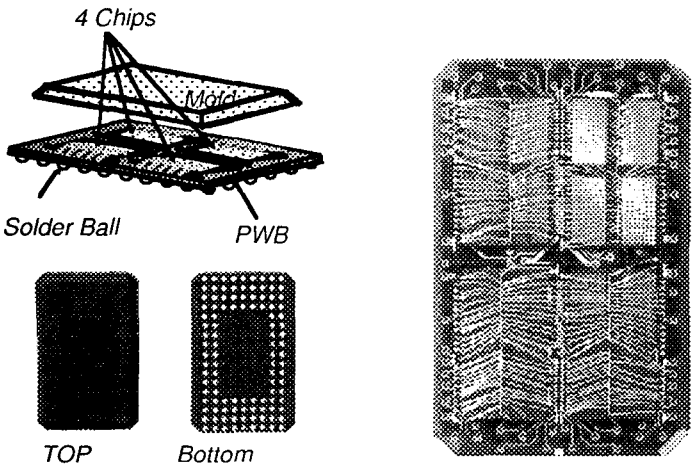

Fig.11 Bite Wide Memory Package(MCM)

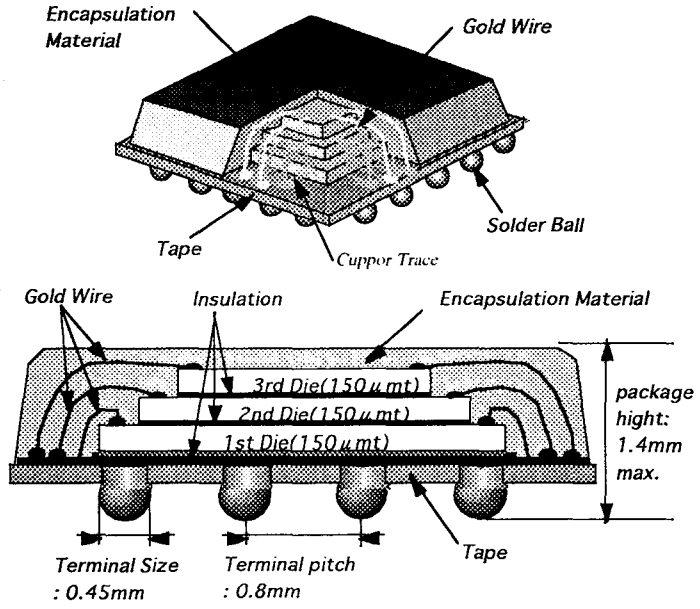

Fig.12 Stacked CSP(Sharp)

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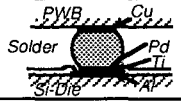
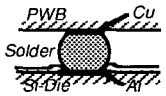
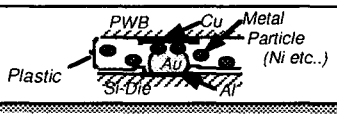
Interconnecting Method		Structure
Metal Interconnection	C C B (Solder Bump)	
	Solder Wire Bump	
	Gold Wire Bump with Solder	
Adhesive Interconnection	Gold Wire Bump with Silver Paste	
Compressive Interconnection	Gold Wire Bump with Anisotropic Conductive Film	

Fig.13 Typical Flip Chip Technology

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KGD Technology Wafer Burn In Die Burn In	Burn In Socket, Fine Pitch Probe Tech.
Fine Pitch Board Tech.	Low Cost High Density Laminate
Fine Pitch Interconnection Tech.	Improvement in Interconnection Reliability
	Assembly equipment
Underfill Tech.	Underfilling Material Infrastructure

Fig.14 Technical Issues for FCA

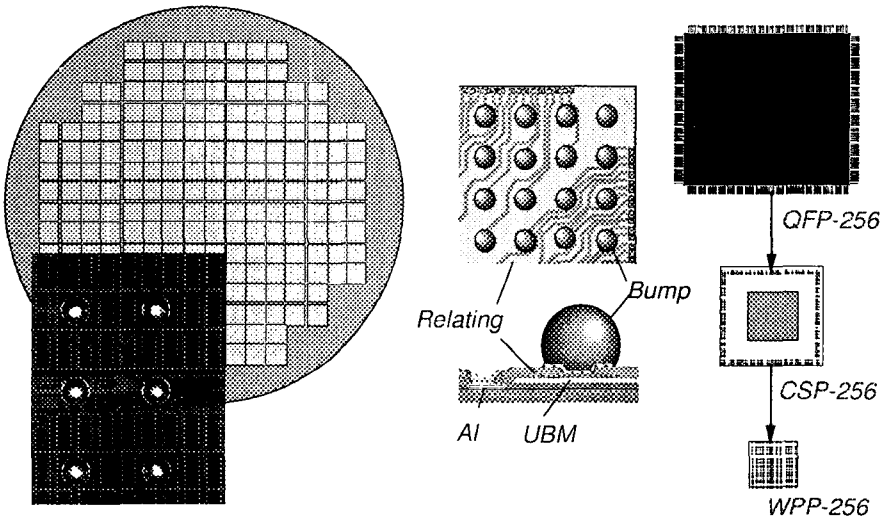

Fig.15 Wafer Process Package

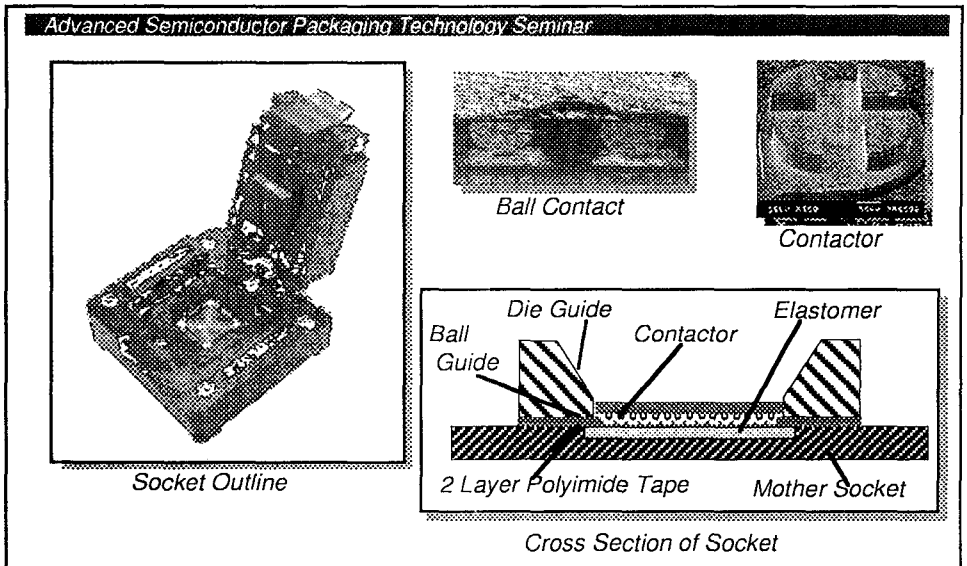

Fig. 16 Sheet Contact Socket for fine Pitch CSP and Flip Chip (Enplas-Hitachi)

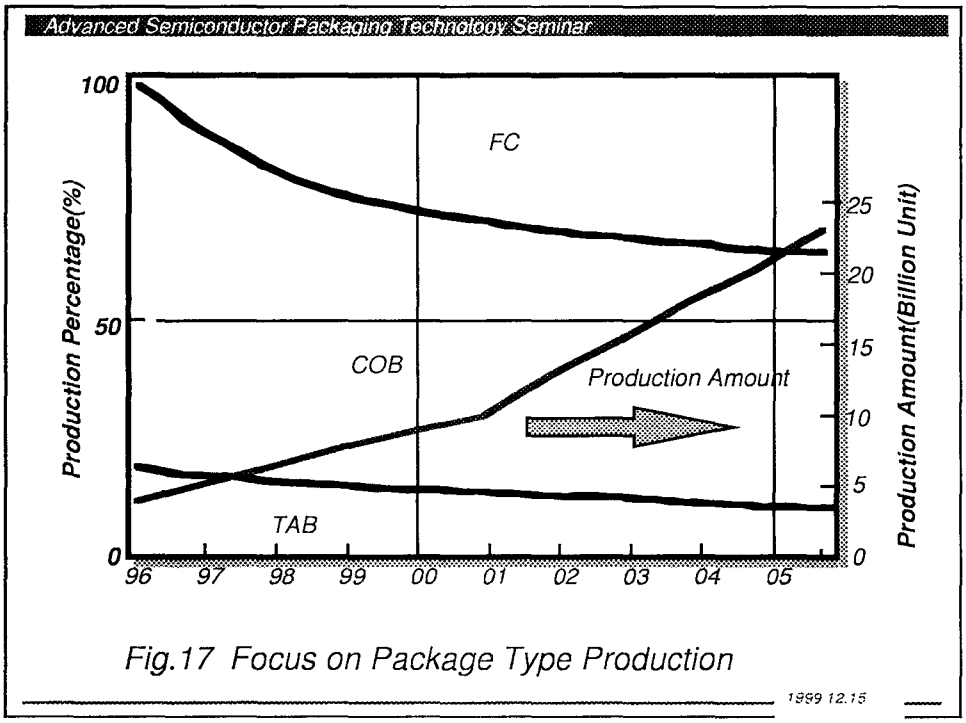

Fig.17 Focus on Package Type Production

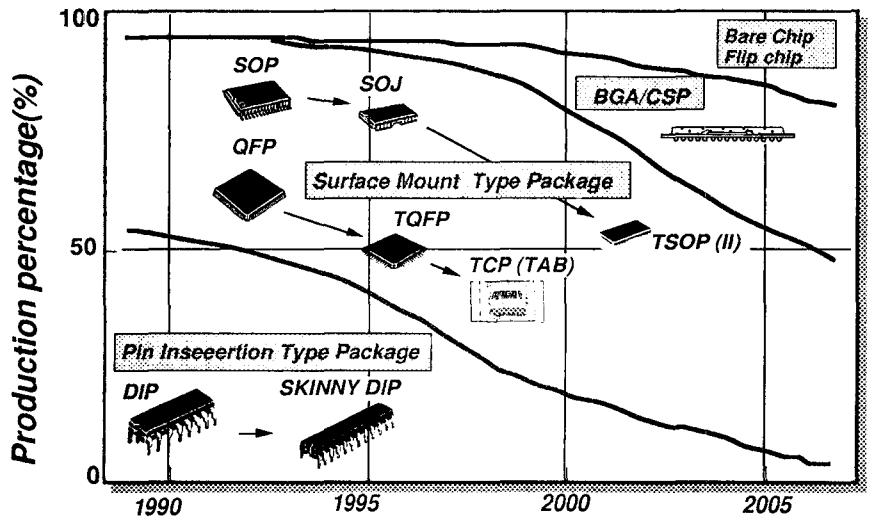

Fig.18 Package Type Evoluation in Production

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◆Processing Big Amount of Information is Required
→ Device Can Achieve High Speed Processing
◆Big Amount of Memory is Required
◆Interconnection between Chips
Restrict High Speed Processing

◆Increase in Requirement of Integration
◆Difficulties in Catching Up Requirement

◆System on a Chip
or
◆System on a Package

Fig.19 Future Assembly Technology

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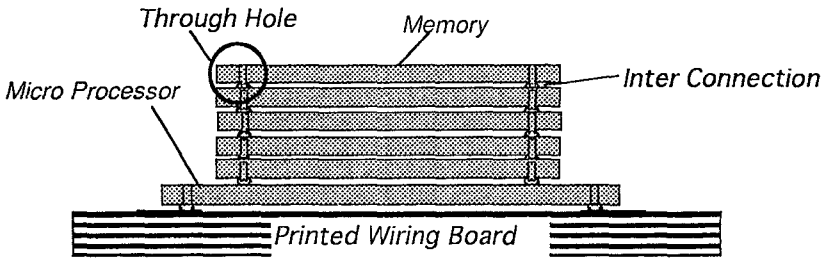

Fig.20 Development of 3-D Structure

COC (Chip on Chip)Technology