

1st Korea-Japan Advanced Semiconductor Packaging Technology Seminar

## **Overview of Japanese Microelectronics Technology**

**Sei-ichi Denda**

**1999.12.15.**

**IMAPS Japan**

# 1st Korea-Japan Joint Seminar

## Overview of Japanese Microelectronics Technology

1999.12.15 in Seoul

S.Denda  
IMAPS Japan

### Microelectronic Packaging R & D Activity

- JIEP (Japan Institute of Electronics Packaging)
  - IMAPS Japan (Committee)
  - NEDO (New Energy and Industrial Tech. Develop. Organization)  
High Density Electronic System Integration Project  
(3D LSI, Optoelectronics, Wiring design)
  - EIAJ (Electronic Industry Association of Japan)  
Research Committee
  - Tokyo University Packaging Laboratory
- 
- International Symposium (IEMT/IMC)
  - Domestic Conferences
  - Technical Meetings, Seminars and Workshops

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### Technology Roadmap

- JIEP: Packaging Technology in 2010

1. Relation to Electronics Industry
2. Packaging materials
3. Environmental Friendly Technology
4. Circuit Design
5. EMC
6. Circuit Board Manufacturing
7. Equipment and Automation
8. Reliability
9. Electronic Devices ←
10. Components Mounting
11. Inspection
12. Optoelectronics
13. 21st Century Packaging

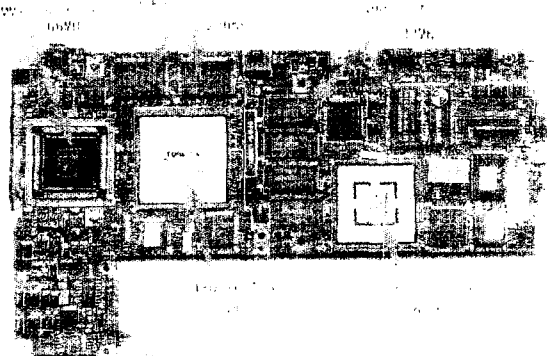
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### Application of Advanced Packaging

- Notebook PC (Note PC)
- Video Cameras
- Mobile Machine, PDA
- Portable Telephone
- LCD Display
- Game Player
- Electronic Cards
- Car Electronics

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### Libretto 1000 Substrate



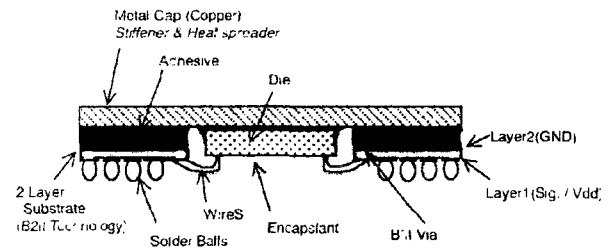
## Semiconductor Packages

### • Area Array Packages

- BGAs
  - PBGA, TBGA
  - MBGA, EBGA
  - FBGA (<0.8mmP)
  - (=CSP)
- CSPs
  - TCSP, MCSP
  - CCSP,  $\mu$ BGA
- Wafer Level CSP  $\leftarrow$

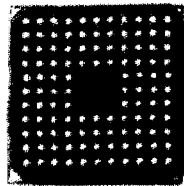
### • Flip Chips

- SBB
- WL Flip Chip
- Stacked Package
- TAB, TCP
- Outer lead QFP
  - 0.5mm Pitch
  - 0.4mm Pitch



## Toshiba EBGA

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112 pin CSP 10x10mm (Hitachi)

## Principal Area Array Structure -1

- Over 50 Area Arrays Announced
- Most of Venders have
  - PBGA, FBGA, Tape CSP
- Toshiba
  - EBGA, 2 Metal BGA, QFN, PTP
- Hitachi
  - $\mu$ BGA, Fan in CSP, FBGA  $\leftarrow$
- IBM
  - OMB-FCA
- NEC
  - D2BGA, FPBGA, MCM,
- Fujitsu
  - Super CSP, SON, MCM
- Matsushita
  - C-CSP, LGA

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## Principal Area Array Structure -2

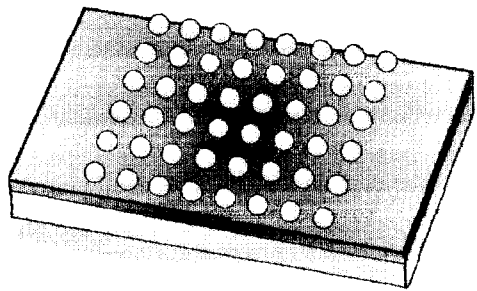
- Sharp
  - Stacked CSP, LCD Driver
- Mitsubishi
  - Mold CSP
- TI
  - Microstar
- Sony
- Oki
  - WLP CSP
- Epson
- Rohm
- Citizen
- Shinko
  - Super-CSP,  $\mu$ BGA, MOST
- Ibiden

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## WLP-Wafer Level Packaging

- Packaging process is completed at the end of the wafer process
- Ultimate low-cost, minimum size package
- Acceptable reliability by resin coating
- Matches to low pin-count (50-100) devices
- Fan-in redistributed bump layout
- Redistributed flip chip structure is Included
- Fujitsu-Shinko, Oki-Casio, Ibiden-Atomnics, Epson, Toshiba, Formfactor-Shinko

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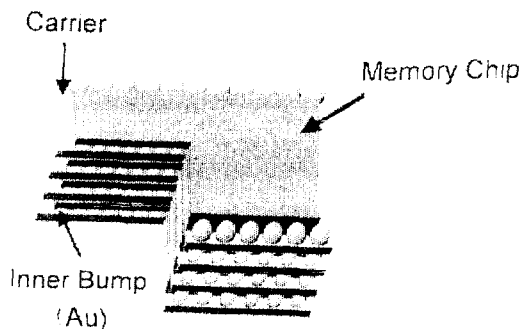


Super CSP (Wafer Level Package)

### Chip Stacking Structure

- 3-Dimensional Chip Integration
- Sharp : Stacked CSP , WB+FC  
DRAM+SRAM,SRAM+Flush,1.4mmH
- NEC : Memory Chip Stacking  
Au Bump FCs on Glass-Epoxy
- Toshiba : SLCC, Paper Thin Package  
Chip 50  $\mu$
- Fijitsu : SOC Module

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Flip Chip Memory Stacking

### Printed Circuit Board Process Technology

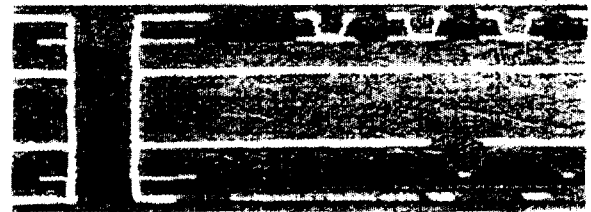
- Laser Via and Photovia Technology (80  $\mu$ )
- Fine Pitch Wiring (25  $\mu$ , IBM)
- Via Filling by Copper
- Low K Material Development
- Super Soft Flexible Tape for LCD Driver
- Surface Roughning Process for Substrate and Cu

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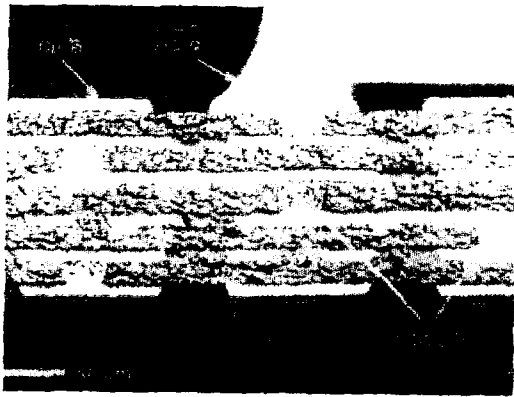
### Built-up Substrates

- Multi Layer PCB+Built-up Layers
- Typical Built-up 1-4 Layers  
(Via 100  $\mu$ , L/S 50  $\mu$ )
- Surface Laminar Circuit, IBM
- B2IT(Toshiba), Thick Film Paste Bump on Cu, All Layers Built-up
- ALIVH(Any Layer Interstitial Via Hole) (Matsushita), Laser Drilling, Paste Filling  
Big Market Share for Telephone
- IBSS(Ibiden) Via diameter 80  $\mu$

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Built-up Substrate, Ibiden

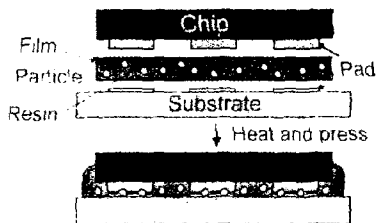
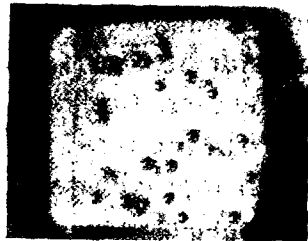


ALIVH Substrate (Matsushita)

### Anisotropic Conductive Material and Underfill

- Vertical Direction ( $R=0$ )
- Horizontal Direction ( $R=\infty$ )
- Ni, Plastic, Metal balls, Cu Pillar
- Film (ACF), Paste (ACP),
- Toshiba Chemical, Hitachi Chemical, Sony Chemical, Nitto,
- Underfill Material, Liquid Epoxy
- Capillary Flow Characteristics

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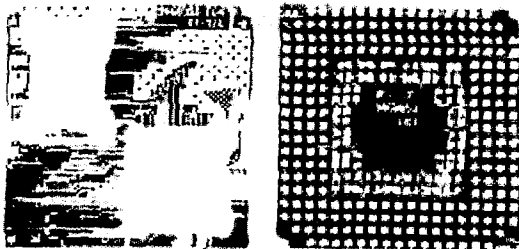


Anisotropic Conductive Paste

### MCM—Multi Chip Module

- Limited Mother Board Area
- Peripheral Pad Flip Chip with Underfill
- CPU and Memory Chips on MCM for PC
- Using Built-up, Fine Pitch Substrate
- Having Area Array Solder Bumps

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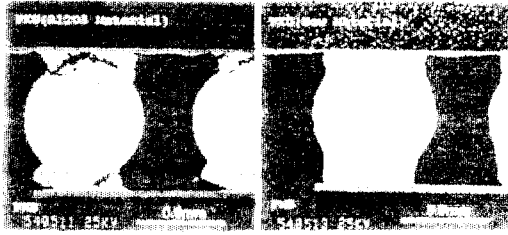
Multi Chip Module (NEC)

### Board Level Reliability

- Good Reliability for Package alone
- Secondary Reliability (Board Level Reliability), Thermal Cycling ( $-40\sim 125^{\circ}\text{C}$ ), more than 1000 Cycles Necessary
- Result of thermal expansion difference among chip, interposer and board
- Simulation Analysis of Internal Stress in Bumps
- Utilize Finite Element Method (FEM) and Software

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0.50 1.00mm 100 0.50 1.00mm 100



40 ~ 125 °C 400 Cycle  
Board Level Reliability

### Lead Free Solder

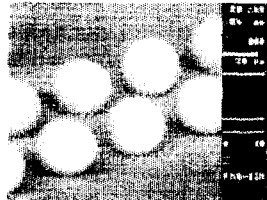
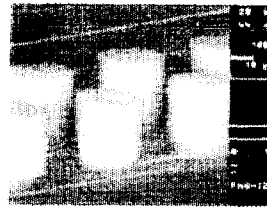
- Sn-Ag-X and Sn-Zn-X Systems
- Application to Volume Production Started
- Infrastructure is in Progress (Furnace, Flux, Components, Chemicals)
- Matsushita : Sn-Ag-Bi (MD Player Production)
- Sony: Sn-Bi-Ag-Cu-Ge
- Toshiba: 91 Sn-9Zn
- NEC: Sn-Ag-Cu
- Indium Solder Development
- Organic Conductive Adhesives
- Extensive Research for Pb Free Solder

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### Bumping Works

- Solder Ball Mounting
- Solder Paste Printing
- Solder Paste Transferring
- Metal Ball Mounting
- Electroplating of UBM, Au, Cu and Solder
- Electroless Plating of Ni-Au on Al Pad

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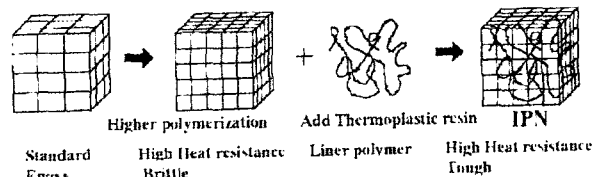


Solder  
Plating  
and  
Reflow  
(50 μ  
Pitch)

### New Organic Materials

- High Tg Material Development
- BT Resin, Tg 170°C
- 293°C MQ Polymer, Hitachi
- Photosensitive Composit Material, IPN (Inter Penetrating Network, Ibiden) Tg200°C
- Photosensitive Polyimide, Tg 230°C, Fujitsu
- DSOL-Deposited Substrate on Laminate Tg230°C, NEC
- Photosensitive Polyimide
- Liquid Crystal Polymer Film Development
- Undeformable Capillary Flow, Compression Flow
- Liquid Encapsulant

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Interpenetrating Network Structure (Ibiden)

## Environment Friendly Technology

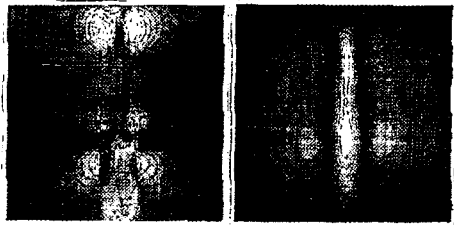
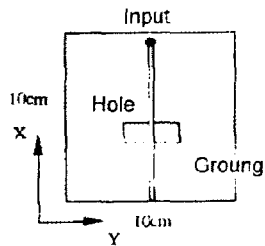
- Reducing Environmental Load from Electronic Products
- Life Cycle Assessment ,LCA
- CFC Usage Stopped
- New Solvent and Water System Develop
- Halogen Free Body, PC Board and Potting Resin Materials
- Volatile Organic Compounds (VOC) in Flux and Solvent
- Recycling of Printed Circuit Board

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## EMI-Electromagnetic Interference

- CPU Operation Frequency Increase(500MHz)
- Power Line Switching Noise
- Electromagnetic Field Analysis using Software
- Shielding by Multilayer Substrate
- Grounding Pattern Design
- Electromagnetic Wave Dark Room (Site) for Checking Product EMI
- EMI of Semiconductor Packages

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PC Board and EM Field

## Advanced Assembly Equipments

- CSP, Flip Chip Bonder  
Higher Placement Accuracy( $\sim 80 \mu$ ) than Conventional Mounter
- Dispensing Liquid resin and Underfill
- $N_2$  Furnace for Pb Free Solder
- Water washing system
- Wafer level burn-in
- Area Array Repair System
- X-Ray Inspection
- Sonic Wave Inspection

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