초청강연 I

Wafer Requirements : Memory Devices

J. G. PARK
한양대학교 부설 전기정보통신기술연구소 산하
첨단반도체 소재/소자 개발 연구소

Abstract

The presence of COP in CZ Si wafers causes the gate oxide integrity degradation and isolation failures in advanced DRAM devices. The COP induced gate oxide breakdown is associated with local oxide thinning and stress induced oxide breakdown while isolation failure is related to N^- channel implantation failure is strongly dependent on the COP size; I. e., it happens as the COP size is greater than 0.32 μm. Alternative way to achieve free of COP is the application of Epi wafers. However, Epi wafers contain the surface quality issue such as surface crystal defects and flatness degradation. Another way to be free of COP issue is the introduction of "Pure Silicon Wafer", pure silicon wafers are free of COPs, large dislocations, and OSF-ring. they are commercially available now.