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Microfabrication of Submicron-size Hole on the Silicon Substrate using ICP etching

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The various techniques for fabrication of Si or metal tip as a field emission electron source have been reported due to great potential capabilities of flat panel display application. In this report, 240nm thermal oxide was initially grown at the p-type (100) (5-25 ohm-cm) 4 inch Si wafer and 310nm Si_3N_4 thin layer was deposited using low pressure chemical vapor deposition technique(LPCVD). The 2 micron size dot array was photolithographically patterned. The KOH anisotropic etching of the silicon substrate was utilized to provide V-groove formation. After formation of the V-groove shape, dry oxidation at 1000℃ for 600 minutes was followed. In this procedure, the orientation dependent oxide growth was performed to have a etch-mask for dry etching. The thicknesses of the grown oxides on the (111) surface and on the (100) etch stop surface were found to be ~330nm and ~90nm, respectively. The reactive ion etching by 100 watt, 9 mtorr, 40 sccm Cl_2 feed gas using inductively coupled plasma (ICP) system was performed in order to etch ~90nm SiO_2 layer on the bottom of the etch stop and to etch the Si layer on the bottom. The 300 watt RF power was connected to the substrate in order to supply ~(-500)eV. The negative ion energy would enhance the directional anisotropic etching of the Cl_2 RIE. After etching, remaining thickness of the oxide on the (111) was measured to be ~130nm by scanning electron microscopy.

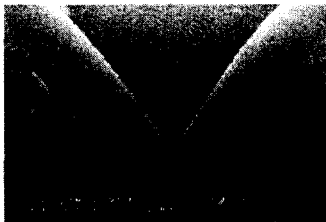

Fig.1.

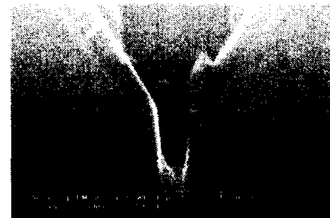

Fig.2

Fig.1. represents a SEM micrograph of the V-groove after dry oxidation.

Fig.2. represents a SEM micrograph of the V-groove after ICP etching. The micrograph presents a hole with 40nm deep after etching.