Progress in Si crystal and wafer technologies

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1.Introduction

The program of real ULSI mass-production using 300mm wafers is delayed and will be performed after 2002 years.On the other hand, device miniaturization towards 130nm is rapidly accelarated. Furthermore, various ULSI devices such as memory-logic hybrid device, so called System on a Chip (SOC) will be put into market.

Therefore, the wafer requirements such as flatness, particle,MCL and so on are becoming harder and severer with device shrinkage year by year. Silicon wafer as a basic material for ULSI has to meet these requirements. Furthermore, the cost reduction technologies are strongly expected. In this paper, progress in Si crystal and wafer technologies is discussed on single crystal growth, wafer fabrication, epitaxial growth, gettering, 300mm and SOI.

2.Si single crystal growth

One of the most concerned issues in crystal growth is grown-in defects. Recently, the mechanism of grown-in defects (voids) formation has been well understood. Excess vacancies which are incorporated from melt aggregate at around 1100-1070C, resulting in the formation of voids of which insides are covered by thin oxide layer due to the oxygen diffusion[1].

It is also widely recognized that the distribution of relative point defects, vacancy and self-interstitial, depends on the ratio of growth rate (V) and the axial temperature gradient (G), V/G[2]. In the case of larger V/G than the critical value of V/G, vacancy becomes rich, on the other hand, for smaller V/G than the critical one, self-interstitial becomes rich. As shown conceptually in Fig.1, the radial distribution of point defects and their aggregates depend on the distribution of V/G[3]. Generally, G increases at the crystal surface, resulting in the decrease of V/G. In the case of Conventional furnace, OSF-ring(Region B) locates at the periphery of crystal and almost all of crystal is occupied by voids (Region C). In the case of Improved 1, the position of OSF-ring moves towards the center of crystal. The vacancy-type defect free region (Region A) increases relatively and the one of voids

decreases. In the case of Improved 2, OSF-ring disappears. Vacancy-type defect free and self-interstitial defect free (Region D) are dominant. This region is called grown-in defects free area. With further lowering V/G, dislocation cluster appears. By controlling V/G along the axial and radial directions, the success of grown-in defects free crystal growth was reported[4].

Nitrogen doped crystals are paid attention from the possibilities of void dissolution by Ar annealing and grown-in defects free crystal growth as well as the enhanced oxygen precipitation[5] which is used for p/p- substrate. It was reported that in nitrogen doped crystal with the concentration of $5X10^{14}$atoms/cm^3 ,voids were easily annihilated by Ar annealing at 1150C compared to undoped crystal[6]. As-grown nitrogen doped crystals showed smaller size and lower density of voids and higher density of micro oxygen precipitates as shown in Fig.2. Figure 3 shows the relation between nitrogen concentration and V/G value of each boundary and OSF-ring position in the case of high oxygen concentration[7]. The V/G tolerance for grown-in defects free region became large with the increase of nitrogen concentration. It should be emphasized that grown-in defects region with nitrogen doping could be obtained much easier than the crystal without nitrogen doping.

3.Wafer fabrication

The silicon wafer fabrication technologies do not change substantially over past forty years. However, in order to improve flatness and to reduce cost, new fabrication technologies have been introduced step by step.

Low damage surface grinding process is now developed in order to overcome the problems of free abrasive lapping process. The industrialization of this process will promise the etchingless one[8], which has potential to avoid the degradation of wafer flatness. Furthermore, double side mirror polishing[9] will be inevitable for the achievement of higher flatness.

4.Epitaxial growth

The production use of homoepitaxial wafer for 64MDRAM and flush memory has been increased rapidly since 1997. Figure 4 shows an example of the trend of 200mm epitaxial wafers, which were produced in Japan and shipped to each region[10]. However, some issues such as heavy metal contamination and epi-micro defects still be remained.

Recently, SiGe/Si heteroepitaxy[11] has been re-examined from the point of advanced heterobipolar transistor (HBT) application as shown in Fig.5 for high speed and high frequency[12] and also bandgap engineering for increased mobility[13]. SiGe selective

epitaxial growth using UHV-CVD using Si_2H_6 + GeH_4 and LPCVD using SiH_2Cl_2 + HCl +GeH_4 have been examined.

5.Gettering technology

Gettering technology is still more concerned to improve device high yield and high performance. The everlasting miniaturization needs super flatness, which will be achieved using double side polishing, and low temperature process such as rapid thermal annealing (RTA). Furthermore, for advanced ULSI, epitaxial wafers are inevitable. Therefore, intrinsic gettering (IG) in RTA must be very important. Figure 6 shows the oxygen precipitation amount of p- wafers after 1000C for 16h as a function of pre- and post-annealing time[14]. Wafers were subjected to low temperature annealings from 650C to 900C before and after RTA process at 1150C for 30min. In the post-annealed wafers, oxygen precipitation was hardly observed, while in the pre-annealed wafers, oxygen precipitation was observed. So it is important to make a wafer design from the point of oxygen precipitation control by optimizing oxygen content, boron concentration, epitaxial growth conditions and pre-annealings.

Recently, the prediction of bulk micro defects (BMD) density and size using Fokker-Plank formula was reported[15]. From the prediction and experimental result, IG map for Ni contamination, which shows IG effect as a function of the precipitate density and size was obtained as shown in Fig.7[16].

6.300mm wafer

Si wafer diameter increased by 1 inch every 4 year. However, the demand for 300mm (12inch) is still aggressive beyond the trend. The technological progress has been made steadily as shown in Fig.8 to meet the 300mm roadmap. On the other hand, the device evaluation is delayed, so a lot of data, for example, the optimization between oxygen precipitation and device yield are not yet accumulated. Recently, it was pointed out that the crystal thermal history of 300mm ingots differs from conventional ingots from the observation of oxygen precipitation behaviors in 300mm CZ silicon[17].

7.SOI

A much attention has been paid to thin film SOI such as SIMOX for the application of next generation devices with high speed, low voltage and low power operation. Recently, the device fabrications using SIMOX, for example, MPU main stream by IBM have been announced. The issues of SIMOX materials are how to improve higher quality, how to getter Fe impurity, how to make and how to reduce cost.

8. Conclusions

Silicon crystal technologies have been made progress steadily for the requirements of ULSI devices. However, new technologies for cost reduction are strongly expected. At the same time, the dense information exchange and mutual step-up between device maker and wafer vender are key issues.

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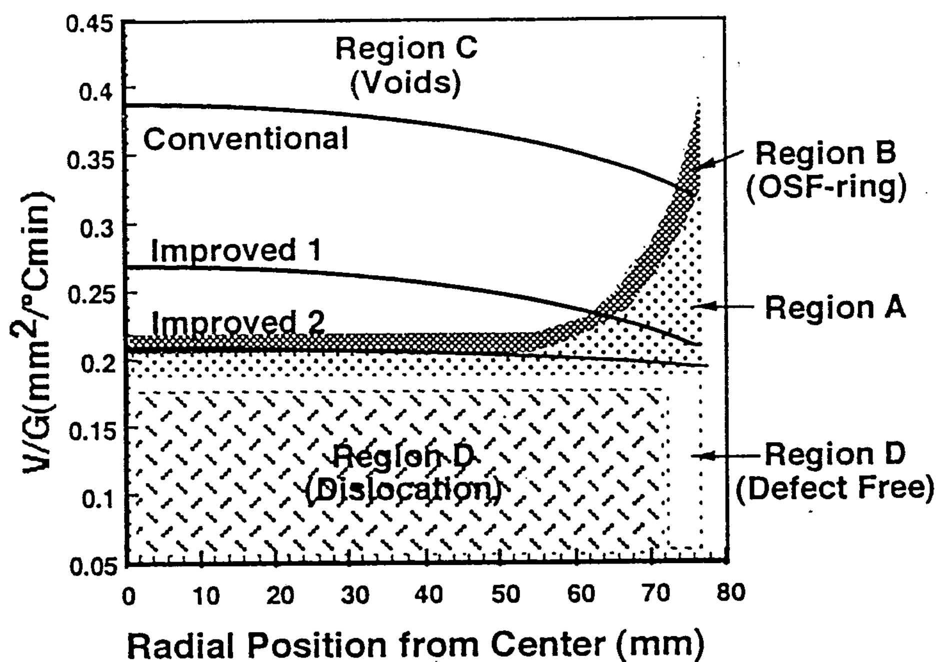

Fig.1 Schematic growth concept for realizing grown-in free Crystals[3]

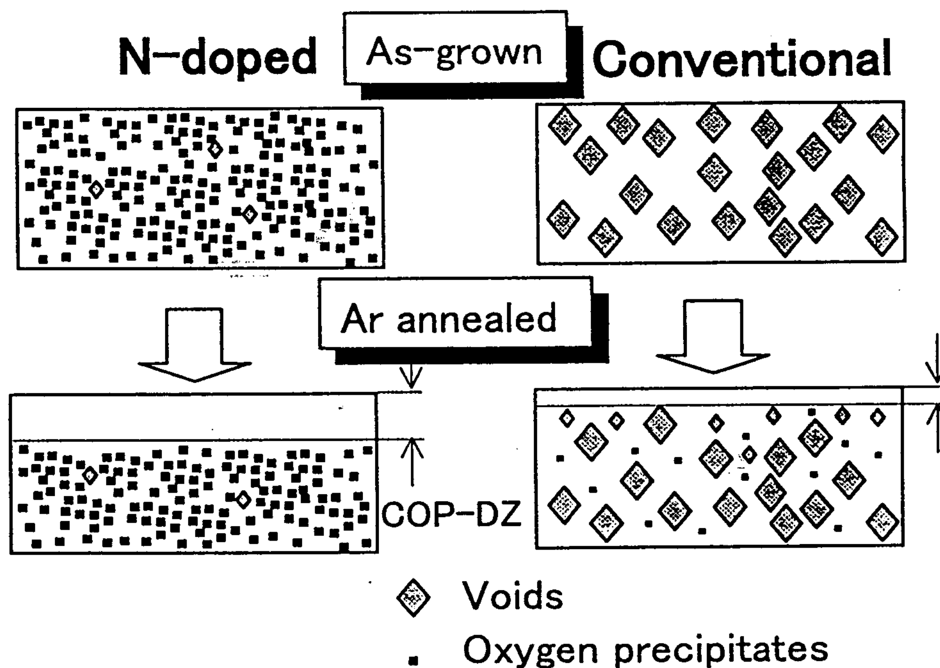

Fig.2 Mechanism of void annihilation and high density oxygen precipitates generation by nitrogen doping[6] (Courtesy of Dr.W.Ohashi).

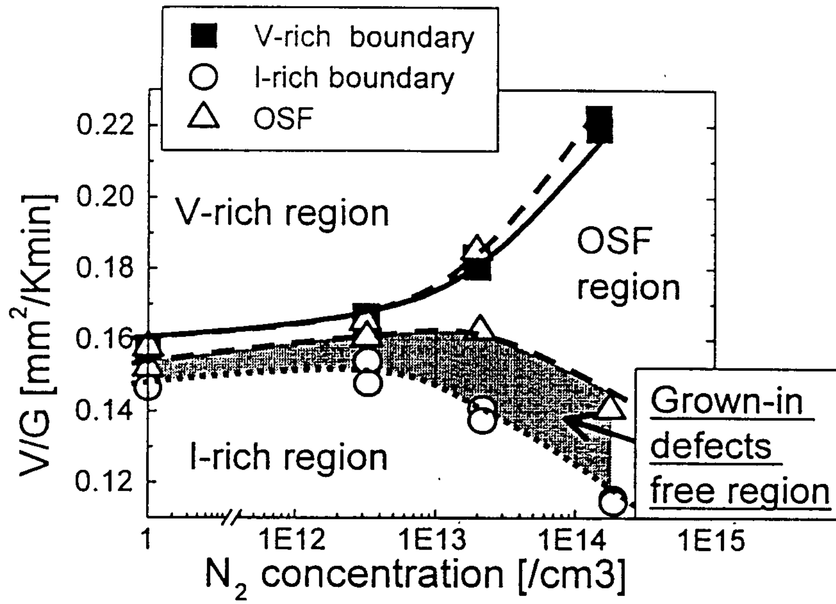

Fig.3 Relation between nitrogen concentration and V/G value of boundaries of each defect region[7].

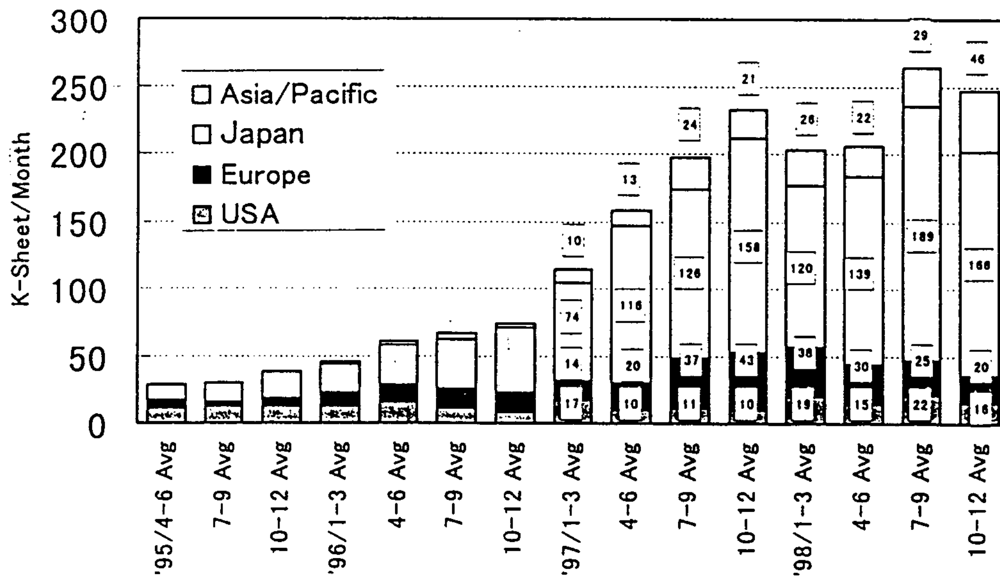

Fig.4 Trend of 200mm epitaxial wafer which were produced in Japan and shipped to each region[10].

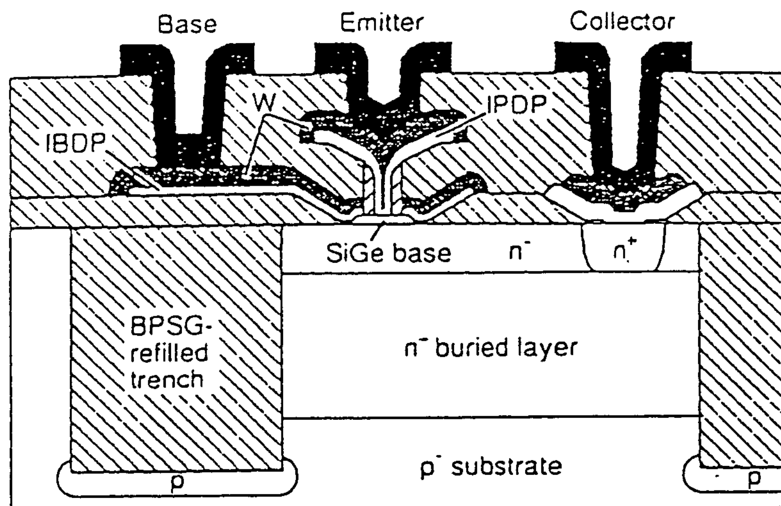

Fig.5 Schematic cross-section of a selective-epitaxial SiGe HBT with SMI electrodes[12].

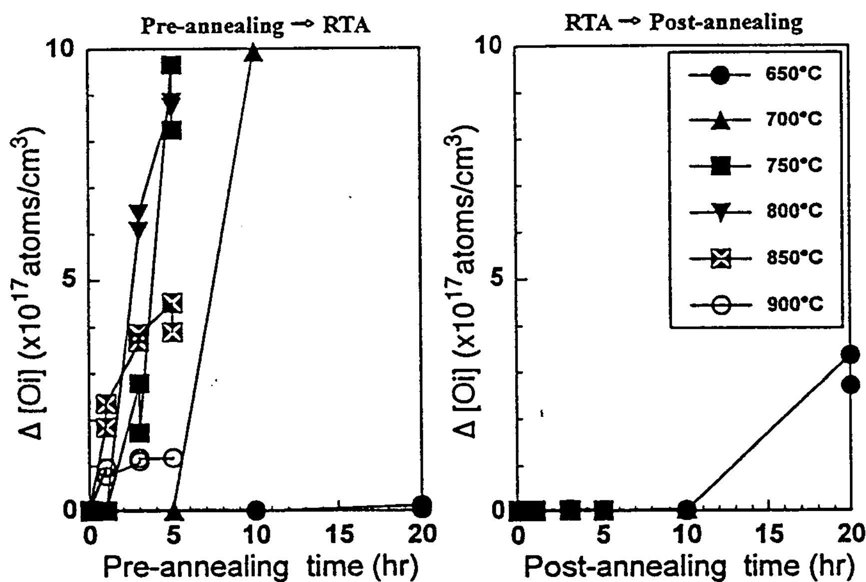

Fig.6 Oxygen precipitation ampunt of p- wafers after annealing at 1000C for 16h as a function of pre- and post-annealing time;wafers were subjected to low temperature annealings from 650C to 900C before or after RTA process[14].

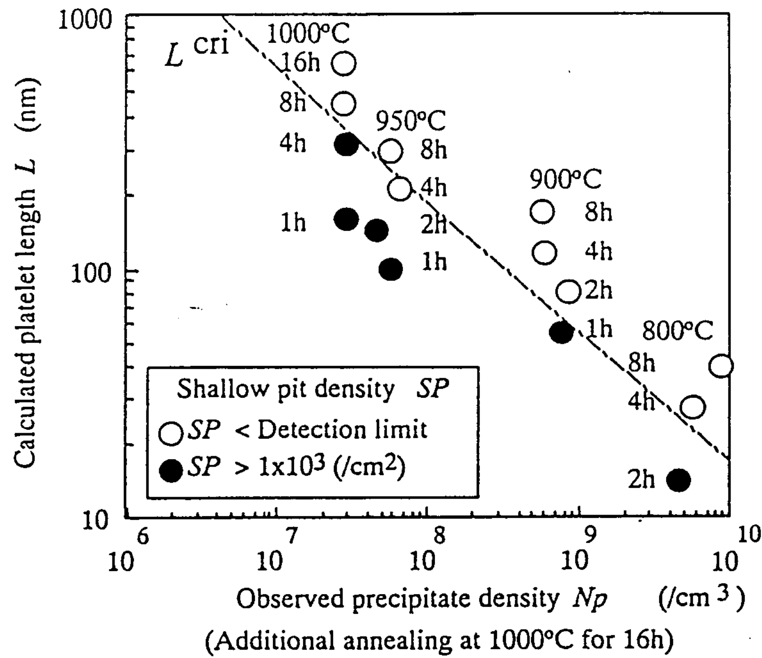

Fig.7 IG effect for Ni contamination as a function of precipitate density and size. Note that the precipitates have IG effect when their size is larger than the critical size(---)[16].

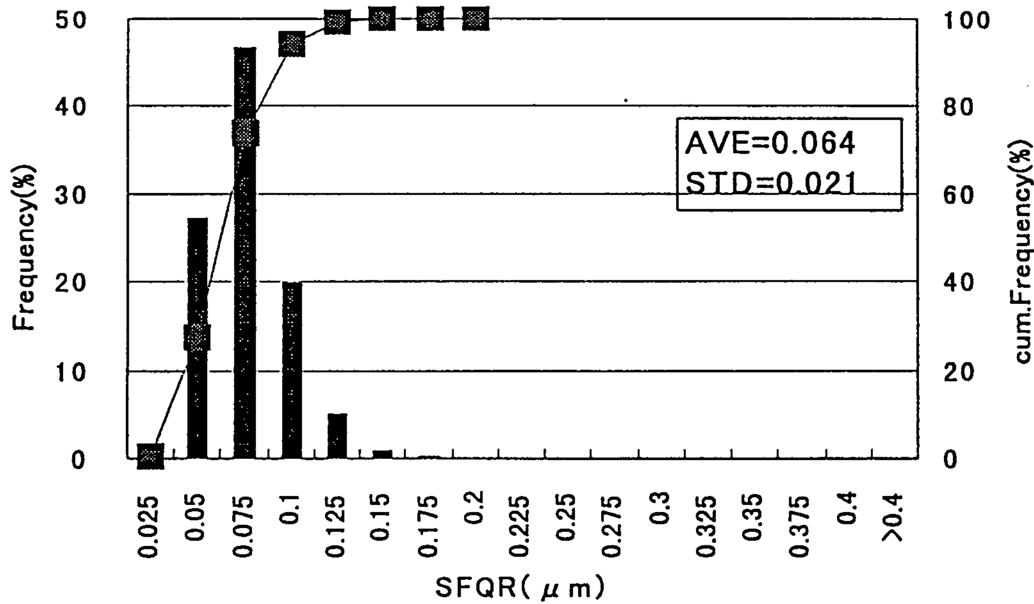

Fig.8 Example of frequency of SFQR measured on 300mm wafer.