LOW-DISLOCATION-DENSITY LARGE-DIAMETER GaAs SINGLE CRYSTAL GROWN BY VERTICAL BOAT METHOD

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Abstract

Low-dislocation-density large-diameter GaAs single crystals with low-residual-strain have been strongly required. We have developed dislocation-free 3-inch Si-doped GaAs crystals for photonic devices [1], and low-dislocation-density low-residual-strain 4-inch to 6-inch [2,3] semi-insulating GaAs crystals for electronic devices by Vertical Boat (VB) technique. We confirmed that VB substrates with low-residual-strain have higher resistance against slip-line generation during MBE process. VB-GaAs single crystals show uniform radial profile of resistivity reflecting to the flat solid-liquid interface during the crystal growth. Uniformity of micro-resistivity of VB-GaAs substrate is much better than that of the LEC-GaAs substrate, which is due to the low-dislocation-density of VB-GaAs single crystals.

1. Introduction

GaAs crystals are used for the substrates of potonic devices, such as LED and LD, and electronic devices, such as MES-FET, HEMT and HBT. Decreasing dislocation density is the strongest requirement for photonic devices, because dislocations deteriorate device performance and shorten the lives of devices. 2-inch wafers have been mainly used for device processes. However, requirement for enlargement of wafer diameter to 2.5-inch or 3-inch is becoming stronger, because of the strong requirement for cost reduction. Requirement for cost reduction is more serious in electronic devices, because the chip sizes of electronic devices are much larger than photonic devices. The size of the wafer has been enlarged from 3-inch to 4-inch. 6-inch wafer process has started in some device manufactures. Slip-line generation and breakage caused in large diameter wafer process, especially in 6-inch process, are serious problems. Slip-line generation and breakage are related to the residual strain in GaAs substrate [4]. Increase of the residual strain by enlargement of the diameter is one of the most serious problems in GaAs single crystal growth.

Figure 1 shows the typical growth techniques of GaAs single crystals. Horizontal Boat (HB), including Horizontal Bridgman and Horizontal Gradient Freeze, and Liquid Encapsulated Czockralski (LEC) are mature growth techniques, which were developed more than twenty years ago. Vertical Boat (VB), including Vertical Boat and Vertical Gradient Freeze, is a classical technique, but production had not succeeded for a long time. Poor temperature control made it impossible to grow a single crystal from a seed crystal reproducibly. Direct contact of GaAs melt to the crucible, namely wetting, sometimes caused polycrystalization. Recent developments of temperature control technique of VB furnace and of suppression technique of wetting made it possible to grow GaAs single crystals reproducibly. VB became the most notable technique for production of GaAs single crystals.

Growth of large diamater GaAs single crystals with low-dislocation-density and low-residual-strain is very difficult because of the physical properties of GaAs. GaAs has low mechanical strength, high dissociation pressure and small thermal conductivity in comparison with Si.

Growth under a low temperature gradient is necessary to obtain a crystal with low-dislocation-density and low-residual-strain. GaAs crystals after growth dose not suffer arsenic evaporation in HB and VB techniques. Therefore the growth under a low temperature gradient can be achieved, so that GaAs crystals with low-dislocation-density and low-residual-strain can be obtained. In LEC furnace, arsenic evaporation from the surface of the crystal is inevitable, therefore the growth under a low temperature gradient is substantially impossible. Dislocation density and residual strain of LEC crystals are much higher than those of HB and VB crystals.

Regarding the growth of large diameter crystal, VB and LEC techniques are much advantageous. In HB technique, quartz boat is deformed at the growth temperature, and the thermal environment around the crystal is asymmetry. These drawbacks make it difficult to obtain large diameter GaAs crystals by HB technique.

Thermal environment around the crystal is symmetry in VB and LEC techniques. pBN crucible used in VB technique keeps enough strength even at the growth temperature. In LEC technique, solid-liquid interface does not contact with the crucible. Therefore, the crystals are not affected by the deformation of the crucible.

Because of the reasons mentioned above, VB is the most promising technique to satisfy with the all requirements of low-dislocation-density, low-residual-strain and large diameter for GaAs substrates. The share of VB is becoming higher in GaAs wafer market. We have developed dislocation-free 3-inch Si-doped and low-dislocation-density and low-residual-strain 4-inch to 6-inch semi-insulating GaAs single crystals by VB technique. Growth and properties of the crystals are reviewed in this paper.

2. Crystal Growth

There are two problems to grow GaAs single crystals by VB technique. One of them is wetting. Poly-crystalization is caused at the region where the melt was wetted to the crucible. Inserting B2O3 layer between the crucible and the melt is very effective to prevent wetting. Another problem is concaving of solid-liquid interface. Large thermal stress is caused in the crystal when the shape of solid-liquid interface becomes concave, which causes the increase of dislocation density and sometimes causes a lineage, which results in polycrystalization.

Growth conditions by VB technique are shown in table 1. Pre-synthesized GaAs poly-crystals as a raw material and boric oxide as insertion to prevent wetting are charged in a pBN crucible. The crucible is mounted on a crucible support placed in cylindrical type multi-zone heater, which can provide very good controllability of temperature profile. The temperature of the heater is raised over the melting point, so that the GaAs poly-crystals are melted. The temperature profile of the heater is adjusted and fixed. Then the crucible is moved from higher temperature region to lower temperature region of the heater, so that a GaAs single crystal is grown under a controlled temperature gradient, which is much smaller than that of the LEC technique.

Figure 2 shows Si doped 3-inch conductive VB-GaAs crystals for photonic devices. Figure 3 is a 20cm length 4-inch semi-insulating VB-GaAs crystal for electronic devices. Longer 4-inch crystals up to 30cm in length, 5-inch and 6-inch diameter crystals are manufactured by VB technique in our semi-conductor factory.

3. Conductive Crystal

Dislocation density is the most important specification of Si-dope conductive GaAs substrates for photonic devices. Dislocation density is mainly increased by the thermal stress caused near the solid-liquid interface. Large thermal stress is caused when the shape of solid liquid interface becomes concave. We estimated the relation between the thermal stress and the shape of solid-liquid interface. Excess thermal stress caused near the solid-liquid interface is evaluated according to the Jordan's theory [5]. The excess thermal stress is defined as the sum of the positive differences between the absolute value of each of the resolved shear stress components to twelve equivalent ⟨110⟩ slip directions on {111} slip planes and the critical resolved shear stress. Distribution of excess thermal stress calculated using finite element method is shown in Fig.4. Large thermal stress is caused near the concave solid-liquid interface even under the smaller axial temperature gradient (5℃/cm) as shown in Fig.4 (a). Thermal stress is much smaller near the flat interface even under the larger axial temperature gradient (15℃/cm) as shown in Fig.4 (b).

Figure 5 shows the shapes of solid-liquid interface and the dislocation densities of 3-inch Si-doped GaAs single crystals grown by VB technique. The solid-liquid interface was deduced from striation profiles revealed by poto-chemical etching. Dislocation density clearly depends on the shape of solid-liquid interface. Dislocation density of the crystal with flatter interface is much lower than that of the crystal with concave interface. Dislocations in a crystal with flatter solid-liquid interface were observed by X-ray transmitting topography. Figure 6 shows a X-ray topographic image of a 3-inch Si-doped GaAs substrate with carrier concentration of $8 \times 10^{17} cm^{-3}$. There are only a few dislocations in the substrate. This substrate is substantially dislocation-free.

Figure 7 shows the correlation between dislocation density and carrier concentration of Si-doped GaAs crystals grown by HB and VB techniques. EPDs of HB crystals are almost on a curved line. EPDs of VB crystals are much lower than the line. Dislocation-free crystals are obtained even in low carrier concentration region. Lower EPDs of VB crystals are due to the symmetric shape of solid-liquid interface and symmetric thermal environment.

Residual strains in GaAs crystals were measured by a computer controlled infrared polariscope [6]. Residual strain is related to the density and distribution of dislocations. Figure 8 shows residual strains of a 3-inch non-doped LEC-GaAs single crystal with high dislocation density of 30,000 cm^{-2} and a 3-inch Si-doped dislocation-free VB-GaAs single crystal. The LEC crystal with high dislocation density shows higher residual strain of 9.2×10^{-6} and 4-fold symmetry which is correlated with the symmetric distribution of dislocations. Dislocation-free VB crystal shows lower residual strain of 3.8×10^{-6} and no symmetry.

4. Semi-insulating Crystal

4.1. Dislocation density and Residual strain

We have developed 4-inch to 6-inch semi-insulating GaAs crystals for electronic devices by VB technique. Keeping flat solid-liquid interface during the crystal growth is most important to suppress lineage formation, which sometimes results in polycrystalization, and to obtain large-diameter long semi-insulating GaAs single crystals. We apply computer simulation technique to optimize the growth condition, so that 4-inch semi-insulating GaAs crystals with 20 to 30 cm in length, 5-inch and 6-inch single crystals with 15 to 20 cm in length have been grown reproducibly.

Figure 9 shows dislocation densities of (a) 4-inch and (b) 6-inch GaAs single crystals grown by VB technique. Dislocation density is evaluated by counting the number of etch pits revealed by molten KOH etching. Dislocation densities of both 4-inch and 6-inch VB-GaAs crystals are one order of magnitude lower than that of the LEC crystals.

Residual strains of 4-inch and 6-inch VB and LEC substrates are shown in Fig.s 10 and 11. Residual strains of the VB substrates are less than half of that of the LEC substrates in both 4-inch and 6-inch diameter. Though the residual strains in the LEC substrates show 4-fold symmetry, those in VB substrates do not show 4-fold symmetry. It is thought that the residual strains of the VB substrates are lower than detection limit even in large diameter crystals.

Profiles of dislocation density and residual strain along the growth axis of 4-inch and 6-inch VB crystals are shown in Fig.12. Dislocation density and residual strain are low enough from the shoulder to the tail in both 4-inch and 6-inch crystals.

We evaluated the resistance against slip-line generation during MBE process. The wafers are heated at 600－650℃ for 30 minutes in MBE chamber. Figure 13 is the sketch of the slip-line on the wafer observed after MBE growth. Though many slip-lines are generated on the 6-inch LEC wafer, no slip-line is generated on the 6-inch VB wafer. It is thought that slip-lines are generated, when sum of the residual strain in the substrate and the thermal strain generated during MBE growth became larger than the critical resolved shear stress. Therefore, the difference of the slip-line generated during MBE process is attributed to the difference of the residual strain in 6-inch GaAs substrates.

4.2. Electrical properties

Control of resistivity is very important for semi-insulating GaAs substrates, because the resistivity affects the performance of electronic devices. Resistivity is dominated by carbon, impurity and EL2 concentrations. The concentration of impurity is stable between lot and lot. Therefore, resisitivity is substantially dominated by carbon and EL2 concentrations. We achieved very good controllability of resistivity in GaAs crystals by developing carbon doping technique. Figure 14 shows the relation between carbon concentration and resistivity of GaAs single crystals grown by VB technique. The wide range control of resistivity in $0.5-50\times10^{7}\Omega\mathrm{cm}$ have been achieved by controlling the carbon concentration strictly. Radial profiles of resistivity, carbon and EL2 concentrations are shown in Fig 15. Radial profile of resistivity on a 6-inch VB-GaAs substrate is as uniform as that on a 4-inch LEC-GaAs substrate due to uniform radial profile of carbon and EL2 concentrations. EL2 concentration and its profile are adjusted by post-growth annealing. Uniform radial profile of carbon concentration is thought be due to the flat solid-liquid interface of the VB-GaAs crystal.

Variation of micro-resistivity affects uniformity of device properties, such as Vth of FET. Therefore, micro-resisitivity is one of the most important properties of semi-insulating GaAs substrates. Figure 16 shows the radial profiles of micro-resistivity on 4-inch LEC and 6-inch VB substrates measured at 100 micron-pitches. Normalized standard deviation of the 6-inch VB substrate is less than half of that of the 4-inch LEC substrate. Figure 17 shows two-dimensional maps of micro-resistivity. The micro-potograph shows the distribution of etch pits at the same position of the VB substrate. The distribution of resistivity corresponds to the distribution of etch pit. The value of resistivity is dominated by carbon and EL2 concentrations. Concentration of carbon is not changed around the cell wall. Therefore, variation of micro-resistivity is due to the change of EL2 concentration around the cell wall.

5. Conclusions

Dislocation-free Si-doped 3-inch GaAs single crystals and 4-inch to 6-inch large-diameter semi-insulating GaAs single crystals with extremely low-dislocation-density and low-residual-strain have been developed by VB technique. We applied computer simulation technique to optimize the growth condition of GaAs single crystals to achieve the flat solid-liquid interface. Wide range control of resistivity has been achieved by developing carbon doping technique. Uniform radial profile of resistivity has been achieved by flatting the solid-liquid interface shape. Good uniformity of micro-resisitivity has been achieved by reducing dislocation density using VB technique.

Figure captions

Table 1 Growth conditions of VB technique.

Fig.1 Typical growth techniques of GaAs single crystals.

Fig.2 Si doped 3-inch GaAs single crystals grown by VB techique.

Fig.3 a 20cm length 4-inch semi-insulating GaAs crystal grown by VB technique.

Fig.4 Distributions of excess shear stress in crystals with (a) concave solid-liquid interface and with (b) flat solid-liquid interface.

Fig.5 Solid-liquid interface shape and distribution of dislocation density.

Fig.6 X-ray topographic image of a 3-inch Si-doped VB-GaAs substrate with carrier concentration of $8 \times 10^{17} cm^{-3}$.

Fig.7 Dislocation density and carrier concentration of Si-doped GaAs crystals grown by HB and VB techniques.

Fig.8 Residual strains of a 3-inch non-doped LEC-GaAs crystal with high dislocation density of 30,000 cm^{-2} and a 3-inch Si-doped dislocation-free VB-GaAs crystal.

Fig.9 Dislocation densities of (a) 4-inch and (b) 6-inch single crystals grown by VB technique.

Fig.10 Residual strains of 4-inch VB and LEC substrates.

Fig.11 Residual strains of 6-inch VB and LEC substrates.

Fig.12 Profiles of dislocation density and residual strain along the growth axis of (a) 4-inch and (b) 6-inch VB-GaAs crystals.

Fig.13 Sketches of the slip-lines on 6-inch GaAs wafers observed after MBE process.

Fig.14 Carbon concentration and resistivity of GaAs single crystals grown by VB technique.

Fig.15 Radial profiles of resistivity, carbon and EL2 concentrations on 6-inch VB and 4-inch LEC substrates.

Fig.16 Radial profiles of micro-resistivity on 6-inch VB and 4-inch LEC substrates measured at 100 micron-pitches.

Fig. 17 Two-dimensional maps of micro-resistivity on VB and LEC substrates.

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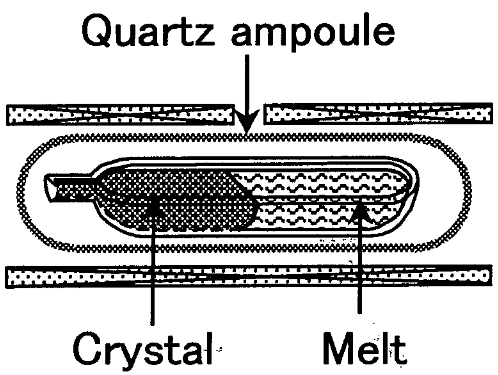
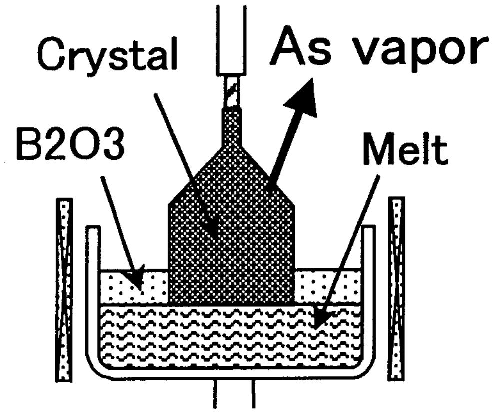
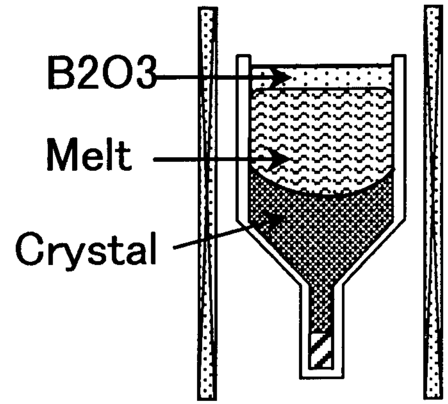
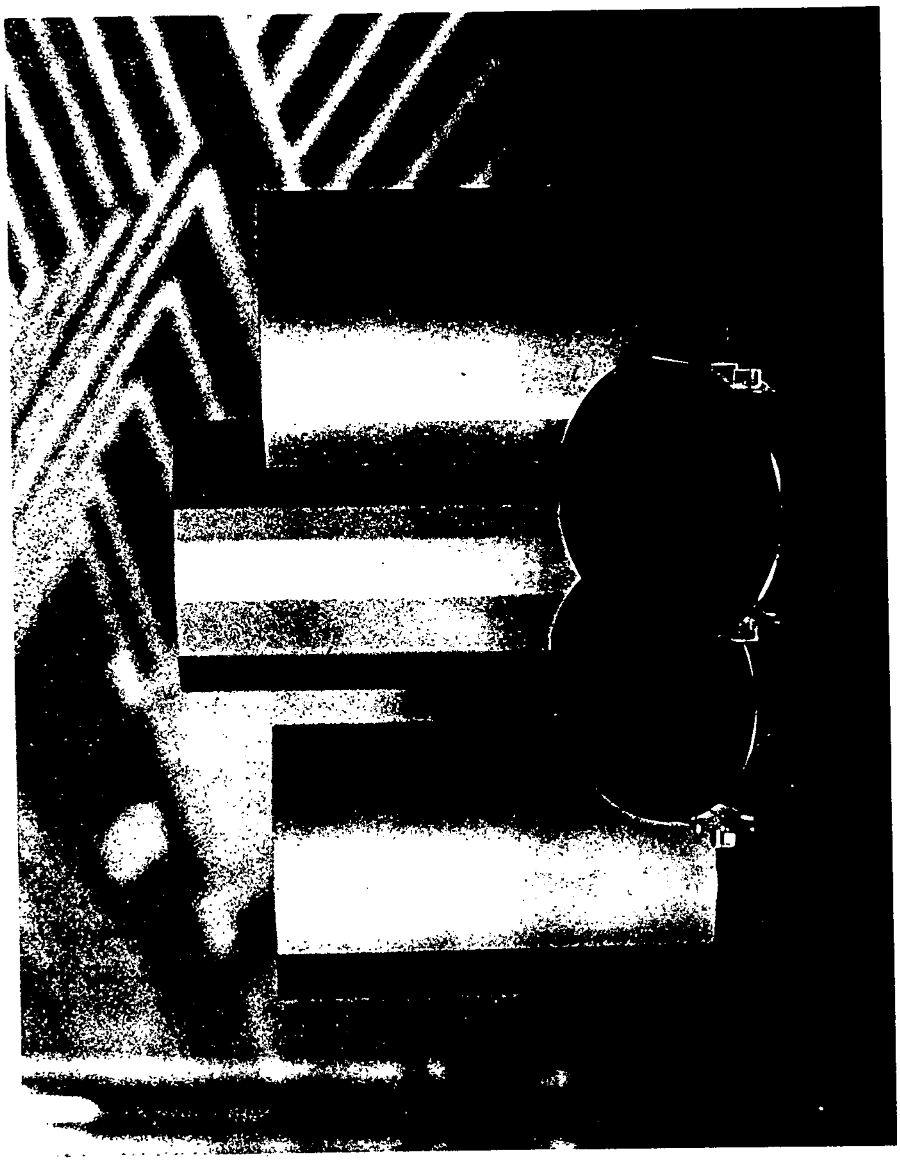
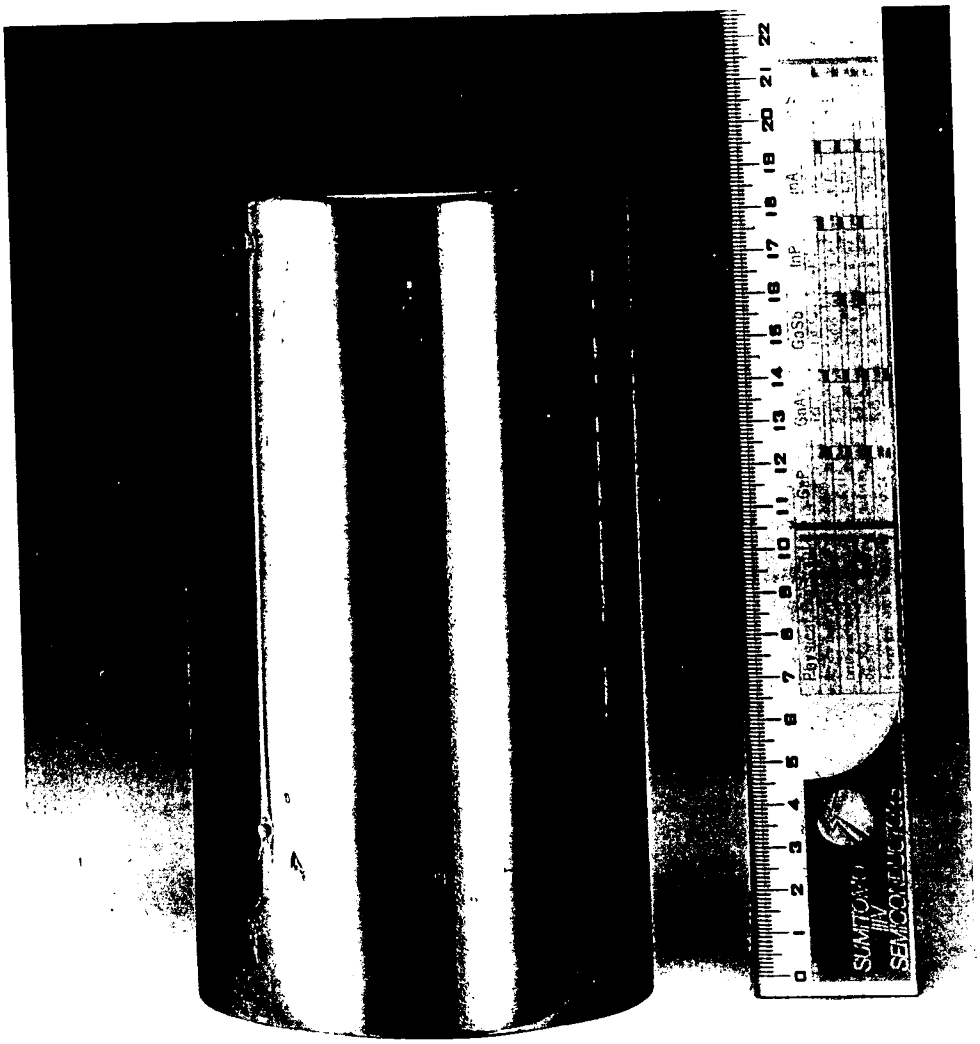
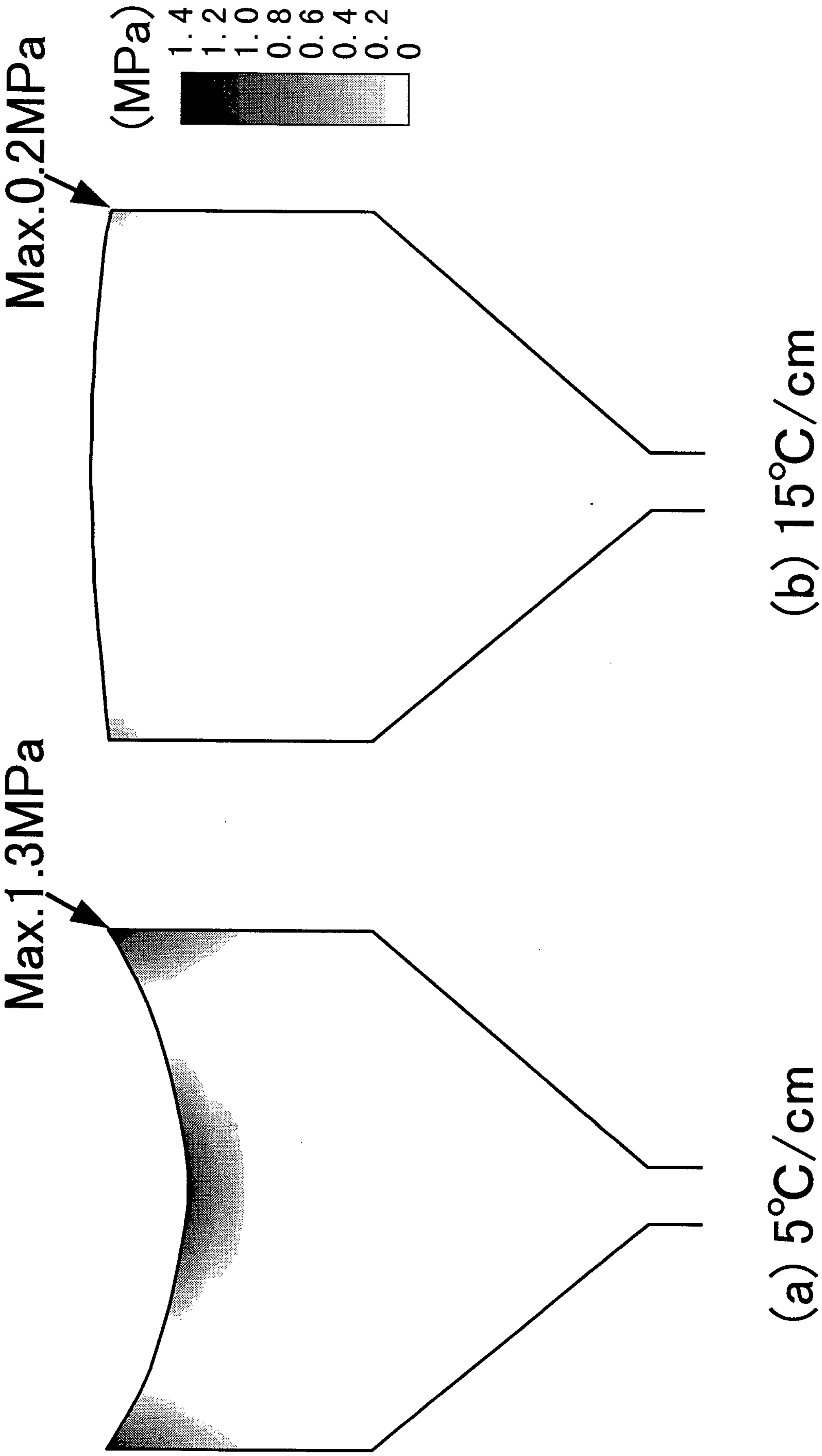
	Conductive	Semi-insulating
Dopant	Si	Carbon
Carrier concentration (cm^{-3})	$2 - 10 \times 10^{17}$	—
Resistivity (Ω cm)	—	$0.5 - 50 \times 10^{7}$
Diameter (inch)	2.5 - 3	4 - 6
Weight of the crystal (kg)	5 - 10	10 - 20
Growth speed (mm/h)	2 - 5	2 - 5

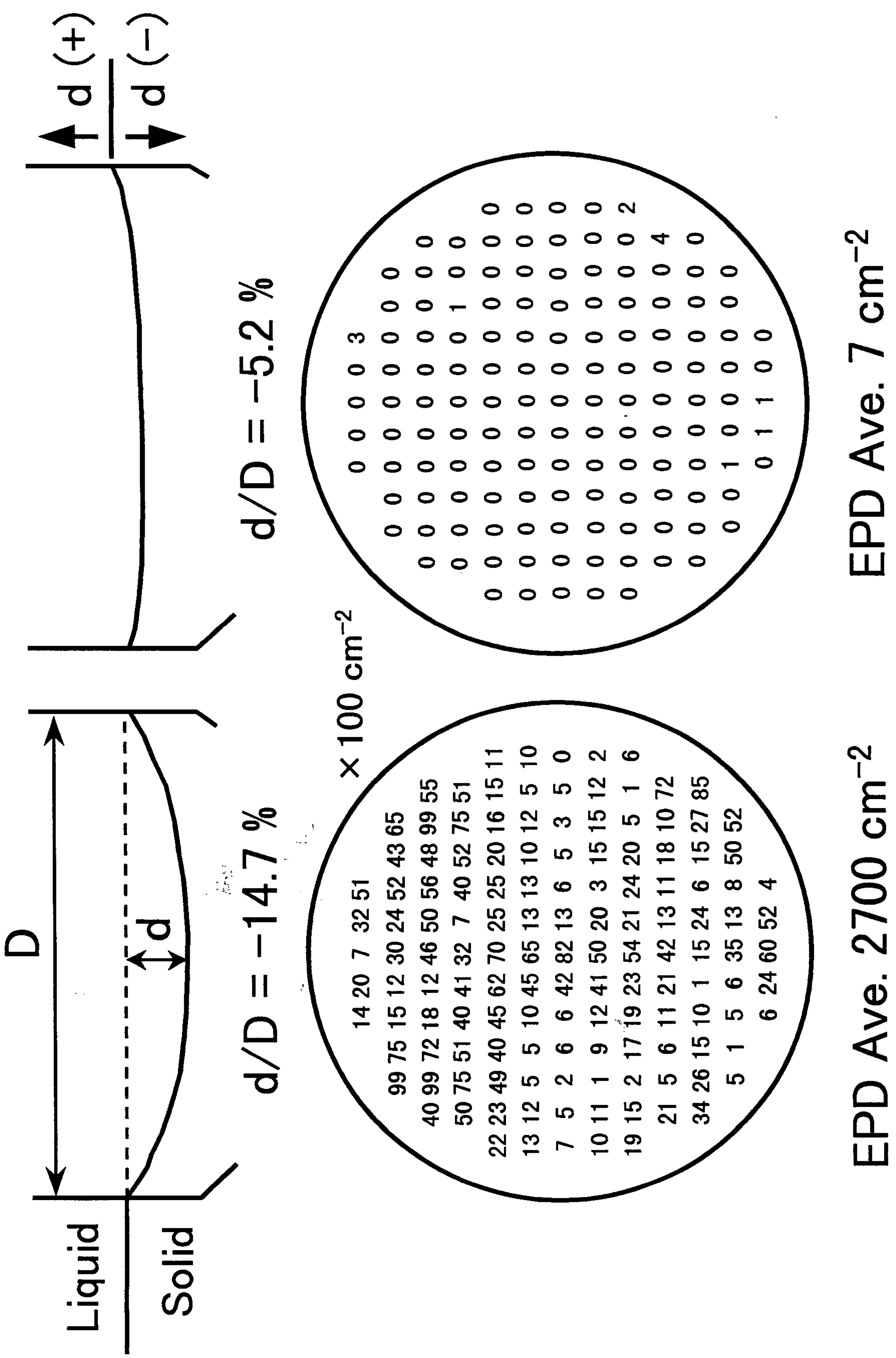
	HB	LEC	VB
			
Evaporation of arsenic	Non	A lot	Non
Temperature gradient	Low	Steep	Low
Crucible/Boat	Quartz	pBN	pBN (or Quartz)
Thermal Environment	Asymmetric	Symmetric	Symmetric
Dislocation-density Residual-strain	○ (Good)	×	○
Large diameter	× (Poor)	○	○

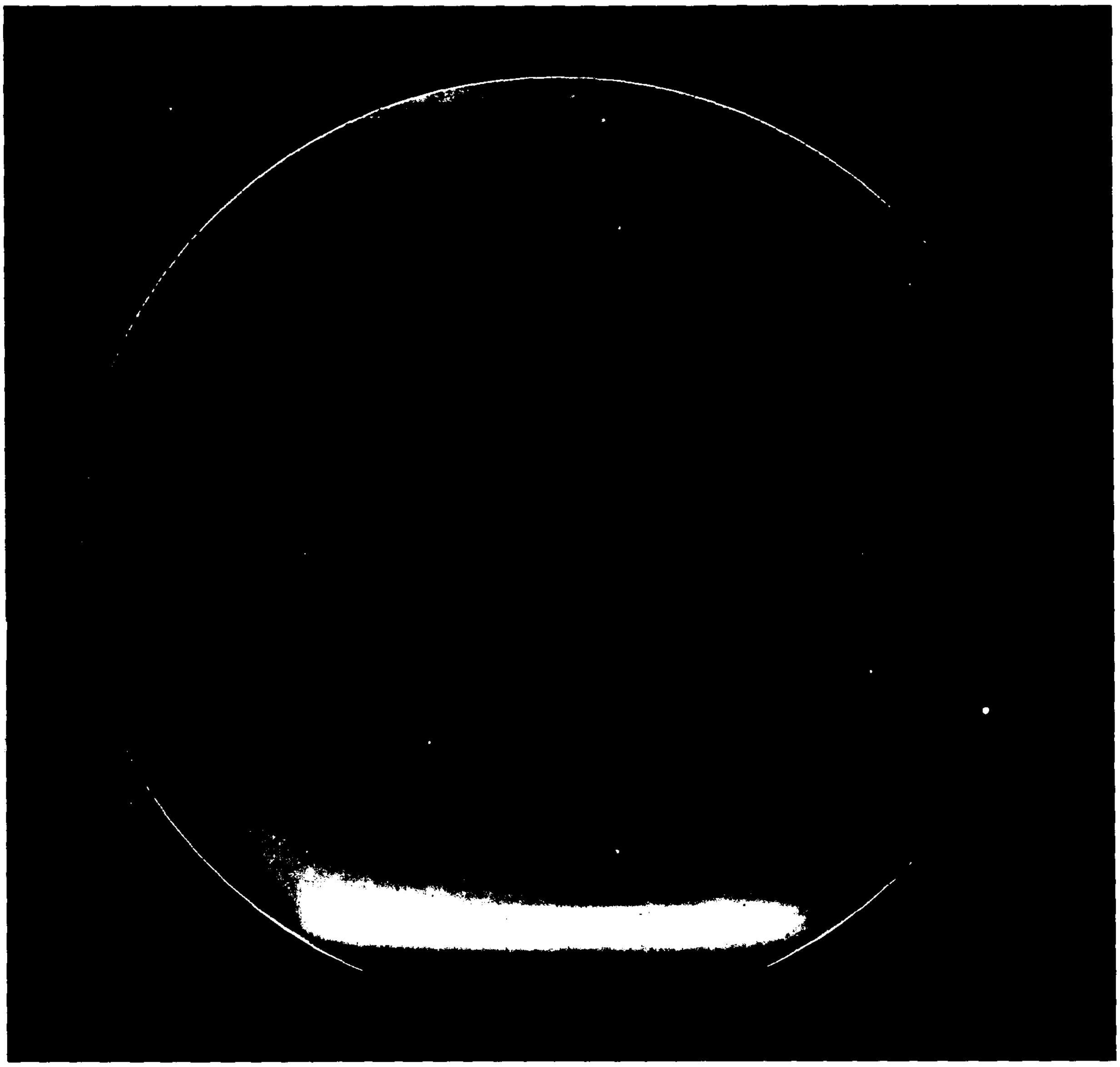


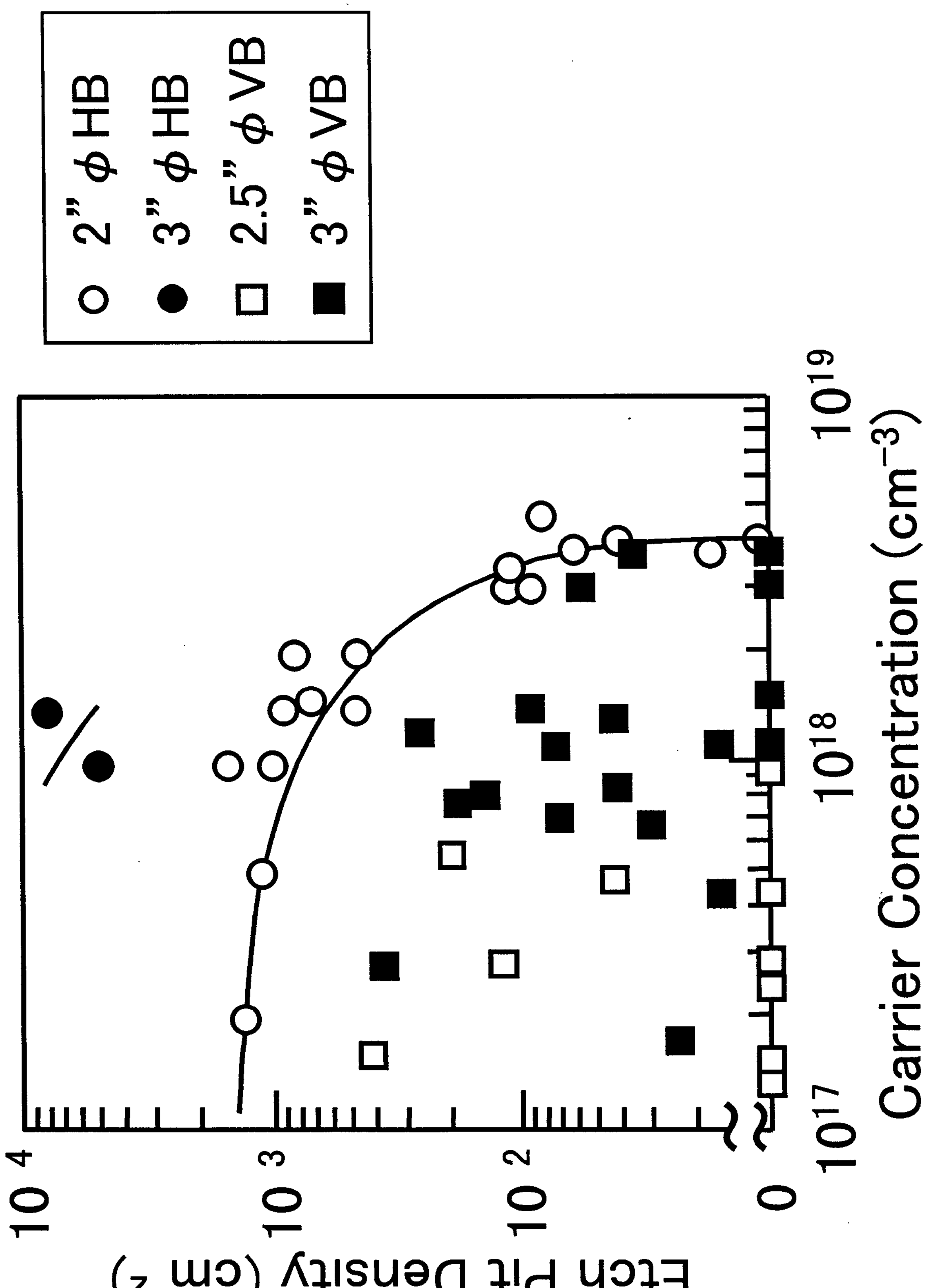
Low-dislocation-density large-diameter GaAs single crystal grown by vertical boat method



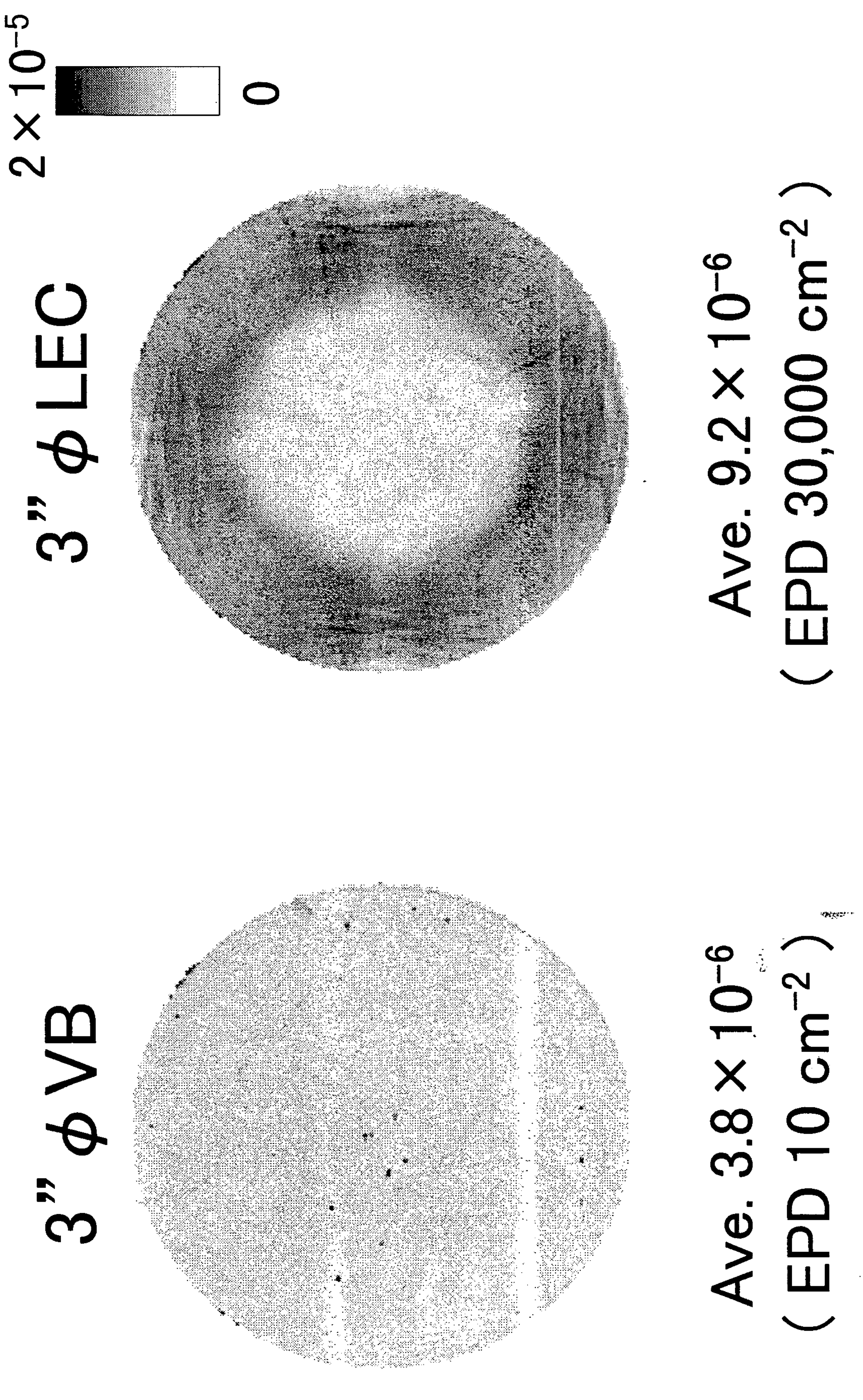

Max.0.2MPa
(MPa)
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
(b) 15°C/cm
Max.1.3MPa
(a) 5°C/cm

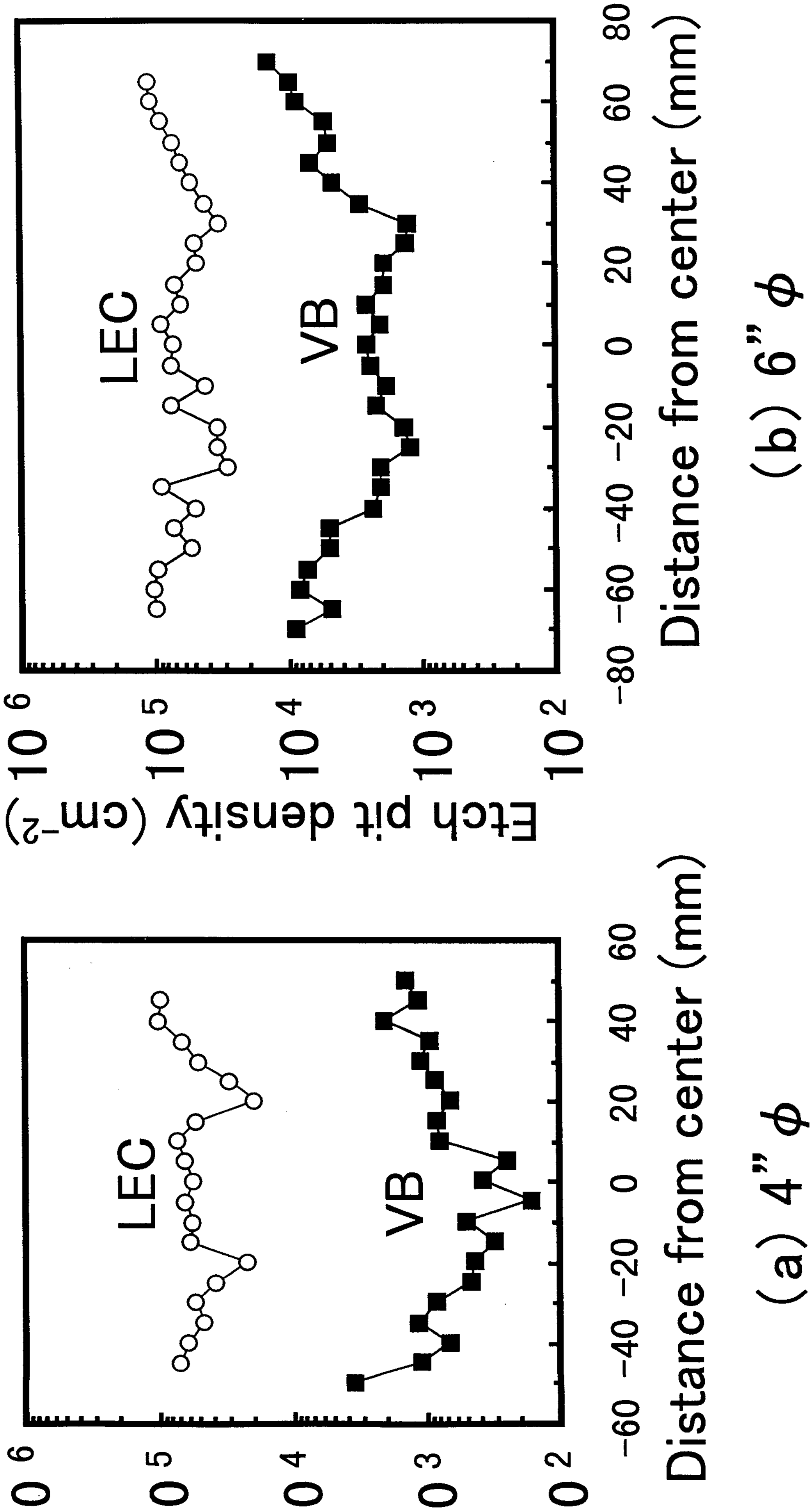

Liquid
Solid
D
d
d (+)
d (−)
d/D = −14.7 %
d/D = −5.2 %
×100 cm^{-2}
EPD Ave. 2700 cm^{-2}
EPD Ave. 7 cm^{-2}

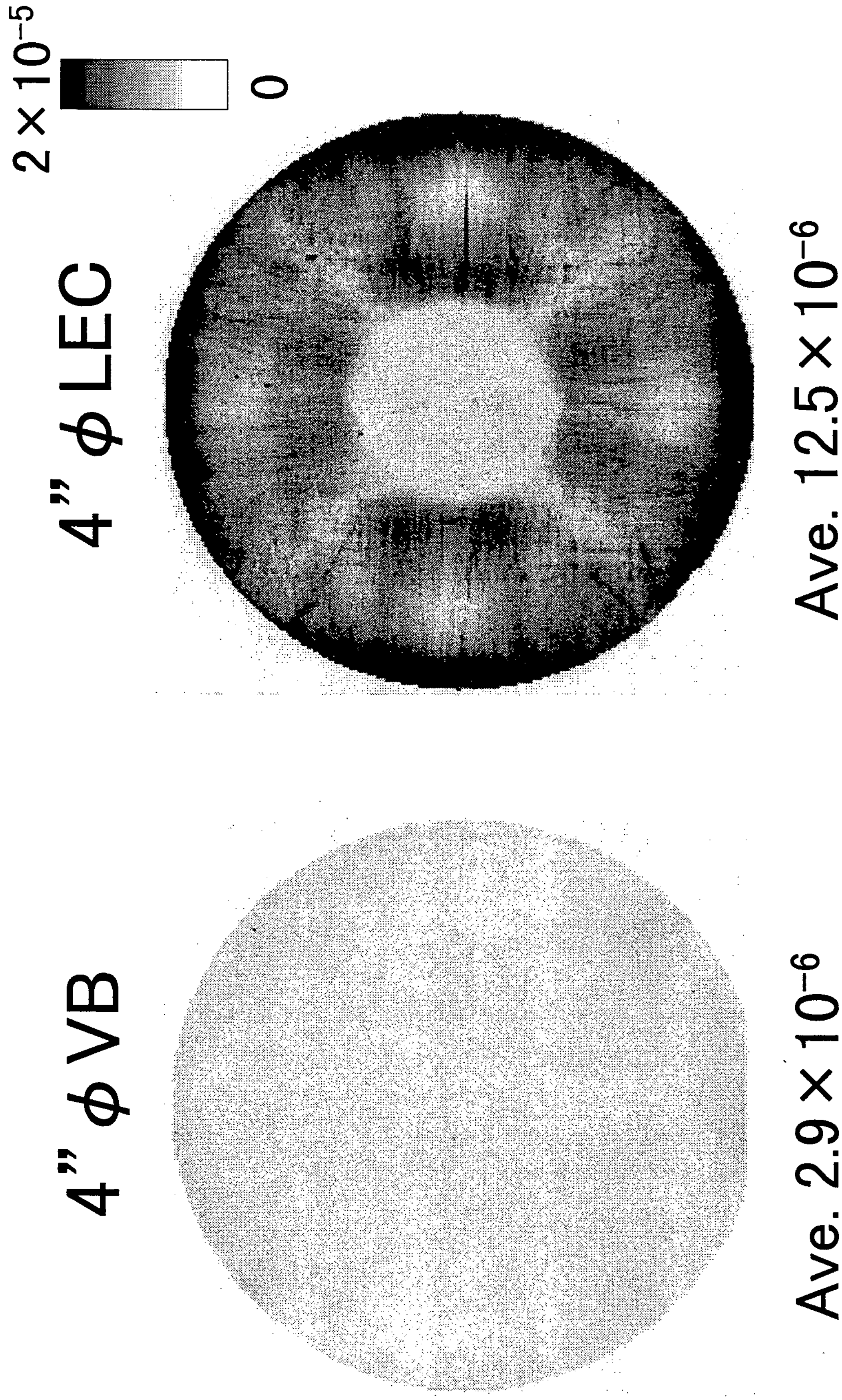


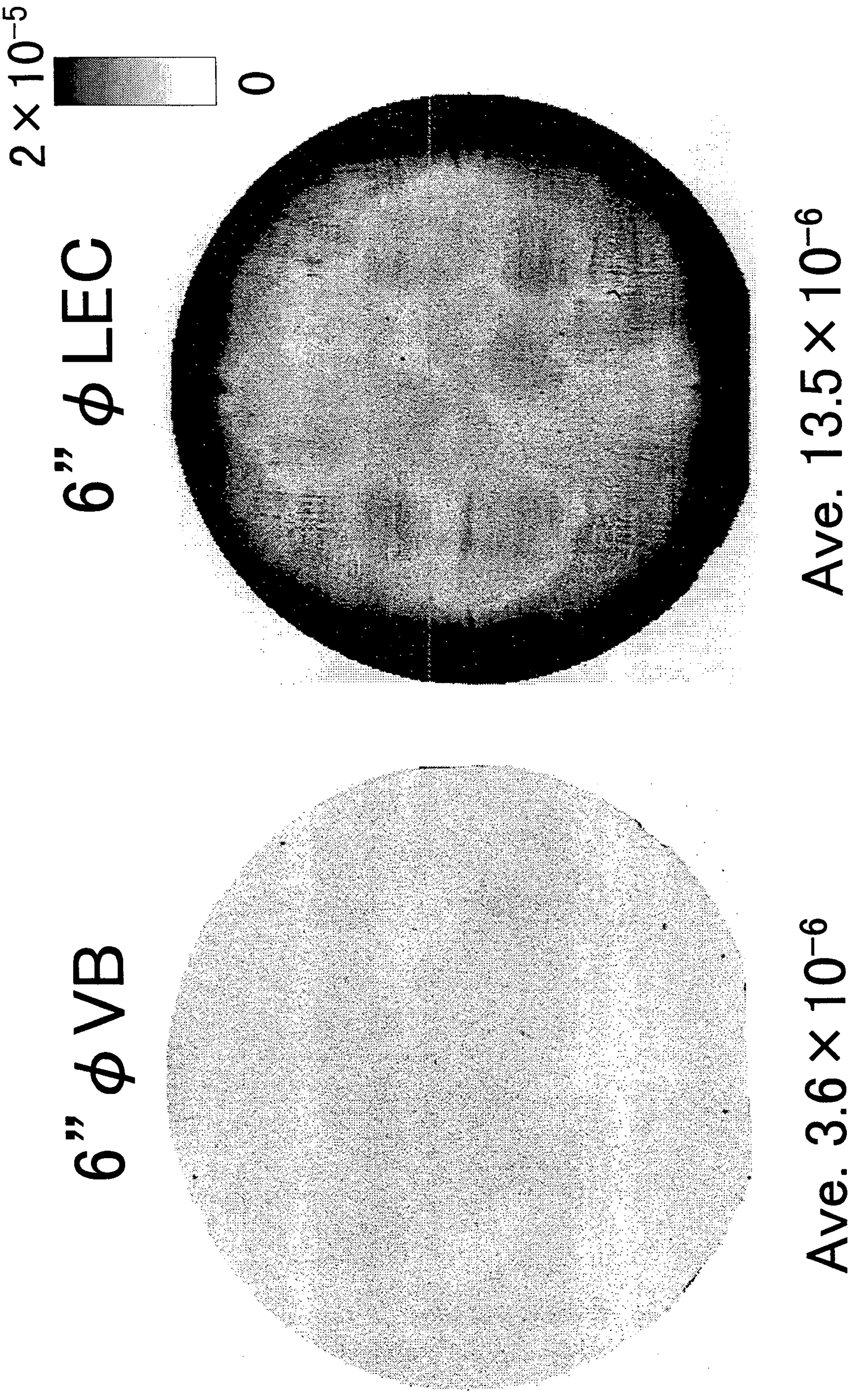


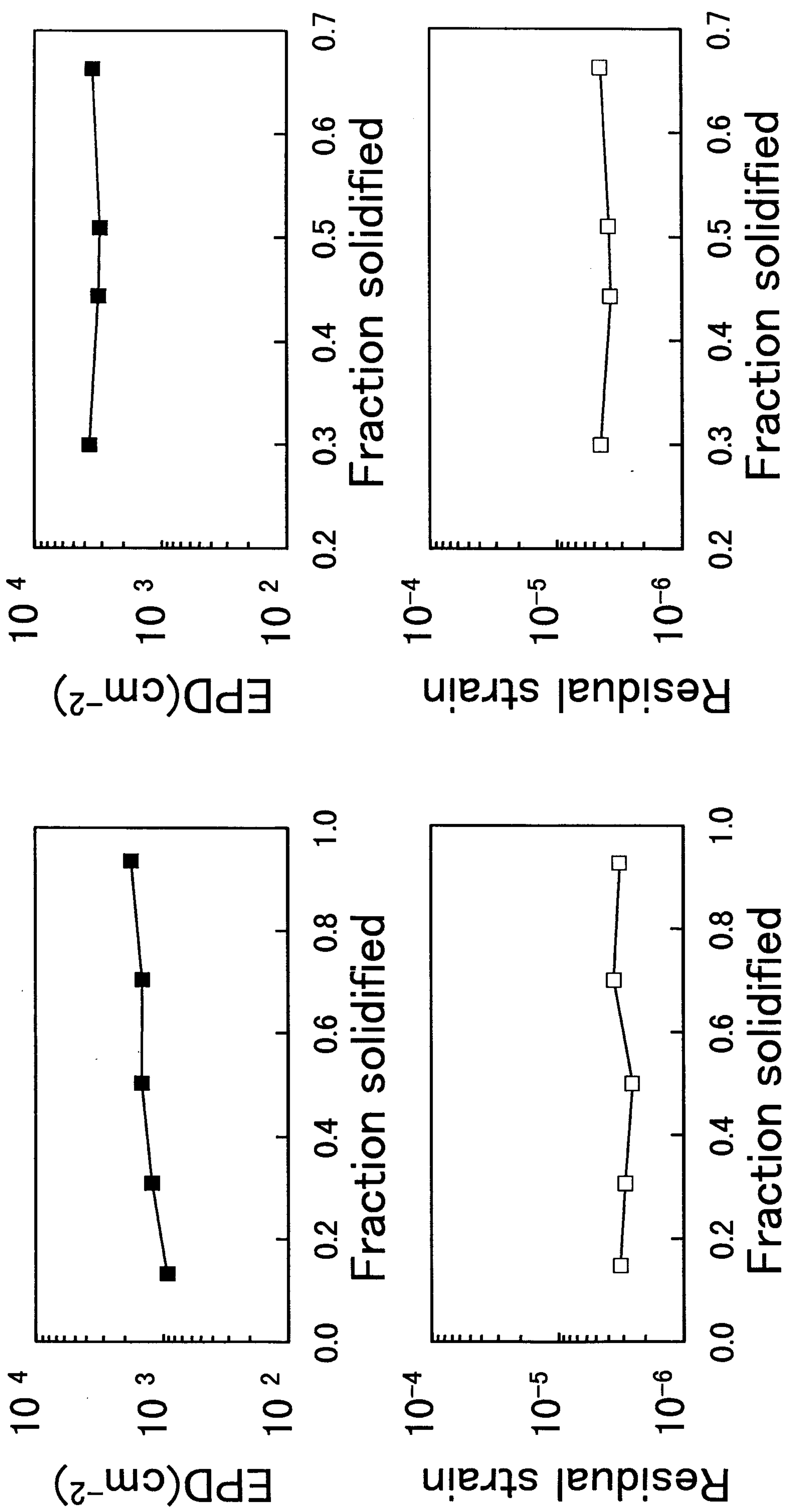
○ 2" φ HB
● 3" φ HB
□ 2.5" φ VB
■ 3" φ VB
Etch Pit Density (cm⁻²)
10 4
10 3
10 2
0
Carrier Concentration (cm⁻³)
10¹⁷
10¹⁸
10¹⁹

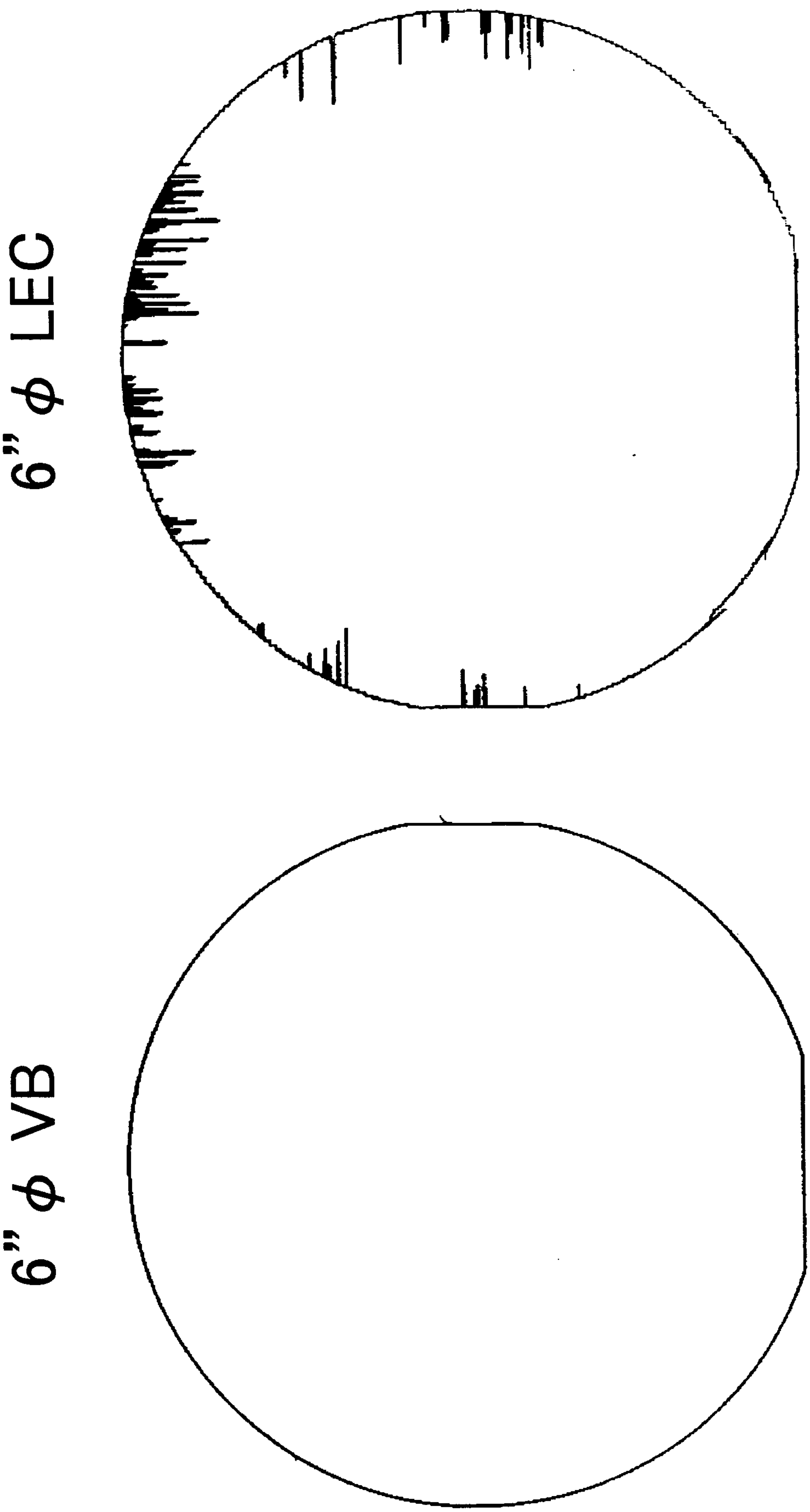

2×10⁻⁵
0
3" φ LEC
Ave. 9.2×10⁻⁶
(EPD 30,000 cm⁻²)
3" φ VB
Ave. 3.8×10⁻⁶
(EPD 10 cm⁻²)

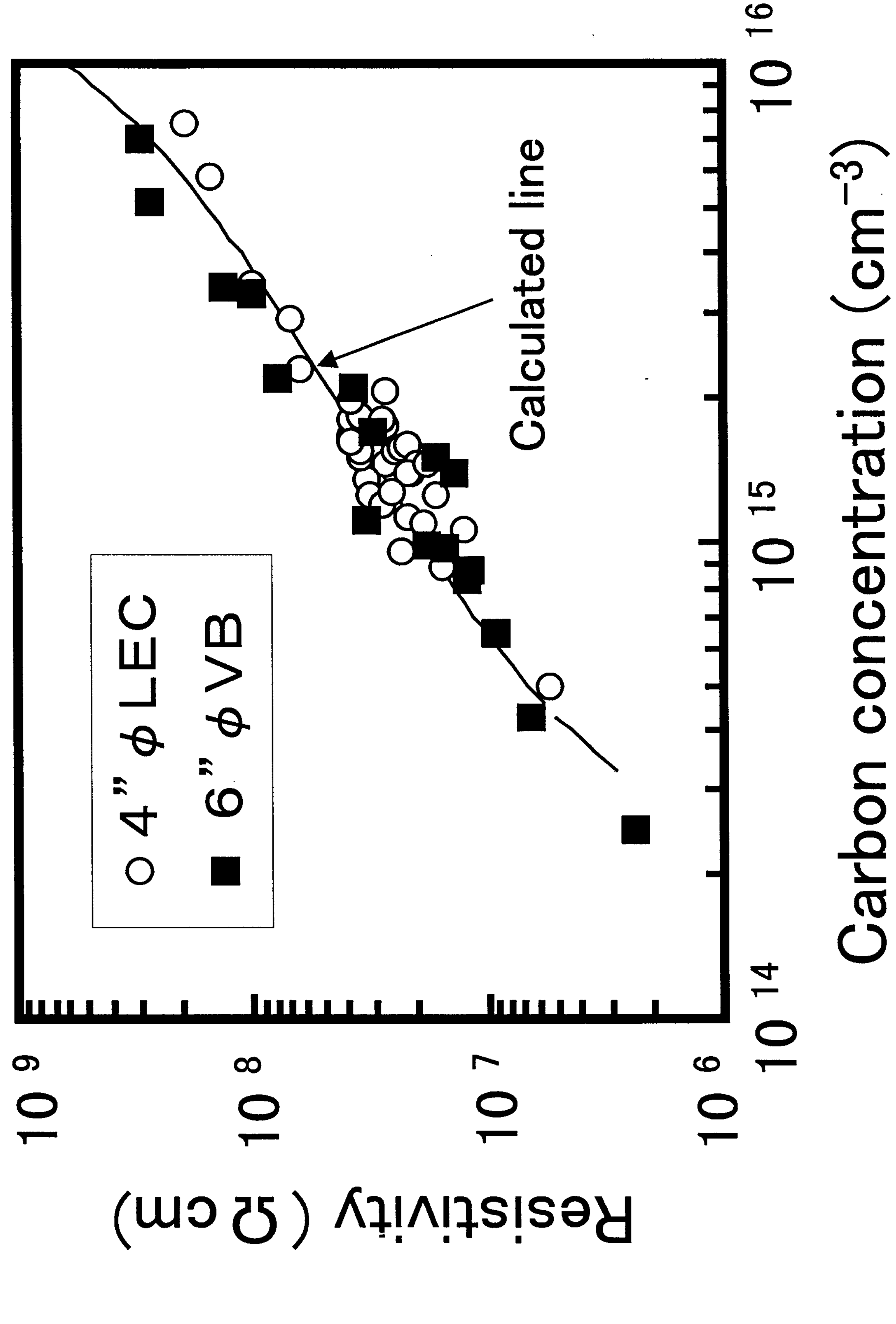

Etch pit density (cm^{-2})
LEC
VB
Distance from center (mm)
(a) 4" φ
(b) 6" φ

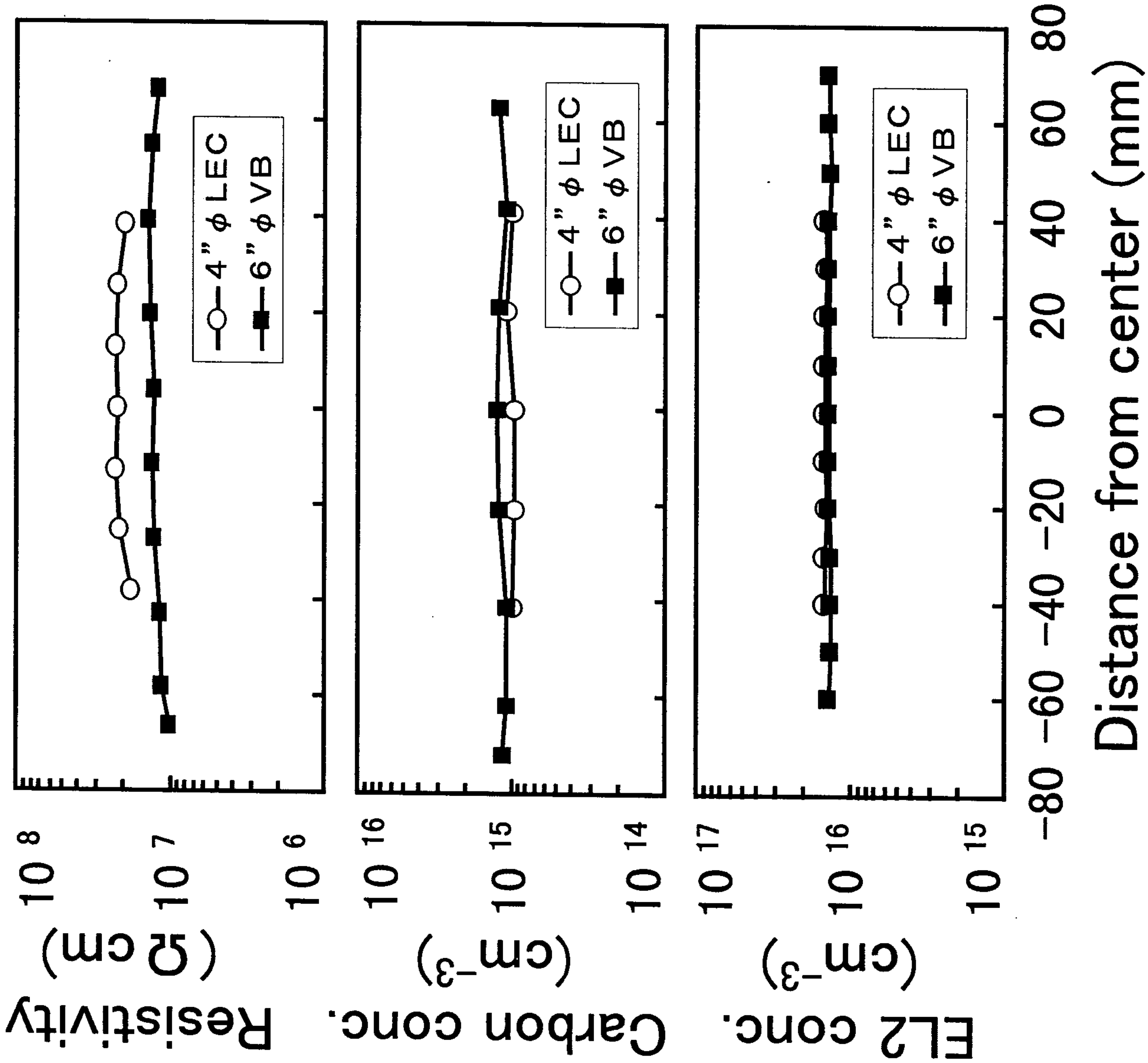

2×10⁻⁵
0
4" φLEC
Ave. 12.5×10⁻⁶
4" φVB
Ave. 2.9×10⁻⁶

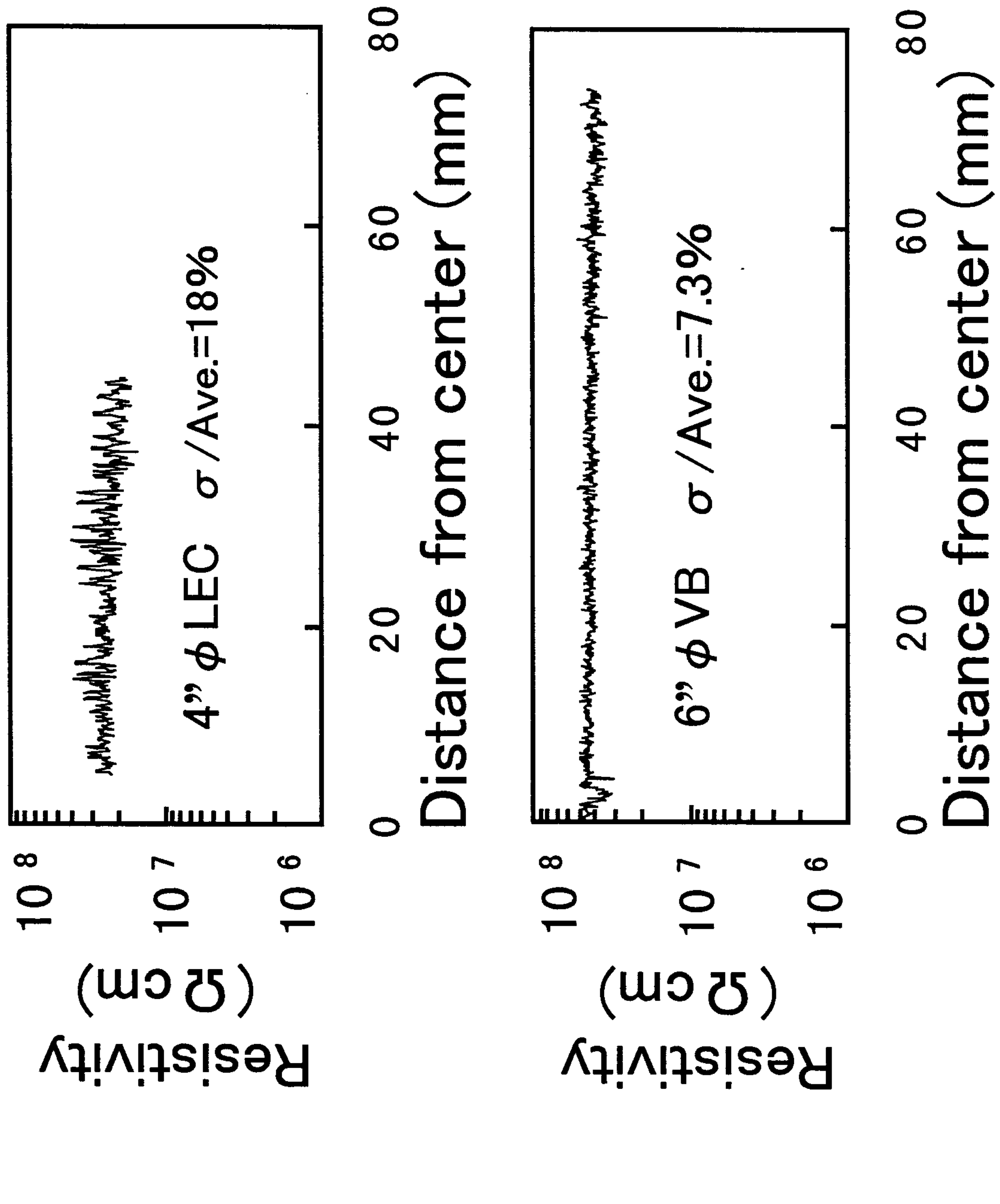

2×10⁻⁵
0
6" φ LEC
Ave. 13.5×10⁻⁶
6" φ VB
Ave. 3.6×10⁻⁶

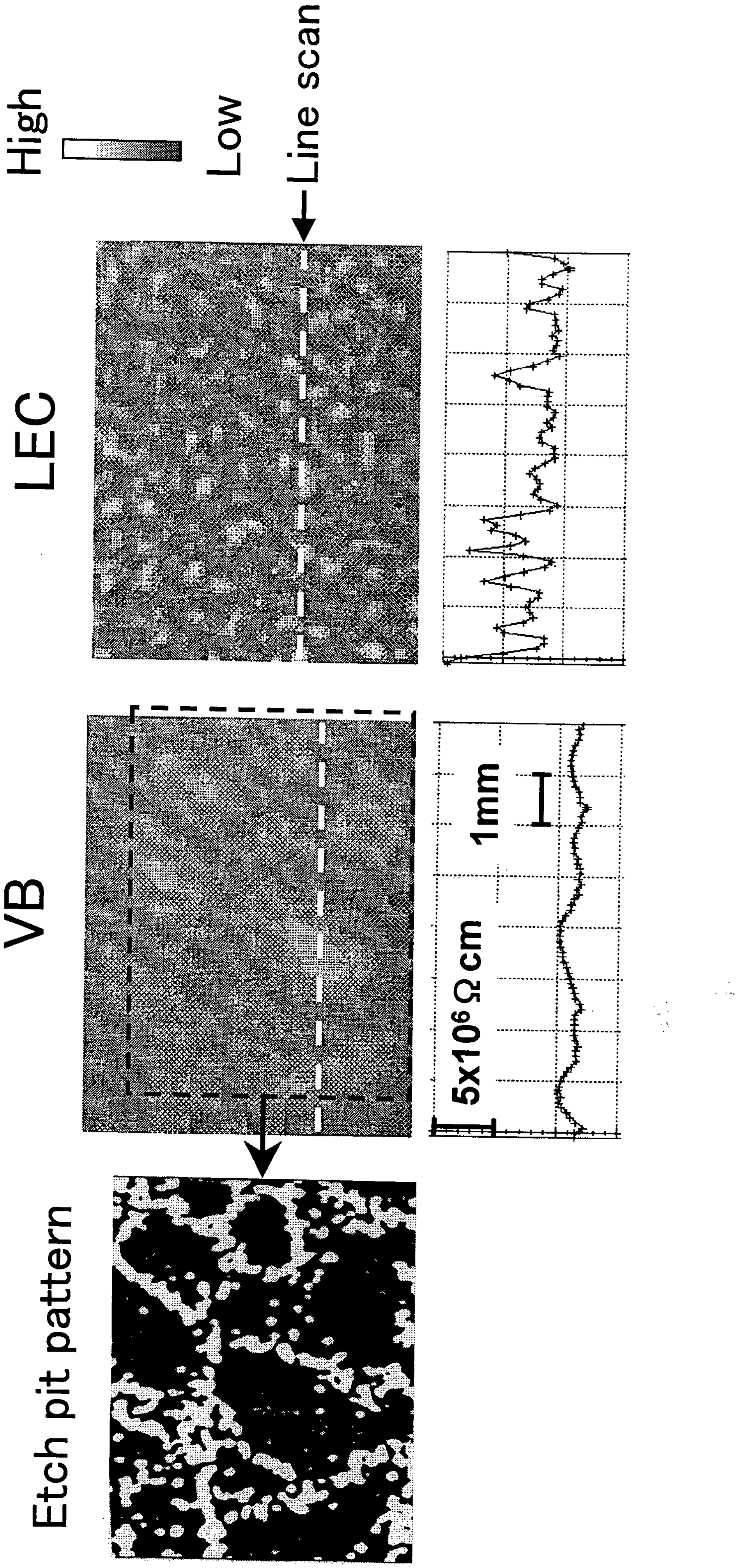

EPD(cm^{-2})
Residual strain
Fraction solidified
(a) 4" φ
(b) 6" φ


6" φ LEC
6" φ VB


Resistivity (Ω cm)
10 9
10 8
10 7
10 6
10 14
10 15
10 16
Carbon concentration (cm^{-3})
○ 4" φLEC
■ 6" φVB
Calculated line


Resistivity (Ω cm)
Carbon conc. (cm⁻³)
EL2 conc. (cm⁻³)
4" φ LEC
6" φ VB
Distance from center (mm)
−80 −60 −40 −20 0 20 40 60 80


4" φ LEC σ/Ave.=18%
6" φ VB σ/Ave.=7.3%
Resistivity (Ω cm)
10 8
10 7
10 6
Distance from center (mm)
0
20
40
60
80


High
Low
Line scan
LEC
VB
1mm
5x10⁶ Ω cm
Etch pit pattern