Balancing Rules in the Semiconductor Fabrication Line

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ABSTRACT

In the semiconductor manufacturing, the cycle time of the fabrication process is relatively long because of difficulties of the process and complexity of the lot flow. In general cycle time is proportional to the WIP level since the more the WIP the longer waiting time in queue. Therefore controlling the WIP is essential in the fabrication line in order to reduce the cycle time. This paper is concerned with scheduling the steps on the bottleneck machines of the fabrication line, which leads to significant improvement on the throughput and the utilization of the equipment as well as reduction of the cycle time and, hence WIP. Management to make the balanced line is critical in these two objectives. LP formulation for the scheduling was presented, and several heuristic scheduling policies for the bottleneck were suggested to keep the balance and to maximize the throughput of the wafer production. Those policies were tested in the simulated model, which was designed and developed using Delphi for the semiconductor manufacturing line. One of policies we suggested was implemented in the real semiconductor manufacturing line, and it was reported that there was significant improvement in the cycle time reduction and in the throughput of the wafer production.