Sym. G : Electro-packaging

ADVANCED PACKAGES- Ⅱ

E-THU-11

Wafer-Scale CSP USING WAFER SCALE ASSEMBLY TECHNOLOGY

D.B. KANG, J.H. YOON, B.J. HAN (R&D Center, Anam Semiconductor Inc., 280-8, 2ga, Sungsu-dong, Sungdong-gu, Seoul, Korea)

Emerging market drive in packaging industry is Chip Size Package(CSP) that is smaller & lighter than conventional IC packages for the portable & hand held electronic devices. Anam Semiconductor Inc. have developed and is currently marketing several types of CSPs for different applications. Even though many other assembly houses have announced many kinds of CSPs, most of the assembly concept is traditional one using strip or lead frame based assembly, wire bonding & molding technologies except a few CSPs. We are announcing in this paper the new CSP named Wafer Scale Chip Size Package(WSCSP) and its wafer scale assembly process. This package is utilizing wafer scale batch process to achieve maximum productivity with a minimum wastage of material and more simple process than conventional or newly developed other CSPs. This package is believed to be most adoptable to a mature memory devices to build a true chip size form factor. Standard foot prints of SRAM, DRAM and flash memory have been achieved using a wafer scale ball formation. This cost effective, smallest possible package is ready for manufacturing to meet the market needs.

E-THU-12

NOVEL OPTICAL COUPLING TECHNIQUES FOR BIDIRECTIONAL TRANSCEIVER MODULE, G. C. JOO, S. H. LEE, K. S. PARK, N. HWANG, M. K. SONG, H. M. KIM, K. E. PYUN (Semiconductor Division, ETRI, Taejon, 305-350, Korea)

To overcome drawbacks and limitations of planar lightwave circuit based modules for bidirectional communications, such as the demand for several chips and in consequence more packaging efforts, we have recently developed a novel optical coupling technique using our discernable 155 Mbps bidirectional laser chip. Since the chip is structured as that a *pin*-photodiode is monolithically integrated on top of an ordinary laser diode's waveguide, the optical coupling is focused only on the alignment of a chip with a fiber, without the requirement of any waveguide device. To make optical couplings to laser diode and photodiode simultaneously by a single line of fiber, we have designed an unusual coupling structure by using the fiber of which cleaved surface to be 55° inclined to the optical axis, and the index controlling medium having its refractive index of ~1.3. The bidirectional chip has been flip-chip bonded and the fiber passively aligned on a V-groove of the same substrate of 2.5x1.3 mm^2 in size. Even with this extremely small and simple scheme for a bidirectional optical coupling, we could obtain the output power of –5 ~ –10 dBm and responsivity of < –30 dBm, which are fully satisfactory to the STM-1 level telecommunications.

E-THU-13

SELF-ALIGNED FABRICATION OF SILICON V-GROOVE AND FLIP-CHIP SOLDER BUMP PADS USING METAL PROTECTION METHODS DURING KOH SILICON ETCHING, S. H. LEE, G. C. JOO, K. S. PARK, M. K. SONG, H. M. KIM, K. E. PYUN (Semiconductor Division, ETRI, Taejon, 305-350, Korea)

Mounting of fiber on anisotropically etched silicon V-groove and flip-chip solder bonding of laser chip are two key techniques in realizing passive-aligned fiber-to-laser coupling on a silicon optical bench. Aqueous KOH solution commonly used for V-groove etching is known to attack most metal films. However the existence of V-grooves prior to the solder bump formation makes the surface morphology so rugged to perform a conventional photolithography processes, which in turn results in a poor resolution and accuracy. In this paper, we report a method for silicon optical bench fabrication to overcome such a situation. It comprised of two major steps; i) opening V-groove etch windows and solder bump pads simultaneously by one photolithography step, ii) protecting the solder bump pads consisted of under bump metallurgy (UBM) and silicon nitride solder dam from the KOH solution. The protection is accomplished by optimizing the UBM composition and solder dam thickness. By employing these techniques, we have reduced the registration errors between the V-groove and solder bumps to be less than ±0.5 μm.

E-THU-14

AN OPTIMAL MODELING STUDY OF POWER PACKAGE, C.H. LEE, S.G. LEE, E.S. SOHN and S.M. KIM (Design & Simulation Team, R&D Center, Anam Semiconductor Inc., 280-8, Sungsu-2ga, Sungdong-Gu, Seoul, Korea)

A modeling study of one of the power packages, PQ2, is performed in an optimal way that includes the integrated analysis from heat transfer, thermal stress, mold flow, and electrical aspects. PQ2 is well known to be one of the packages that have excellent thermal performance. It has an exposed heat sink of which external surface is alumina blasted aiming at electrical insulation. Peeling the alumina blasted layer at deflash, solderplating and detaping processes, however, may be open to electrical problems. One of the possible solutions for this is to reduce the thickness of heat sink in such a way that even the exposed area of heat sink can be overmolded.

Then several questions related to overmolded thin heat sink may be raised: will thermal performance still be maintained, how about the possibility of void in molding process, how will thermal stress be, what about the change in electrical properties and so on. This kind of questions should be dealt with through an approach that offers the total solution. In this paper we will describe the plausible solution associated with each analysis mentioned above.

This sort of a new package has to undergo all real processes and get the confirmation of their stability, which will be started in fairly near future.