Sym. B : Compound Semiconductors for Electronic & Photonic Devices

Ⅱ-Ⅵ & RELATED MATERIALS

D-THU-22

ATOMIC LAYER DEPOSITION OF CALCIUM SULFIDE THIN FILMS IN TRAVELING WAVE REACTOR, SUN JIN YUN, Y. S. KIM, and K. -S. NAM (Semiconductor Technology Division, Electronics and Telecommuniçations Research Institute, Yusong P. O. Box 106, Taejon, Korea 305-600)

Calcium sulfide(CaS) has been one of the most attractive host materials of phosphor layer of electroluminescent devices due to a wide band gap and an appropriate ionic radius match with luminescent center ions. In the present work, the depositions of polycrystalline CaS and rare earth ions-doped CaS on amorphous Al_2O_3 film were studied using traveling wave reactor atomic layer epitaxy(ALE). ALE is a self-limiting growth technique utilizing surface saturation. The precursors used in the ALE process were bis(2,2,6,6-tetramethyl-3,5-heptanedionato) calcium and H_2S. The results indicated that stoichiometric CaS films could be grown by ALE. The dependences of crystallinity, surface morphology, and growth rate of CaS were investigated on growth temperature. The growth rate increased from 0.3 to 0.45 Å/cycle as increasing the growth temperature from 300 to 390°C. The CaS films grown using ALE had a distinctive surface structure showing well-developed cubic structure. The x-ray diffraction data also illustrated dominant (002) diffraction of cubic CaS. The present work indicated that the crystallinity and the morphology of CaS films does not strongly depend on the growth temperature but on the dopant concentration.

D-THU-23

ZnTe:Cu BACK CONTACT FOR CdS/CdTe SOLAR CELLS, DONG-IL CHOI and DONGHWAN KIM (Div. of Mat.Sci. & Eng., Korea Univ., Seoul 136-701, Korea)

Thermal evaporation of ZnTe films was investigated as a back contact material for CdS/CdTe solar cells. Cu-doped ZnTe layers (0.2μm) were deposited either on glass or CdS/CdTe substrates. Post-deposition annealing was performed at 200, 300 and 400°C for 3, 6 and 9 minutes. Bandgap of 2.2eV was measured for undoped ZnTe but a lower value by 0.5eV was measured for Cu-doped ZnTe. The resistivity of as-deposited ZnTe (10^5~$10^6\Omega$-cm) decreased by more than five orders of magnitude as Cu concentration increased from 2 to 14 at. %. There was not a noticeable change in resistivity with increasing annealing temperature. Undoped ZnTe showed a preferred orientation in cubic (111) regardless of annealing temperature up to 300°C whereas films annealed at 400°C revealed hexagonal (101) peak as well. We also found that Cu-doped ZnTe had some of Cu_2Te peaks with cubic peaks that could debilitate the effect of Cu injection. With increasing the thickness of undoped ZnTe from 0.13μm to 0.2μm, open-circuit voltage (V_{oc}) and fill factor (FF) of the solar cells significantly increased from 0.66V to 0.72V and from 36.8% to 53.7%, respectively. Solar cell efficiencies up to 10% ~12% were achieved as a result of this study.

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Sym. G : Electro-packaging

ADVANCED PACKAGES- I

E-THU-01

A NOVEL BGA PACKAGE FOR RF APPLICATIONS

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It has recently become evident that there are many important design and performance advantages to be gained by using a flip-chip silicon-on-silicon FBGA architecture for RF applications. As an example, this paper will describe the structure and assembly of a GSM module in which an RF transceiver chip was flip-chip mounted onto a circuited silicon substrate which incorporated embedded capacitors, inductors and resistors. The resulting silicon-on-silicon "tile" structure, which included all of the RF sensitive nodes, was then enclosed in a cavity down, FBGA package. Electrical tests of the resulting assembly showed an exceptionally clean RF resonance peak with none of the spurious resonances observed during tests of a transceiver IC chip of the very same design when enclosed in a conventional leaded package and surface mount soldered to a conventional PWB mother board. In addition, this unique FBGA structure allows for the design and manufacture of optimized RF transceivers that can be as thin as the tile alone, i.e. only a hair's width thicker than twice the thickness of a thinned silicon wafer.

E-THU-02

LOW COST & HIGH RELIABILITY MCM-D SUBSTRATE UNIT PROCESS DEVELOPMENT, J. S. KIM, H. S. KO, S. D. CHO, H. K. YOON and K. W. PAIK (Dept. of Mat. Sci. & Eng., KAIST, Taejon 305-701, Korea)

The MCM-D substrate manufacturing technology has been developed and each unit process was investigated to ensure the low cost and high reliability MCM-D substrate. While the majority of reports in the literature have focused on the spin coating of polyimide to fabricate a dielectric layer, this paper mainly focuses on the lamination process which use heat and pressure to bond the composite film to the substrate. The interlayer adhesion strengths between various polymer dielectric films and silicon substrate as well as the surface chemistry of the interfaces were investigated. TaO_x thin film capacitors were sputter deposited on polymer films in MCM-D substrate and their properties were measured and analyzed. The important issues in via formation process like etch rate and sidewall angle control, residues control, and Al pad damage as a function of rf power, and plasma gas ratio and pressure have been studied using oxygen RIE (Reactive Ion Etching). Thermo-mechanical stress in MCM-D substrate is an important reliability and fabrication issue. A simpler analytical model which predicts a stress contribution from each individual layer during MCM-D substrate fabrication is proposed and verified by computer simulation as well as experimental results.