A-THU-05

FORMATION MECHANISM OF EPITAXIAL $CoSi_2$ IN *EX-SITU* Ti-CAPPING OME PROCESS, Gi Bum Kim, Joon Seop Kwak, Hong Koo Baik, Dept. of Metallurgical Engineering, Yonsei Univ., Seoul, Korea ; Sung Man Lee, Dept. of Materials Engineering, Kangwon National Univ., Chunchon, Korea

Epitaxial $CoSi_2$ has attracted much attention as device scales down, because it has a very low resistivity, less overgrowth on oxide sidewall, good thermal stability, and no highly resistive compounds with B and As dopants. Recently, OME(Oxide Mediated Epitaxy) process was proposed as a new method for obtaining epitaxial $CoSi_2$ of good quality. However, it is not applicable to the actual production line, because the OME process involves repeated *in-situ* deposition and annealing.

In this study, we adopted Ti-capping for the OME process to obtain a $CoSi_2$ layer of thickness applicable to ULSI devices in a single process. The crystallinity of the $CoSi_2$ layer was very different depending on the Ti-capping thickness. We have suggested the formation mechanism responsible for such a difference.

A-THU-06

A STUDY ON THE UNSTABILITY OF CONTACT RESISTANCE IN W(tungsten) POLYCIDE BIT LINE TO W POLYCIDE WORD LINE CONTACT

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As the design rule reduces to below quarter-micron range, polycide gate and bit line has been commonly used in memory devices. When the polycide to polycide contact is formed, large contact resistance is usually observed. Obviously, such an increase of contact resistance is a big obstacle for next generation DRAMs, as it not only increases the RC time delay, but also reduces the low Vcc margin.

In this study, we analyzed the contact interface in W polycide bit line to W polycide word line contact by HRTEM equipped with μ-EDS, XRD, and ESCA characterization. The results from TEM and μ-EDS investigation of contact interface showed a residual layer was formed at the contact interface during contact etch process. Thermodynamic consideration revealed the reaction of plasma gas with word line WSix layer during contact etch process mainly responsible for the formation of residual layer at the contact interface. The electrical analysis of contact with chain and Kelvin resistance measurement suggested the residual layer acted as a barrier to the electron flow through the contact interface and hence minimized the channeling current.

A-THU-07

EFFECT OF VACUUM ANNEALING OF MOCVD TiN ON THE DIFFUSION BARRIER PROPERTY, JAEGAB LEE, HEUNGLYUL CHO(Dept. of Metallurical Eng. Kookmin Univ.), EUNGU LEE, KIBUM KIM

We have prepared TiN films using TDMAT as a single source. The effects of vacuum annealing of TDMAT-source TiN on its diffusion barrier property in Cu/TiN/Si structure has been investigated. Annealing of the films in vacuum continued to reduce the resistivity with anneal temperature and to make the films stable in air. According to XRD analysis, the TiN films remained amorphous after high-temp annealing at 750℃. From these facts, it was understood that annealing of the films in vacuum increased the film density, leading to the reduction in resistivity. This was consistent with the increase in density of the films annealed in vacuum, which was identified with the combined results obtained using XTEM and RBS. In addition, annealing of the films in vacuum caused the incorporation of oxygen into the TiN films. 2×10^{-6} Torr of H_2O in vacuum was expected to diffuse into the porous TiN films, increasing the oxygen content in the films. The barrier properties of TDMAT-source TiN films for Cu metallization was enhanced by vacuum annealing of the films prior to Cu deposition. It was also noted that during high temp annealing Cu/TiN/Si in H_2, Cu diffused into Si-substrate and Si atoms diffused into Cu at the same time, causing the overgrowth of silicon particles on the Cu surface.

A-THU-08

ELECTRICAL PROPERTIES OF COPPER THIN FILMS PREPARED BY MOCVD, N.I. CHO, D.I. PARK, and H.G. NAM(Dept. of Electronics Eng., Sun Moon University, Chungnam, 336-840, Korea), C.K. KIM (Dept. of Electrical Eng, Soonchenhuang Univ., Chungnam 336-745, Korea)

For the applications in the VLSI metallization processing, copper thin films have been prepared by metal-organic chemical vapor deposition (MOCVD) technology on TiN/Si substrates. The films have been deposited with varying the experimental conditions of substrate temperatures and copper source vapor pressures. The films are annealled in vacuum after the deposition, and the dependence of the annealing effects to the electrical properties of the films were analyzed. The crystallinity and the microstructures of the films were observed by transmission electron microscopy, the electrical resistivity was measured by 4-point probe. The best electrical property of the films was obtained by the post-annealing at above 350C for the sample prepared at 180C of the substrate temperature. Other material properties of the films, such as surface roughness, grain size, and crystallinity will also be presented. The relations between the electrical and material properties are discussed.