P-019

A STUDY ON THE FORMATION AND IT'S CHARACTERISTICS OF SOD STRUCTURE, Y. S. LEE[1], K. M. LEE[2], J. D. Ko[1], and C. K. Choi[1](Dept. of Physics[1], Dept. of Electronic Eng[2]., Cheju National Univ., Cheju 690-756, Korea), Y. J. Baik(Div. of Ceramics, KIST, Seoul 130-650, Korea)

The properties of diamond with excellent thermal conductivity and electrical insulation can be applicable to the silicon device of SOD (silicon on diamond) structure. High quality polycrystalline diamond films were deposited on (100) silicon substrate by microwave plasma CVD method using CO, B_2H_6, H_2 and O_2 gases. The films were deposited under the conditions of various boron concentrations(100~400 ppm) and deposition times(2~5 hours). The influence of surface treatment of the films by oxygen and hydrogen plasma was investigated, respectively. The surface state and crystalline structure of the deposited diamond films in each conditions have been analyzed by XRD, SEM, AFM, TEM, Raman spectroscopy and XPS, etc. The interfacial properties, internal stress, thermal conductivity and I-V characteristics of the deposited polycrystalline diamond films in SOD structure will be discussed.

P-020

EFFECT OF NEUTRAL GAS FLOW ON THE PLASMA STATE IN ICP PROCESS, W. Y. CHUNG and D. H. KIM(Dept. of Chemical Engineering. KAIST, Taejon, 305-701, Korea)

Escalation of costs for the semiconductor device fabs has been driven in large part by the increasing cost of process equipments including the equipments using plasma. Mathematical modeling and computer simulations have become major tools in semiconductor industry to lower costs and shorten time involved in the design of equipments and processes while they are not widely used for the plasma reactors because of the complexity of plasma. We have performed mathematical modeling and computer simulations for inductively coupled Ar-plasma reactor used in CVD and etching of thin film. Mathematical model which includes the description of transport phenomena of the neutral gas are solved numerically using Galerkin FEM. Effects of interaction of the neutral gas and the charged particle on plasma density, electron temperature and ion fluxes are examined. In addition, the effects of the process conditions, geometry of the coils and process pressure are also examined.

P-021

ELECTROCHEMICAL AND PHOTOELECTROCHEMICAL ETCHING OF N-TYPE SILICON, CHI-WOO LEE[1], DONG-IL KIM[1], BUEM-SUCK KIM[1] and NAM-KI MIN[2] (Dept. of Chemistry[1], and Dept. of Control and Instrumentation Engineering[2], Korea University, Jochiwon, Choongnam 305-701, Korea)

Silicon has become the most important semiconductor material for electronics industry since it was shown to have a good semiconducting property with an indirect bandgap energy of 1.1 eV fifty years ago and is available in large area wafers in high quality to produce almost all semiconductor devices. It can be effectively etched by electrochemical and photoelectrochemical methods to produce porous silicon. Porous silicon has been used as dielectric insulator for silicon-on-insulator technology since it was discovered to have a microscopic structure network within the bulk of silicon wafer fourty years ago and is now believed to be one of the most promising optoelectronic materials showing efficient photoluminescence as well as electroluminescence at room temperature. To understand the correlation between crystal silicon and posous silicon, we have been involved in investigating electrochemical and photoelectrochemical processes to form porous silicon for the past several years. In this work, we will present the recent developments in this lab.

P-022

A STUDY ON THE EFFECT OF METALLIC IMPURITIES ON MICROROUGHNESS OF SI WAFER, HYUNGSEOK CHOI, and HYEONGTAG JEON (Semiconductor Materials Laboratory, Division of Materials Science Engineering, Hanyang University, 17, Haengdang-dong, Seongdong-ku, Seoul 133-791, Korea)

A cleaning of Si surface has become one of the most critical processes on ULSI device. One of the major concerns is about the removal of metallic impurities on Si surface. In this study we concentrated on the metallic impurity of Ca. The Si surface was cleaned using piranha(H_2SO_4:H_2O_2=4:1) and HF(HF:H_2O=1:10) solutions to eliminate the organics and the native oxide. Then the initial Si substrate was contaminated intentionally by dipping it into 10ppm standard solution of Ca and followed by the cleaning splits of HF solution and the chemical mixture of HF with H_2O_2. After these treatments, Si substrates were oxidized about 200Å thickness. The contamination level of initial wafer which was measured by TXRF(Total X-Ray Fluorescence) was 4×10^{11} atoms/cm^2 and removed down to the levels as low as 10^{10} atoms/cm^2. Also the microroughness of each split was measured by AFM(Atomic Force Microscope). After oxidation the minority carrier lifetime was measured by SPV(Surface Photo Voltaic)method and the microroughness was measured by AFM again. The interface morphologies between Ca contaminated Si and SiO_2 were examined by TEM(Transmission Electron Microscope). Finally the electrical properties of Ca contaminated surface were measured by I-V measurement. These results will be discussed and compared depending on the concentration of metallic impurities and microroughness on Si substrates.