Sym. F : Ferroelectric Thin Films

FERROELECTRIC FIELD EFFECT

A-WED-01

ELECTRICAL PROPERTIES OF MFIS CAPACITORS WITH PZT/TiO_2 LAYERS, HYUNG-SEOK KIM, SUNGWON JUNG, WOOSUNG CHOI, JIYOUNG KIM (Dept. of Met. & Mat. Eng., Kookmin Univ., Seoul 136-702, Korea)

Recently, MFIS (Metal/Ferroelectrics/Insulator/Semiconductor)FET memory cells are attracted an attention for nonvolatile memory applications because their mobile electrons are not only operated with low power and voltage but also kept data without supplied power. Especially, MFIS capacitors with PZT/TiO_2 layers are suitable for nonvolatile memory. PZT that presents excellent ferroelectrical properties in low voltage conditions is widely used as a ferroelectric material. TiO_2 is a good candidate for an insulator because it is a diffusion barrier with a moderate high dielectric constant. So, in this paper, capacitors with PZT/TiO_2 layers were fabricated and their electrical properties will be reported.

Ir/PZT/TiO_2/Si capacitors were fabricated on the (100) p-type Si substrate. Si wafers were cleaned by piranha method. TiO_2 layers for insulator were deposited by DC reactive sputtering technique and they were annealed in O_2 ambient. Sol-gel method was used for deposition of 350nm PZT films followed by an crystallization anneal. 100nm Ir top electrode was deposited using DC sputtering and the patterned device size is $2\times10^{-4}cm^2$. Accumulation capacitance for MFIS capacitors is a $400nF/cm^2$, and memory window for nonvolatile memory is about 2.5V in high frequency C-V measurement.

A-WED-02

LOW PERMITTIVITY FERROELECTRIC THIN FILMS FOR FERROELECTRIC GATE FIELD EFFECT TRANSISTOR BY CHEMICAL SOLUTION DEPOSITION, S.W. JANG, C.Y. KIM, D.C. WOO, H.Y. LEE, W.S. JUNG (College of Eng., Yeungnam University, Kyongsan, 712-749, Korea), W.-J. LEE (ETRI, Daejon, 305-350, Korea) and S.H. KIM (Dept. of Mat. Sci. & Eng, North Carolina State University, Raleigh, NC 27695-7919, USA)

It is known that low permittivity ferroelectric thin film is required for ferroelectric gate FET memory device. Ferroelectric $La_2Ti_2O_7$ (LTO) and $Sr_2(Nb,Ta)_2O_7$ (SNTO) thin films have dielectric constant values of about 20, and are possible candidates for this application. Thin films were deposited on platinized silicon wafers by modified sol-gel and metalorganic decomposition (MOD) processes. Annealing of multiple-coated film stacks was done above 900°C. After top Pt electrode deposition through shadow mask, ferroelectric properties of gate capacitors of MFMIS structure were measured using RT66A ferroelectric tester. Leakage current characteristics were also determined. In this paper, the comparison between two chemical solution processes will be made in case of LTO and SNTO films. Emphasis will be placed on the composition and/or processing parameter dependence of ferroelectric and leakage characteristics.

A-WED-03

CHARACTERISTICS OF THIN FILM $LiNbO_3$ ON P-TYPE SI(100) Y. S. ChOI, S. M. JUNG, D. Y. KIM, and J. YI (School of EEC, SKKU, Suwon,440-746, Korea)

$LiNbO_3$ transistor showed relatively stable characteristic, low interface trap density, and large remanent polarization. This paper reports ferroelectric $LiNbO_3$ thin films grown directly on p-type Si(100) substrates by 13.56MHz RF magnetron sputtering system for FRAM applications. RTA(Rapid Thermal Annealing) treatment was performed for as-deposited films in an oxygen atmosphere at 600℃ for 60 s. We learned from X-ray diffraction that the RTA annealed films were changed from amorphous to poly-crystalline $LiNbO_3$ which exhibited (012), (015), and (214) orientation. RTA improved the leakage current of films, and the leakage current density of films decreased from 10^{-7} to 10^{-8} A/cm^2 at room temperature measurement. Breakdown electric field of the films exhibited higher than 500kV/cm. The C-V curves showed the counterclockwise hysteresis represents ferroelectric switching characteristics. From C-V curves, we calculated dielectric constant of thin film $LiNbO_3$ as 27.5 which is close to that of bulk value.

A-WED-04

INFLUENCE OF RAPID THERMAL ANNEALING OF CERIUM OXIDE ON THE MORPHOLOGICAL AND ELECTRICAL PROPERTIES OF METAL/FERROELECTRIC/INSULATOR/SEMICONDUCTOR CAPACITOR, Ho Nyung Lee†, Dong Suk Shin, Yong Tae Kim (Semiconductor Materials Laboratory, Korea Institute of Science and Technology, Seoul 136-791, Korea) and Sung Ho Choh (†Department of Physics, Korea University, Seoul 136-701, Korea)

Preparing $SrBi_2Ta_2O_9$ (SBT) film by metal organic deposition (MOD), we have found that the surface morphology of SBT film becomes smoother on rougher CeO_2 film rather than smooth one after annealing at 800 °C. This result drastically improves electrical properties of Pt/SBT/CeO_2/Si capacitors. The reason for smooth surface of SBT and electrical improvements seems due to smaller grains of SBT on the rough CeO_2 film. Therefore, in this work, we have tried to investigate the surface and interface morphologies of Pt/SBT/CeO_2/Si structure and correlate these results with capacitance, memory window, and leakage current of ferroelectric capacitor using capacitance-voltage (C-V) measurement, X-ray diffraction (XRD), atomic force microscopy (AFM), and transmission electron microscopy (TEM).