Anomalous Phenomena on Subthreshold Characteristics of SOI MOSFET Back Gate Voltage

Seung-Min Lee and Mike Myung-Ok Lee
Department of Information and Communication Engineering, Dongshin University,
252 Daeho-Dong, Naju, Chonnam, 520-714, Korea
(Tel) 0613-330-3195 (Fax) 0613-330-2909 (E-mail) mikelee@dongshinu.ac.kr

SOI MOSFET Back게이트전압에 따른 Subthreshold 특성의 특수현상

전남 나주시 대호동 252번지 동신대학교 정보통신공학과
이 승 민, 이 명 옥
(전화) 0613-330-3195 (Fax) 0613-330-2909 (E-mail) mikelee@dongshinu.ac.kr

Abstract

The 1-D numerical model and its extraction methodology are suggested and these simulation results for the S-swing as a function of back-gate voltage are well matched with the measured. S-swing characteristics are analyzed using PD-SOI devices with enough deeper regions up to substrates. The PD-SOI device doesn't have to be short channel to see the anomalous subthreshold phenomena based on the back gate bias. This results recommend to operate better SOI device performances by controlling the back gate voltages. So SOI performances will be much optimistic with proper control of the back-gate voltage for the already- proven- high-performance (APHP) SOI VLSIs.

1. Introduction

It is well known that SOI MOSFET is promising for High speed(HS) and especially Low Power(LP) in VLSI design due to Low parasitic capacitance, well-less simple AMOS process, low voltage operation and high drivability. these performances depend upon gate oxide thickness, gate poly materials, SOI silicon island thickness, buried oxide thickness. One of the most interesting characteristics on MOS device is to thoroughly analyze the subthreshold slope factor (S-swing or S-factor) which influences on the performance, *i.e.*, Low power investigation related to current information & communication era. Thereby this research presents new investigative rather anomalous findings on the S-swing depending on the backgate voltage of the SOI MOSFET. The 1-D numerical model and its extraction methodology are suggested and these simulation results for the S-swing as a function of back-gate voltage will be compared with measured one. It is forced that the model and extracted S-swing results are well matched with the measured and also the SOI performances will be much optimistic with proper control of the back-gate voltage for the already- proven- high-performance(APHP) SOI VLSIs.

2. Model Development of SOI MOSFET

1) Necessity of the numerical model

SOI process technology has recently matured to improve the performances. However there are some unsolved problems for variations of SOI silicon thickness, gate oxide uniformity high substrate costs and floating body mechanisms. Commercial products using SOI VLSIs to those problems against conventional bulk-Si SOI VLSIs. There are two types of SOI CMOS: one is Partially Depleted(PD); the other Fully- Depleted (FD)[1]. These SOI types are classified by processing technology, varying a forementioned SOI parameters. Currently possible commercial products are mainly made out of the PD-SOI CMOS[2]. Another thrust for SOI researches so far is focused on deep submicron high performance FD-SOI design, varying thin gate oxide and thin SOI silicon thickness, but leakage currents and reliability issues by FD-SOI design causes the gate oxide uniformity and bleeding power at low voltage operation. It is so important that S-swing characteristic must be analyzed using PD-SOI devices with enough deeper regions up to substrates. The PD-SOI device doesn't have to be short channel to see the anomalous subthreshold phenomena based on the back gate bias. First, there are many analytical and numerical models to evaluate device characteristics and verifications of valid parameter fittings, but those analytical & numerical models can not include the effect of bulk substrate, and just approximates the potential distribution within the substrate. Therefore, accurate 1-D numerical model is constructed to see the effect of SOI's backgate voltage for S-swing. The model converges fast and simulation time is short. Based on the result of the simulation model, structural parameter extraction of the SOI MOSFET shows the fundamental extraction methodology using 1-D numerical model with various physical characteristics.

2) Basic Mathematical Formulations

The 1-D numerical equations of the SOI MOSFET are eq. (1), (2), (3) and (4). Those poisson's and related continuity equations calculate the region of subthreshold and then election concentrations, and hole concentrations will be evaluated using the thermal equilibrium states.

$$\frac{d}{dx}\left(\varepsilon \frac{d\psi}{dx}\right) = -q(N_A - n(x) + P(x)) \quad (1)$$

$$n(x) = ni \ e^{\left[\frac{1}{(kT/q)}\psi(x)\right]} \quad (2)$$

$$n(x) = ni \ e^{\left[\frac{1}{kT/q}(\psi(x) - V_{DS})\right]} \quad (3)$$

$$p(x) = \frac{ni}{n(x)} \quad (4)$$

Where N_A is impurity concentration of SOI layer, is a thermal voltage as 25.9mV. Fig.1 shows the cross-sectional of SOI MOSFET for the simulations. As shown in Fig.1, considered PD-SOI parameters including the substrate are gate oxide thickness, SOI layer thickness, buried-oxide thickness, bulk substrate thickness, SOI layer's doping concentrations, bulk substrate impurity concentration. Based on the model with various SOI parameters, surface potentials, surface trapped states, gate voltage and bulk substrate voltages are calculated with proper boundary conditions as:

$$\Psi g = Vgf - \Phi gate \quad (5)$$

$$\Psi b = Vgb - \Phi sub \quad (6)$$

Where Φgate is potential difference between SOI layer and n-type poly silicon and is about -0.8V, Φsub is a Fermi voltage difference between SOI layer and bulk substrate, $\Phi sub = \frac{kT}{q}\log\left(\frac{Nsub}{N_i}\right)$ and Nsub is bulk substrate density.

3)Surface Trapped States Model

Interface trapped states are analyzed from the interface trapped charge model along with Fermi-dirac distribution formula as the below Eqs[1]:

$$F_{SD}(E_i) = \frac{1}{1 + g\, e^{\left(\frac{E_F - E_i}{kT}\right)}} \quad (7)$$

$$F_{SA}(E_i) = \frac{1}{1 + \frac{1}{g}\, e^{\left(\frac{E_i - E_F}{kT}\right)}} \quad (8)$$

$$Q_{it1,2,3} = \int_0^{E_i} (D^d_{it1,2,3} F_{SD} - D^a_{it1,2,3} F_{SA} + D_{it1,2,3}) dE_i + Q_{it1,2,3} \quad (9)$$

4. Results, Discussions and Summary

Performances and characteristics of SOI MOSFET generally depend on various parameters such as SOI thickness(t_{SOI}), front gate oxide(t_{fOX}), buried oxide thickness(t_{BOX}), impurity concentration(N_A or N_{SUB}), and surface interface states(D_{it1},D_{it2},D_{it3}). It is well-known that SOI has excellent advantages over Bulk-Si MOS for future low power and high speed ULSIs[2]. Analysis and optimization of the electrical properties of SOI, however, need some actual parameter for development of the fundamental device performance. Plane numerical model and model parameters with device capacitances of partially depleted(PD) SOI MOSFET are shown in Fig. 1(a),(b) where the dose of (100) p-type substrate is $4X10^{19}/cm_3$, expected fabricated values of t_{fOX}, t_{SOI}, t_{BOX}, are 7, 50, and 80(nm), respectively. The sampled gate length and width of the PD SOI are 1 and 20(um)[3] to understand the subthreshold slope factor(S-swing) characteristics by varying back gate voltages[4]-[6]. This research presents thorough S-swing phenomena by the gate bias voltages for better performance of better S-swing region. Fig. 2(a),(b) show measured and simulated drain-gate characteristics as a function of backgate voltage in the region of subthreshold. Fig. 2 looks a normal subthreshold characteristics [7][8] without indicating parasitic MOS effect of edge area of SOI silicon layer, i.e., drain currents above the back gate voltages of 2v is not decreasing up to measured critical limit and indicate a constant value of the drain currents because the back channel is generated due to inversion at the boundary of SOI silicon layer[9]. Fig. 3(a),(b) show the numerical and measured results for the S-swing as a function of back gate voltages where the region I is acc. of SOI layer, II is complete dep. toward SOI layer, III weak inv. of the SOI layer, IV weak inv. of the SOI layer with acc. from dep. at the bulk substrate, and V sharp increase of S-swing since there is no way to control the front gate when the back channel is generated. From the Fig. 3, unlike normal MOS, the S-swing shows anomalous phenomenon of boundaries at each layer. Further electron and hole density explain those regions as shown in Fig. 4(a),(b). D_{it2}- and D_{it3}-dependence by the back gate voltage clearly, for the first time to date, reveal local minima of the S-swing whose values largely varies, depending on the D_{it2}- and D_{it3}-variation. As shown in Fig. 5(a), (b), the numerical calculations match with the measured results from various samples where extracted parameter sets are listed as Table 1. This results recommend to operate better SOI device performances by controlling the back gate voltages. Further, validity of characteristics from various fitting parameters is analyzed by least square error method based on the following eq.:

$$\Delta = \sum\{(S_m(V^i_{BS}) - S_s(V^i_{BS})) \cdot \omega(S^i)\}^2,$$

where w(S) is weighted factor, Sm and Ss are

S-swing of measured and simulation. Fig. 6 show the valid contour plot for local minimum for each parameters.

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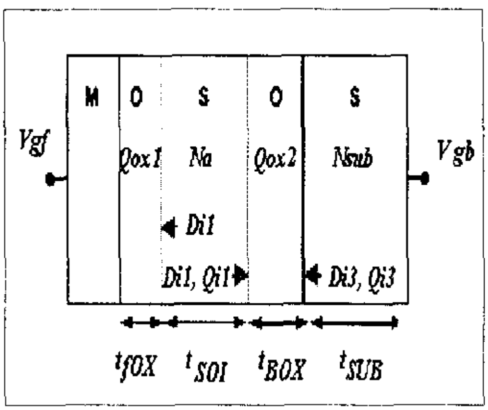
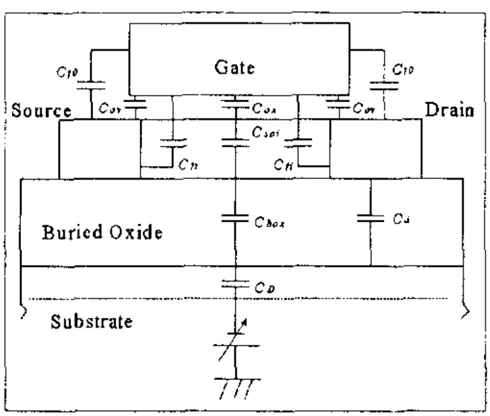


(a)

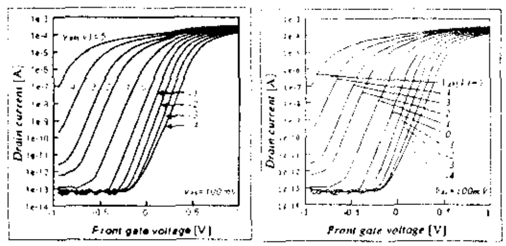


(b)

Fig.1(a) SOI device view.(b)PD SOI device capacitances

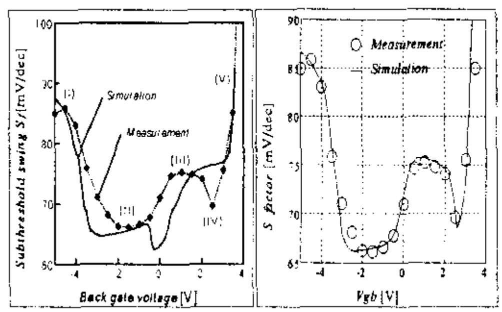
Table. 1. Extracted parameter sets for S-swing

Parameters	Sample 1	Sample 2	Sample 31
t_{OX}[nm]	7.0	6.0	7.3
t_{SOI}[nm]	50	55	65
t_{BOX}[nm]	80	95	100
N_A[/cm^3]	4X10^{16}	1X10^{17}	1X10^{17}
N_{SUB}[/cm^3]	4X10^{14}	6X10^{15}	1X10^{15}
D_{i1}[/cm^2 eV]	5X10^{10}	5X10^{10}	5X10^{10}
D_{i2}[/cm^2 eV]	2X10^{11}	1X10^{10}	3X10^{10}
D_{i3}[/cm^2 eV]	1X10^{11}	1X10^{11}	2X10^{11}
Q_{i2}[/cm^2]	1.1X10^{11}	1X10^{11}	3X10^{11}
Q_{i3}[/cm^2]	4X10^{11}	8X10^{11}	7X10^{11}



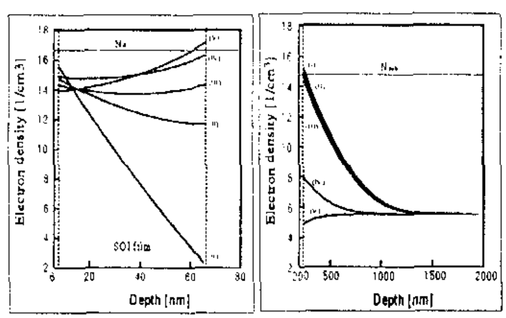
(a) (b)

Fig.2(a)Measured I-V as a function of front gate voltage.

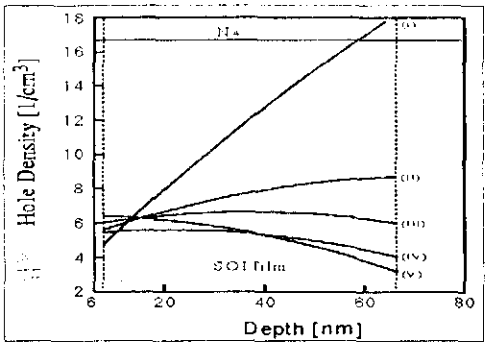


(a) (b)

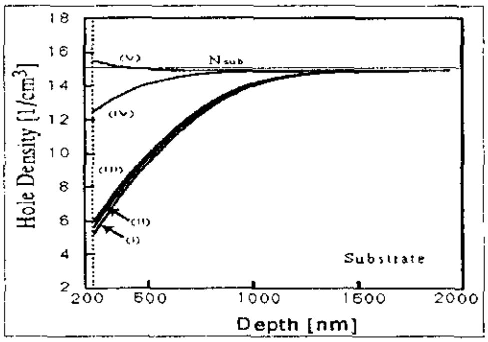
Fig.3(a)S-swing characteristics as a function of back gate voltage. (b)Magnified portion of (a).



(a) (b)



(c)



(d)

Fig.4. Electron density for S-swing characteristics of (a)SOI thickness depth, (b) substrate depth, (c) Hole density for S-swing characteristics of thickness depth, (d) of substrate depth.

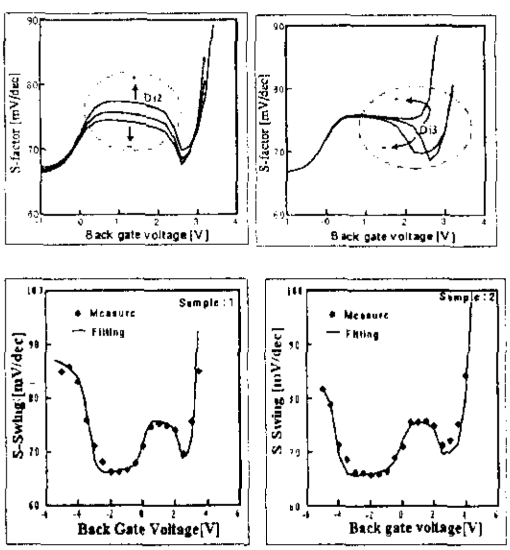
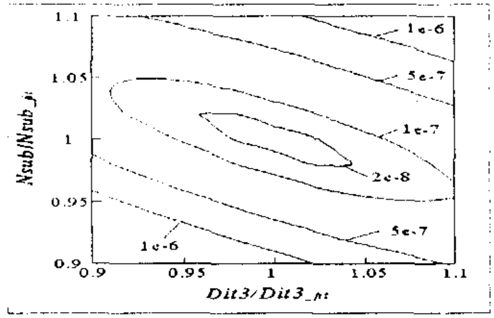
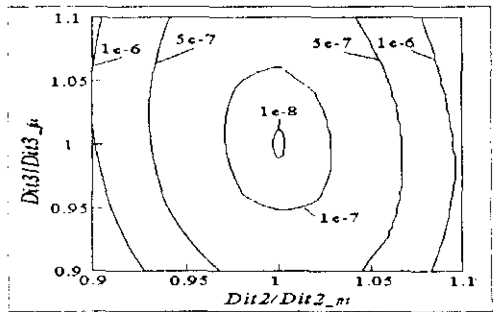


Fig. 5(a)Di2-dependence of S-swing characteristics, (b) Di3-dependence of S-swing characteristics, (c) A typical Di3-dependence of S-swing characteristics with measured ones, (d)A typical Di3-dependence of S-swing characteristics with measured ones.



(a)



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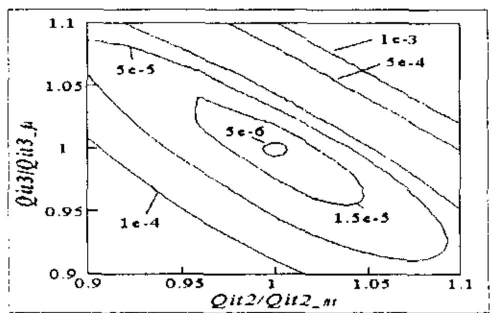

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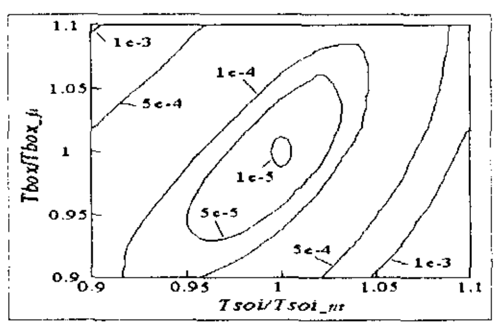

(d)

Fig.6(a) The valid contour plots for local minimum for each parameters as a error analyses in (a) (Di2, Nsub)-space, (b) (Di3, Nsub)-space, (c)(Qi2, Qi3)-space, and (d) (T_{SOI}, T_{BOX})-space.