Thermal treatment effect of CaF_2 films for TFT gate insulator applications

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Abstract

Fluoride (CaF_2) films exhibited a cubic structure with similar lattice constant to that of Si and have sufficient breakdown electric field as gate dielectric material. Therefore, CaF_2 are expected to replace conventional insulator such as SiO_2, Ta_2O_5, and Al_2O_5. However, CaF_2 films showed hystereisis properties due to mobile charges in the film. To solve this problem we performed thermal treatment and achieved improved film characteristics in hystereisis properties and breakdown electric field. C-V results indicate a reduced hystereisis window of ΔV=0.2V, low interface state $D_{it}=2.0\times10^{11}cm^{-1}eV^{-1}$ in midgap, and good MIS diode properties. We observed a preferential crystallization of (200) plane from XRD analysis. RTA treatment effects on various material properties of CaF_2 are presented in this paper.

1. Introduction

Fluoride film have many practical applications such as gate insulator of thin film transistor (TFT), antireflection coating, and optical waveguide. We carried out a research work on CaF_2 gate insulator for TFT applications. Most of gate oxide films like SiO_2, Ta_2O_5, Al_2O_3, and SiO_x exhibited problems on interface trap charge density (D_{it}), lattice mismatch, interface state in corporation with O-H bond created by mobile hydrogen atoms in a-Si:H and oxygen atoms in gate oxide layer. We have employed fluoride film as a gate insulator for TFT applications. CaF_2 films with low D_{it} and similar lattice constant to Si surface are expected to circumvent problems in conventional gate insulators.

2. Experimental Procedures

We used to (100) p-type Si (10~20Ωcm) as a substrate of MIS structure samples. To remove substrate contamination, p-Si substrate was cleaned by RCA method. Upon cleaning of p-Si, a metal of Al electrode was deposited at the backside of Si substrate to the thickness of 2000Å by thermal evaporation method. Thermal treatment using a resistive thermal furnace in 620℃ for 15min with N_2 gas flow rate of 2.5 *lpm* formed a backside ohmic contact. To remove negative oxide layer(<20Å) Si surface were dipped to BHF (HF(49%) : H_2O = 1:10) for few seconds. Fabricated MIS device structure is shown in Fig. 1. CaF_2 deposition source was in 3-5mm pieces with purity of 99.95%. To prevent explosive evaporation of poly atomic clusters we used baffled furnace type as a source boat. Top electrode metals were formed with thickness of 500~700Å for an electrical property measurement. MIS devices were treated by Rapid Thermal Anneal (RTA) system for various temperatures and time durations. Interface and film properties of CaF_2 were evaluated by C-V and I-V measurement using Keithley 617, Fluke 5100B, Boonton 7200, and computer data acquisition system. We determined breakdown electric field (E_{br}) from I-V characterization. These electrical properties were analyzed in conjunction with structural properties using a XRD result.

3. Results and Discussions

p-Si(100) substrate have exhibited the resistivity of 10~15Ωcm from four-point prove measurement. Irwin curve showed doping density of $10^{15}cm^{-3}$ for the corresponding substrate resistivity. Figure 2 shows C-V results of MIS at 1MHz as a function of substrate temperature during the film growth. We calculated dielectric constant of samples from accumulation region capacitance which is somewhat lower value (ε_r~4.11) than bulk CaF_2 (ε_r=6.8). In case of sample grown at room temperature, there existed a shoulder in front of the inversion region because the internal structure of insulator have positive charges and defects induced by low thermal energy due to the low substrate temperature. Low temperature deposited CaF_2 films showed the high value of flatband shift window as ΔV=0.5~1V depending on a bias scan direction which indicates imperfection of growth film quality. Interface trap density calculated from HF C-V and Quasistatic method showed low D_{it} of $1.8\times10^{11}cm^{-1}eV^{-1}$ for 100℃ deposited sample. Figure 3 shows D_{it} profile as a function of deposition temperature. This result indicates that very high deposition temperature lead to an increased D_{it} $>2.6\times10^{11}cm^{-1}eV^{-1}$. Current-Voltage(I-V) characteristics showed conventional p-n junction diode profile. But E_{br} decreased as repeatedly applied high voltage bias to the MIS devices from 0.7MV/cm to 0.3MV/cm. I-V curve changed into ohmic curve when electric field exceeded E_{br}. We observed in comparison with C-V and I-V that hysteresis properties were occurred for the low substrate temperature but this disappeared as increasing temperature. However, I-V properties of sample without hysteresis were not so good as MIS devices with hysteresis because of low E_{br} <0.3MV/cm. This causes some problems to the gate insulator application because of instabilities and low E_{br} characteristics. But low temperature deposited samples exhibited high E_{br} and good diode properties. If hysteresis loop can be reduced to this sample, we expect that CaF_2 films to be adopted in gate insulator application. Aiming at this expectation, we carry out an anneal treatment using a RTA system. Figure 4 shows C-V characteristics before and after anneal treatment of 400℃ for 100sec on the sample deposited at 100℃. Anneal temperature of 400℃ exhibited an improved ΔV than other RTA treatment temperature. This result indicates imperfection of insulator was removed during RTA process. Dielectric failure was detected for the anneal treated samples at high temperature because film stress relaxation created pinholes and pittings. This result was analyzed in conjunction with crystalline analysis. Figure 5 shows XRD curves as a function of anneal temperature. As anneal temperature was increased, CaF_2 films are transformed to randomly oriented from (200) preferential orientation for 400℃ RTA anneal treated sample. XRD results and electrical characterizations are well explain the property improvement by 400℃ RTA.

4. Conclusion

In this work we deposited CaF_2 film by thermal evaporation method on the p-Si(100) substrate. Low temperature deposited MIS device have larger hysteresis ΔV than high temperature deposition. But high temperature deposited film had lower E_{br} than low temperature deposited device. This properties induce problems as gate insulator of TFT application. RTA of 400℃ for 100sec improved this short fall. After annealing we observed ΔV decreased less than 0.3V. From crystalline analysis result on 400℃ RTA sample, the peak of (200) plane showed FWHM=0.2 and lattice constant a=5.81Å. Our recommendation for the high quality MIS device is that deposition temperature of 100℃, thickness 1500Å, and RTA 400℃ for 100sec.

Acknowledgments

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References

1 Gerard Barnottin, Andre Vapaille, Instabilities in Silicon Devices, **2**, (1989).

2 D. B. Cuttriss, Bell Syst. Tech. J. **40**, (1961) 509.

3 S. Sinharoy, Thin Solid Films, **187** (1990) 231.

4 J. C. Alvarez, M. I. Veksler, I. V. Grekhov, N. S. Sokolov, and A. F. Shulekin Semiconductors, **30** (7) (1996) 698.

5 Tanemasa Asano and Hiroshi Ishiwara, Jpn. J. Appl. Phys., **21**, No. 10, (1982), L630.

6 M. Barkai, Y. Lereah and E. Grünbaum, Thin Solid Films, **139** (1986) 287.

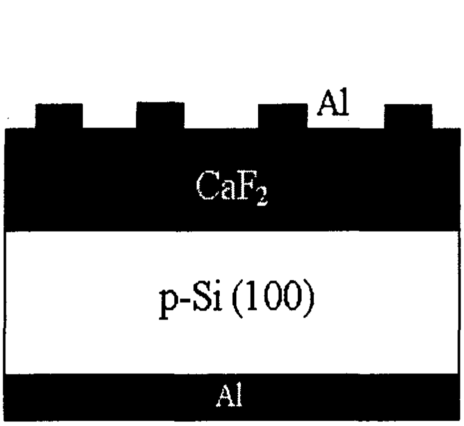

Fig. 1. MIS structure using CaF_2 insulator

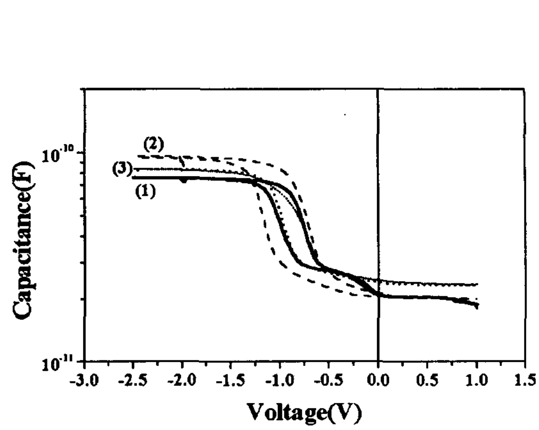

Fig. 2. Hysteresis properties as a function of substrate. temperature (1) room temp. (2) 100℃ (3) 200℃

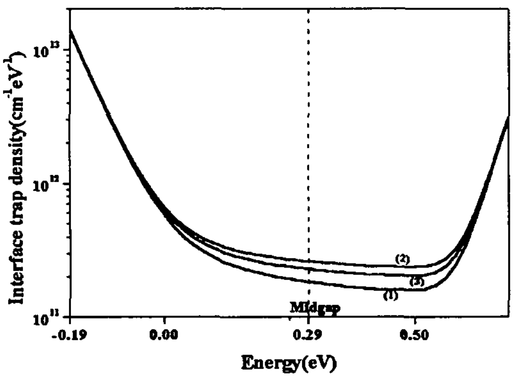

Fig. 3. D_{it} of CaF_2/p-Si(100) as a function of substrate temperature. (1) 100℃ (2) 200℃ (3) 300℃

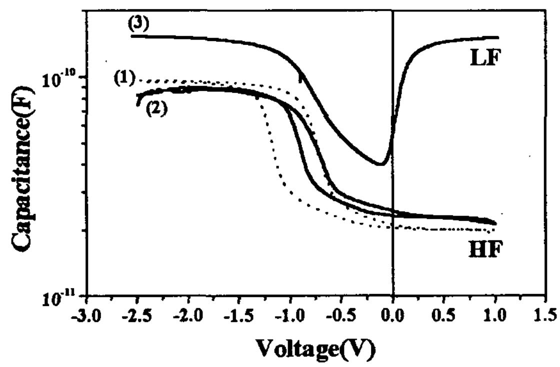

Fig. 4. Hysteresis properties after RTA (1) before annealing (2) after annealing (3) ideal curve

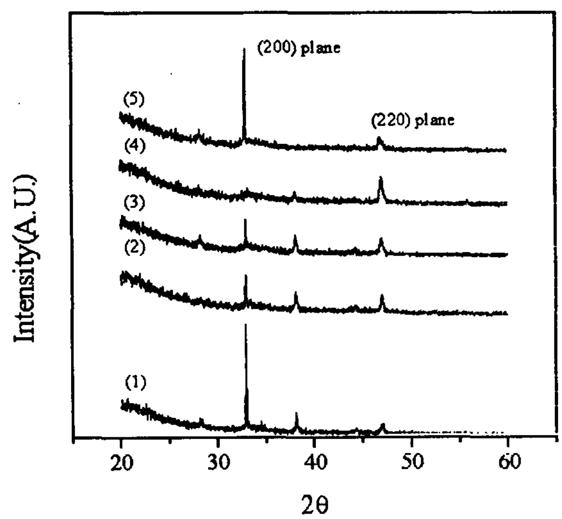

Fig. 5. XRD curve as a function of RTA annealing temperature (1) 400℃ (2) 500℃ (3) 600℃ (4) 700℃ (5) before RTA