Design of Digital Controller for Uninterruptible Power Supply Using Disturbance Observer

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ABSTRACT - This paper describes a new digital control method of 3-phase PWM inverter with LC filter for uninterruptible power supply(UPS) The overall control system is based on the dead beat control, which has the minor loop of current control within the voltage control major loop. In this paper, the full-order disturbance observer is proposed to compensate the disturbances generated due to a sudden change of load currents. The proposed disturbance observer is composed of dead beat observer which estimates state values within a finite time, and cancels the disturbances by adding feedforward compensation loop in the control system. In addition, in order to remove a defect of oscillation generated in output of conventional dead beat controller, a modified dead beat algorithm is proposed in this paper.

1. INTRODUCTION

In recent years, the various electronic machines as well as computer systems have been widely used and the reliance on the power source has became a important issue. If power source shut down even for a short period, the damage would be serious. Therefore, the demand of UPS(uninterruptible power supply) system to avoid damage is getting more and more.

The objective of UPS system is to supply sinusoidal voltage with constant amplitude and frequency to loads without any interruption in most of cases on power source failure. The quality of UPS can be evaluated by low total harmonic distortion (THD) of output voltage for nonlinear loads such as rectifier loads and characteristics of transient response. To improve the performance of UPS output voltage, the PWM inverter control circuit has changed analogue into digital controller. In general, controllers of UPS have double control loop that consists of voltage major loop and current minor loop, and it was proposed that fully digital control of PWM inverter has fast transient response with dead beat controller[1],[2] But this control method requires load current sensor to compensate disturbances generated by load currents.

To remove current sensors for measurement of load currents, this paper proposes a new disturbance observer algorithm. The proposed disturbance observer estimates the load current without current sensor and cancels the disturbances by adding feedforward compensation loop. In addition, in order to solve another problem of conventional dead beat digital controllers such as output oscillations of controller, a modified dead beat control algorithm is proposed, too. Though the proposed control algorithm, the THD value of output voltage of the UPS system is reduced and the transient response of controller is improved. In addition to these effects, the modified dead beat controller makes it possible to decrease dc-link voltage of the PWM inverter by eliminating the oscillations from output of the digital controller. To verify the validity of the proposed new control algorithm, simulation is carried out with RL linear load and 3Φ rectifier load, respectively.

2. DISCRETIZATION OF STATE EQUATION FOR UPS

Fig. 1. shows overall configuration of UPS system which consists of 3-phase inverter, LC filter to supply sinusoidal voltage to the loads, and dc link batteries. From the relation of system input and output, the state equation of UPS system is described as follows

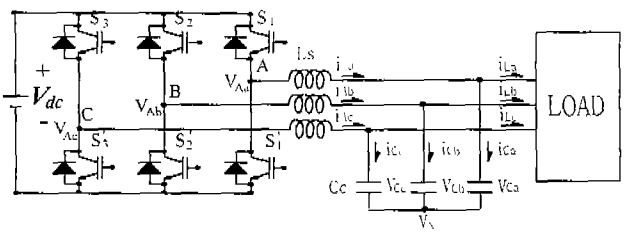


Fig. 1. Overall configuration of UPS system.

$$C_c \frac{d}{dt} \vec{V}_C = \vec{I}_A - \vec{I}_L \quad (1)$$

$$L_s \frac{d}{dt} \vec{I}_A = \vec{V}_A - \vec{V}_C \quad (2)$$

$$\vec{I} = [I_a, I_b, I_c],\ \vec{V} = [V_a, V_b, V_c] \quad (3)$$

Equations (1)~(3) can be transformed into state equation (5), which represent the d-q variables of voltage and current on the synchronous reference frame. Choosing the capacitor voltage V_{Cqd} and inductor current I_{Aqd} as the state variables, the system state equation is represented as Eq. (5) by the general state equation of (4).

$$\dot{x} = Ax + bu + v \quad (4)$$

$$\begin{pmatrix} \dot{I}_{Aq} \\ \dot{I}_{Ad} \\ \dot{V}_{Cq} \\ \dot{V}_{Cd} \end{pmatrix} = \begin{pmatrix} 0 & -\omega & 1/L_s & 0 \\ \omega & 0 & 0 & 1/L_s \\ 1/C_c & 0 & 0 & -\omega \\ 0 & 1/C_c & \omega & 0 \end{pmatrix} \begin{pmatrix} I_{Aq} \\ I_{Ad} \\ \vec{V}_{Cq} \\ \vec{V}_{Cd} \end{pmatrix} + \begin{pmatrix} 1/L_s & 0 \\ 0 & 1/L_s \\ 0 & 0 \\ 0 & 0 \end{pmatrix} \begin{pmatrix} V_{Aq} \\ V_{Ad} \end{pmatrix} + \begin{pmatrix} 0 & 0 \\ 0 & 0 \\ 1/C_c & 0 \\ 0 & 1/C_c \end{pmatrix} \begin{pmatrix} I_{Lq} \\ I_{Ld} \end{pmatrix} \quad (5)$$

In Eq. (4), the vector v is the disturbance term which is induced in the voltage major loop of controller. Equation (5) can be separated into (6), (7), respectively.

$$\begin{pmatrix} \dot{I}_{Aq} \\ \dot{I}_{Ad} \end{pmatrix} = \begin{pmatrix} 0 & -\omega \\ \omega & 0 \end{pmatrix} \begin{pmatrix} I_{Aq} \\ I_{Ad} \end{pmatrix} + \begin{pmatrix} 1/L_s & 0 \\ 0 & 1/L_s \end{pmatrix} \begin{pmatrix} V_{Aq} \\ V_{Ad} \end{pmatrix} - \begin{pmatrix} 1/L_s & 0 \\ 0 & 1/L_s \end{pmatrix} \begin{pmatrix} V_{Cq} \\ V_{Cd} \end{pmatrix} \quad (6)$$

$$\begin{pmatrix} \dot{V}_{Cq} \\ \dot{V}_{Cd} \end{pmatrix} = \begin{pmatrix} 0 & -\omega \\ \omega & 0 \end{pmatrix} \begin{pmatrix} V_{Cq} \\ V_{Cd} \end{pmatrix} + \begin{pmatrix} 1/C_c & 0 \\ 0 & 1/C_c \end{pmatrix} \begin{pmatrix} I_{Aq} \\ I_{Ad} \end{pmatrix} - \begin{pmatrix} 1/C_c & 0 \\ 0 & 1/C_c \end{pmatrix} \begin{pmatrix} I_{Lq} \\ I_{Ld} \end{pmatrix} \quad (7)$$

Equation (6) is the inverter current state equation and (7) represents capacitor voltage state equation. A reference voltage of the output capacitor voltage on time domain will be given as Eq. (8) and on synchronous reference frame Eq.(9)

$$\begin{pmatrix} E^*_{an} \\ E^*_{bn} \\ E^*_{bn} \end{pmatrix} = \begin{pmatrix} \sqrt{2}\, V_m \cos \omega t \\ \sqrt{2}\, V_m \cos(\omega t - \frac{2}{3}\pi) \\ \sqrt{2}\, V_m \cos(\omega t + \frac{2}{3}\pi) \end{pmatrix} \quad (8)$$

$$V^*_{Cqd} = \begin{pmatrix} V^*_{Cq} \\ V^*_{Cd} \end{pmatrix} = \begin{pmatrix} \sqrt{2}\, V_m \\ 0 \end{pmatrix} \quad (9)$$

Also, the state equations (6) and (7) of the inverter current and the capacitor voltage can be converted into disretization state equations of (10), (11) and the controller consists of discretization form like these equations.

$$I_{Aqd}(k+1) = KI_{Aqd}(k) + LV_{Aqd}(k) - LV_{Cqd}(k) \quad (10)$$

$$V_{Cqd}(k+1) = KI_{Aqd}(k) + MI_{Aqd}(k) - MI_{Lqd}(k) \quad (11)$$

where $K = \begin{pmatrix} 1 & -\omega T \\ \omega T & 1 \end{pmatrix}$, $L = \begin{pmatrix} \frac{T}{L_s} & -\frac{\omega T^2}{2L_s} \\ \frac{\omega T^2}{2L_s} & \frac{T}{L_s} \end{pmatrix}$

$$M = \begin{pmatrix} \frac{T}{C_c} & -\frac{\omega T^2}{2C_c} \\ \frac{\omega T^2}{2C_c} & \frac{T}{C_c} \end{pmatrix} \quad (12)$$

3. PROPOSED DEAD BEAT CONTROL SYSTEM WITH DISTURBANCE OBSERVER

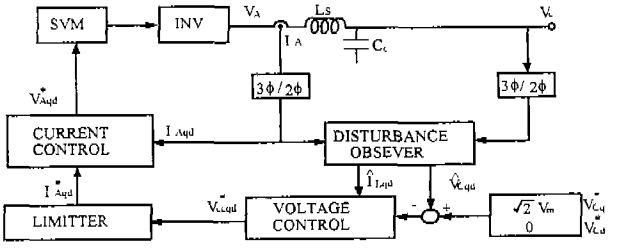


Fig.2. The control block diagram with disturbance observer.

Fig. 2. shows the proposed double dead beat control system with the disturbance observer. The controller has the current control minor loop within the voltage control loop and disturbance observer which estimates load currents. In the voltage control loop, it is possible to cancel the disturbances without load current sensors.

Dead beat current controller

Equation (10) can be transformed into Eq. (13) and Fig. 3. represents the current control block diagram of Eq. (13). As shown in Fig.3, the current control loop includes the mutual coupling term on d-q synchronous reference frame.

$$Z\, I_{Aqd}(z) = K\, I_{Aqd}(z) + L\ V_{Aqd}(z) - L\ V_{Cqd}(z) \quad (13)$$

Therefore, the decoupling matrix L_d and K_{d1} of Eq. (14), (15) are included to decouple the coupling

elements $\frac{\omega T}{2L_s}$ within the coefficient matrix L of $V_{Aqd}(z)$ and ωT within coefficient matrix K of $I_{Aqd}(z)$.

$$L_d=\begin{pmatrix} 1 & \frac{\omega T}{2} \\ -\frac{\omega T}{2} & 1 \end{pmatrix} \tag{14}$$

$$K_{d1}=\begin{pmatrix} 0 & \omega L_s \\ -\omega L_s & 0 \end{pmatrix} \tag{15}$$

Adopting IP controller as Fig. 3, the open loop transfer function of current controller can be obtained as follows :

$$G_o(z)=\frac{N_1 z}{z-1}\frac{L}{z+K-N_2L} \tag{16}$$
$$=\frac{N_1Lz}{z^2+(K-N_2L-1)z-K+N_2L}$$

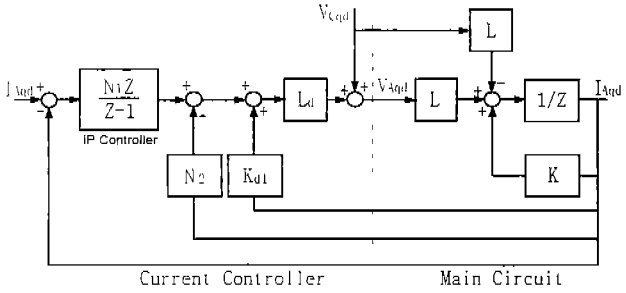


Fig. 3. Dead beat current control loop

To get dead beat control characteristic, the two roots of the closed loop transfer function needs to be placed on the origin of the z domain. Therefore, the gain N_1, N_2 of controller are derived as $N_1=\frac{L_s}{T}$, $N_2=\frac{L_s}{T}$

Disturbance observer

Assuming a state variable $I_{Lqd}(k)$ is constant for a sampling period, $I_{Lqd}(k+1)=I_{Lqd}(k)$ and the state equation for voltage control is derived as follows :

$$x(k+1)=Ax(k)+bu(k) \tag{17}$$
$$y=Cx(k)$$

where $x(k)=(V_{cqd}(k), I_{Lqd}(k))^T$ and

$$A=\begin{bmatrix} 1 & -\frac{T}{C_c} \\ 0 & 1 \end{bmatrix},\quad b=\begin{bmatrix} \frac{T}{C_c} \\ 0 \end{bmatrix},\quad c=[1,0].$$

From Eq. (17), the equation of observer to estimate load currents is given as Eq. (18) and Eq. (19) can be separated into d-q components.

$$\begin{bmatrix} \hat{V}_{cq}(k+1) \\ \hat{I}_{Lq}(k+1) \end{bmatrix}=\begin{bmatrix} 1 & -\frac{T}{C_c} \\ 0 & 1 \end{bmatrix}\begin{bmatrix} \hat{V}_{cq}(k) \\ \hat{I}_{Lq}(k) \end{bmatrix} \tag{18}$$
$$+\begin{bmatrix} \frac{T}{C_c} \\ 0 \end{bmatrix} I_{Aq}(k)+G\,(V_{cq}(k)-\hat{V}_{cq}(k))$$

where G is the observer gain vector and $G=[g_1\ g_2]^T$

Moreover, the characteristic equation of observer obtained from (18) is as follows :

$$ZI-A+GC=0 \tag{19}$$
$$Z^2+(g_1-2)Z+1-g_1-\frac{T}{C_c}g_2=0$$

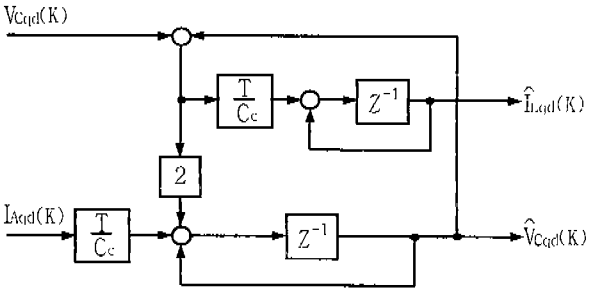


Fig. 4. The structure of dead beat disturbance observer

To achieve characteristics of observer operation by dead beat, the two roots of Eq. (19) must be zero. Therefore observer gain g_1 and g_2 is obtained as $G=[2,\ -\frac{C_c}{T}]^T$, which makes state variable to be estimated by observer for one sampling period. The gain of d axis component can be obtained as the same way in case of q axis component. Fig. 4. shows the structure of disturbance observer by dead beat.

Modified dead beat voltage controller

The voltage control loop includes the coupling terms on d-q synchronous reference frame too alike former case of current controller. Also, to decouple the coupling elements, decoupling matrix M_d and K_{d2} of Eq. (20), (21) is provided.

$$M_d=\begin{pmatrix} 1 & \frac{\omega T}{2} \\ -\frac{\omega T}{2} & 1 \end{pmatrix} \tag{20}$$

$$K_{d2}=\begin{pmatrix} 0 & \omega C_c \\ -\omega C_c & 0 \end{pmatrix} \quad (21)$$

Fig. 5 shows the block diagram of voltage control loop. If current minor loop is assumed to be ideal current source, feedforward loop of Fig. 5 compensates the generated disturbance.

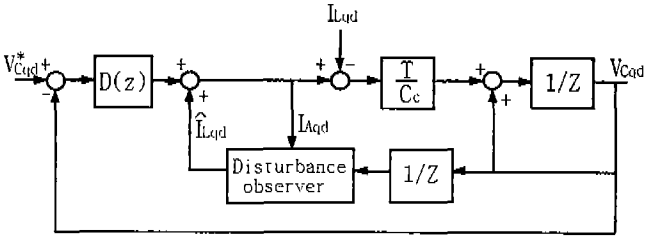


Fig. 5. Simple block diagram of voltage control loop.

In conventional case, the dead beat controller has the proportional function (P controller) but this function makes controller output to be oscillated. Therefore, in order to make system stable, the modified dead beat controller is proposed. The modified dead beat algorithm produces a first-order exponential response in an input step. When Eq. (22) is used as the output of voltage control loop, the output $y(t)$ can be transformed into a function of z domain as Eq. (23).

$$y(t)=(1-e^{\alpha t}) \quad (22)$$

where α is the time constant.

$$Y(z)=\frac{(1-e^{-\alpha T})}{(z-e^{-\alpha T})(z-1)} \quad (23)$$

Then simple open loop transfer function of voltage control loop is derived as follows :

$$G(z)=\frac{V_{Cqd}}{V^{*}_{Cqd}}=\frac{\frac{T}{C_c}z^{-1}}{1-z^{-1}} \quad (24)$$

If the unit feedback loop transfer function is expressed as $G_c(z)$ of Eq. (25), the voltage controller $D(z)$ in Fig. 5 is represented as (26)~(27).

$$G_c(z)=\frac{1-e^{-\alpha T}}{z-e^{-\alpha T}} \quad (25)$$

$$D(z)=\frac{G_c(z)}{[1-G_c(z)]G(z)} \quad (26)$$

$$D(z)=\frac{(1-e^{-\alpha T})(1-z^{-1})}{\frac{T}{C_c}(1-z^{-1})} \quad (28)$$

By using the modified voltage controller, most of oscillation of controller output is reduced and the stability of control system is improved. With the effect of improved controller, the dc-link voltage of PWM inverter can be reduced.

4. SIMULATION AND RESULTS

The system parameters for simulation are shown in table 1. The sampling period for real time processing is 100[usec] and the LC filter are designed in the view of the performance of controller and THD of output voltage waveform. To prove the validity of the proposed algorithm, simulation is executed for R-L linear and rectifier nonlinear loads, respectively. The results of simulation from proposed method are compared with the results from conventional one.

Fig. 6~7 shows the simulation results for R-L linear loads. The load currents in case that the power rating is changed from 20[%] to 100[%] and the output line-to-line voltages of UPS system and the control characteristics are displayed in Fig. 6 and Fig. 7 In each case, Fig. 6 is the result that disturbance observer is not included in the control loop. Fig. 7 represents the case from the proposed method. Fig. 6(a) shows that the line-to-line inverter output voltage are decreased in the instant that the power rating of load is increased. But, in Fig. 7(a), the output voltages are maintained consistently. Fig. 6(b) and Fig. 7(b) represent the comparison between the reference voltage and inverter output voltage on the rotationary d-q axes. In this case, it is shown that Fig. 6(b) has the steady state error comparing to the reference voltage and Fig. 7(b) shows that the steady state error is largely reduced.

Table 1. System parameter

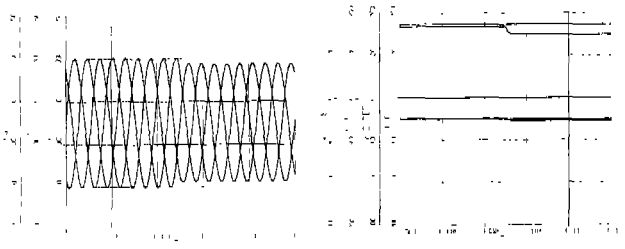
Ls : filter inductance	400 [uH]
Cc : filter capacitance	400 [uF]
V^{*} : reference peak voltage	179 [V]
Vdc : dc voltage	310 [V]
Ts : sampling period	100 [usec]
DC capacitor of rectifier load	4700 [uF]
inductance of R-L load	2 [mH]
rated load	5 [kVA]

Fig. 8~9 show the results of simulation for nonlinear rectifier loads. The load currents by diode rectifier, in case that the power rating is changed from 20[%] to 100[%]. Fig. 8 shows the case which directly compensates the load current by using sensors

and Fig. 9 represents the simulation results by proposed disturbance observer. In both two cases, (a) is the line-to-line inverter output voltage and (b) shows the reference voltage and inverter output voltage on the rotationary q axis. It is noticed that the compensating characteristic to compensate a sudden change of load currents are similar in both cases.

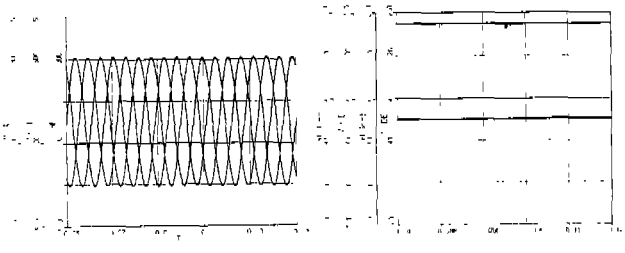
Fig. 10(a) shows the load current of rectifier by sensor and Fig. 10(b) represents the load current estimated by using disturbance observer. Here, it is proved that load currents can be estimated by disturbance observer with dead beat characteristic.

Fig. 11(a) shows the output signal of voltage controller by the modified dead beat controller and Fig. 11(b) is the case by conventional dead beat controller. Because the output of conventional dead beat controller includes much more oscillation and ripple, the stability of system become lower and controller can not be operated at low dc-link voltage of PWM inverter. To improve this defect, the modified dead beat controller has been adopted in this paper. Therefore the modified dead beat controller confirms higher stability of control system and hence the UPS system can be operated normally with lower dc-link voltage than the case that conventional controller is used.



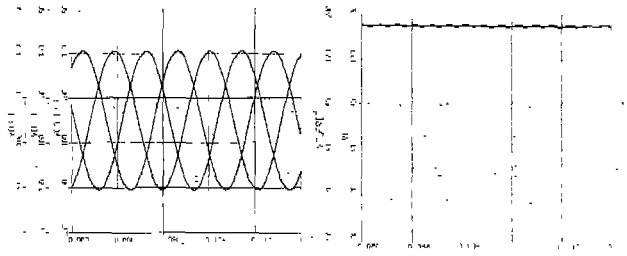
(a) (b)

Fig. 6. The result of simulation the case which remove the feedforward loop for compensating load current.
(a) Line-to-line voltage of Inverter (b) reference voltage and inverter voltage on the rotationary d-q axes.



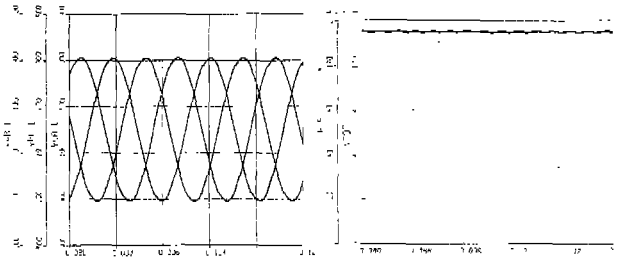
(a) (b)

Fig. 7. The result of simulation in case which compensate the load current by proposed disturbance observer.
(a) Line-to-line voltage of Inverter (b) reference voltage and inverter output voltage on the rotationary d-q axes.



(a) (b)

Fig. 8. The result of simulation in case which compensate the load current by sensing load current directly (a) Line -to-line voltage of Inverter (b)reference voltage and inverter voltage on the rotationary q axis.



(a) (b)

Fig. 9. The result of simulation in case which compensate the load current by proposed disturbance observer for nonlinear load. (a) Line-to-line voltage of Inverter (b) reference voltage and inverter voltage on the rotationary q axis.

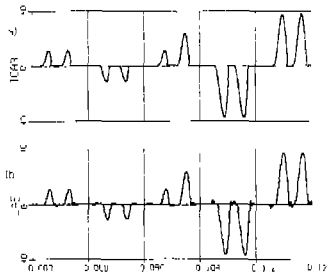
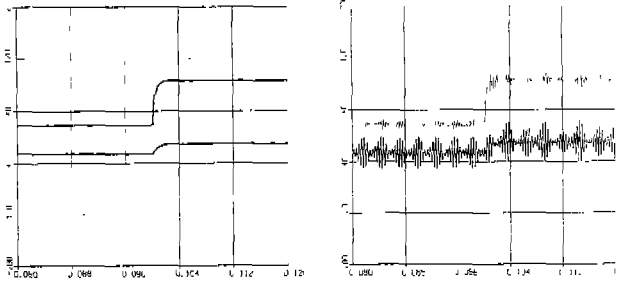


Fig. 10. The comparison the load current to the estimated load current by disturbance observer (a) load current (b) estimated load current.



(a) (b)

Fig. 11. The output value of modified and conventional dead beat controller (a) Modified dead beat controller (b) Conventional dead beat controller

5. CONCLUSIONS

In this paper, a novel digital control method, which is accomplished with modified dead beat controller and disturbance observer, is purposed. The current and voltage control loop consist of dead beat controller and disturbance observer which estimate the load currents. In the major loop, the disturbances are cancelled without load current sensor by using disturbance observer. And also, to remove a defect of oscillation generated in output of conventional dead beat controller, a modified dead beat algorithm is proposed in this paper. Therefore proposed control method reduces THD of output voltage, and improves transient response characteristics of controller.

ACKNOWLEDGEMENT

This work was supported by a grant No.962-0701-01-3 from Korea Science and engineering Foundation.

6. REFERENCE

[1] T. Kawabata et al.,"deadbeat control Three Phase PWM Inverter", IEEE Transaction Power Electronics. vol 5. p.p21-28 Jan. 1990

[2] T. Kawabata et al. "Digital Control of Three-phase PWM Inverter with LC Filter", IEEE Transaction Power Electronics. vol 6. p.p62-72 Jan. 1991

[3] J.G. Hwang, S.Y. Lee, G.H. Choe, "A Novel Detecting Noise Reduction Scheme for Voltage-Regulated Current Fed Power Filter", IEEE Proc. PESC'96, pp. 1047-1052, June. 1996

[4] Youichi Ito et al., "Digital Control of Three-phase PWM Inverter for UPSs Using deadbeat Observer", PCC-Yokohama '93, p.p79-84 1993

[5] K. P. Gokhale, A. Kawamura, and R. G. Hoft, "Deadbeat microprocessor control of PWM inverter for sinusoidal output waveform synthesis", in Proc. IEEE PESC., Toulouse, France, 1985, pp.28-36

[6]Maciej TONDOS, et al. "A MICRO PROCESSOR - BASED SPEED REGULATOR USING STATE AND DISTURBANCE OBSERVER", EPE'97, Trondheim, p.p 4626-4631

[7]Atsuo Kawamura, et al., "Digital Control of Induction Motor current with Deadbeat respnse using Presictive state Obserber". IEEE Transction Power Electronics, vol. 7, NO. 3, July 1992