ANALYSIS OF THREE-ARM PWM UPS

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ABSTRACT – A three-arm PWM UPS is realizable low price and small size UPS. In this UPS configuration, the center arm operates in both PWM converter mode and PWM inverter mode. Therefore, the operation of this UPS differs from the conventional UPS. In this paper, the three-arm PWM UPS is analyzed and a trial product is realized.

I. INTRODUCTION

As uninterruptible power supply (UPS) systems are used to critical loads including computers and network servers, a demand for UPS of a few kVA rating is recently increasing. For the UPS, miniaturization, low price, and communication function for computers are required.

For that, it is necessary for UPS the power circuit with high frequency switching, minimized parts numbers and computerizd control circuit. Then we propose all arms of conventional Three-arm Inverter/Converter[1][2] operate high frequency PWM, and the wave-form controllers consist of analog and digital control them. This UPS is called three - arm PWM UPS.

II. OPERATION ANALYSIS

In this section, analysis of operation is discribed to realize the three-arm PWM UPS. The load of the three-arm PWM UPS is assumed as a current source i_o to keep generality. The IGBT's of each arm in Fig. 1 are turned on or turned off alternately. Therefore, the circuit operation is divided into 8 states in Fig. 2.

The gate signals of IGBT are generated by means of

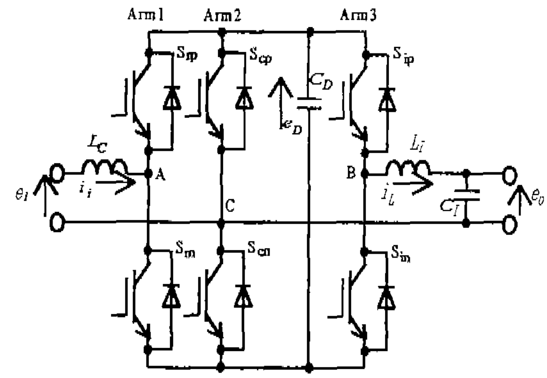

Fig.1 Power circuit of 3 arms PWM UPS

comparing the gate control signal u_r, u_c, and u_i with triangle-wave carrier as shown in Fig. 3. u_r, u_c, and u_i mean the gate control signals of Arm 1, Arm 2, and Arm 3. The amplitude relationship of u_r, u_c, and u_i are divided into 6 modes in Fig. 3. The duty ratio d_k (k is r, c and i) of IGBT S_{kp} is

$$d_k = \frac{1}{2}(1 + u_k). \qquad \cdots\cdots(1)$$

The state space averaging equations of each mode are derived using d_k, then these equations are all the same, it is

$$\frac{d\hat{x}}{dt} = A\hat{x} + be_i + wi_O. \qquad \cdots\cdots(2)$$

where,

$$\hat{x} = \begin{bmatrix}\hat{i}_i & \hat{e}_D & \hat{i}_L & \hat{e}_O\end{bmatrix}^T$$

$$A = \begin{bmatrix} 0 & -(d_r - d_c)/L_C & 0 & 0 \\ (d_r - d_c)/C_D & 0 & -(d_i - d_c)/C_d & 0 \\ 0 & (d_i - d_c)/L_I & 0 & -1/L_I \\ 0 & 0 & 1/C_I & 0 \end{bmatrix}$$

$b = [1/L_C \quad 0 \quad 0 \quad 0]^T$, $w = [0 \quad 0 \quad 0 \quad -1/C_I]^T$

$\hat{x}$ is averaging the state vector x.

By the way, (2) is divided into two state averaging equations of PWM converter and PWM Inverter by state space vectors of these, they are,

$$\frac{d\hat{x}_r}{dt} = A_r \hat{x}_r + b_r e_i + w_r i_L \qquad \cdots\cdots(3.1)$$

$$\frac{d\hat{x}_i}{dt} = A_i \hat{x}_i + b_i e_D + w_i i_O \qquad \cdots\cdots(3.2)$$

where,

$\hat{x}_r = [\hat{i}_i \quad \hat{e}_D]^T$ 、 $\hat{x}_i = [\hat{i}_L \quad \hat{e}_O]^T$

$$A_r = \begin{bmatrix} 0 & -(d_r - d_c)/L_C \\ (d_r - d_c)/C_D & 0 \end{bmatrix}$$

$$A_i = \begin{bmatrix} 0 & -1/L_I \\ 1/C_I & 0 \end{bmatrix}$$

$b_r = [1/L_C \quad 0]^T$, $b_i = [(d_i - d_c)/L_I \quad 0]^T$

$w_r = [0 \quad -(d_i - d_c)/C_D]^T$, $w_i = [0 \quad -1/C_I]^T$

Formulae (3.1) and (3.2) are the state space averaging equations of PWM converter and that of PWM Inverter. From these equations, it will be concluded that Arm 1 and Arm 2 constitute a PWM converter, and that Arm 2 and Arm 3 constitute a PWM inverter. As to PWM converter, the load is usually assumed as a resistance when PWM converter is analyzed alone, but load of PWM converter in the three-arm PWM UPS is PWM inverter. Therefore, it is found that the duty ratio of Arm 3 d_i has influence on the operation of PWM converter from third term $w\hat{i}_L$ of right side in (3.1). And as to PWM inverter, the DC voltage E_D is usually assumed as a voltage source when PWM inverter is analyzed alone, but the DC Voltage e_D of the three-arm PWM UPS is generated from PWM converter. These are common for all UPS's, not only for three arm circuit.

Therefore, to design of PWM converter and PWM

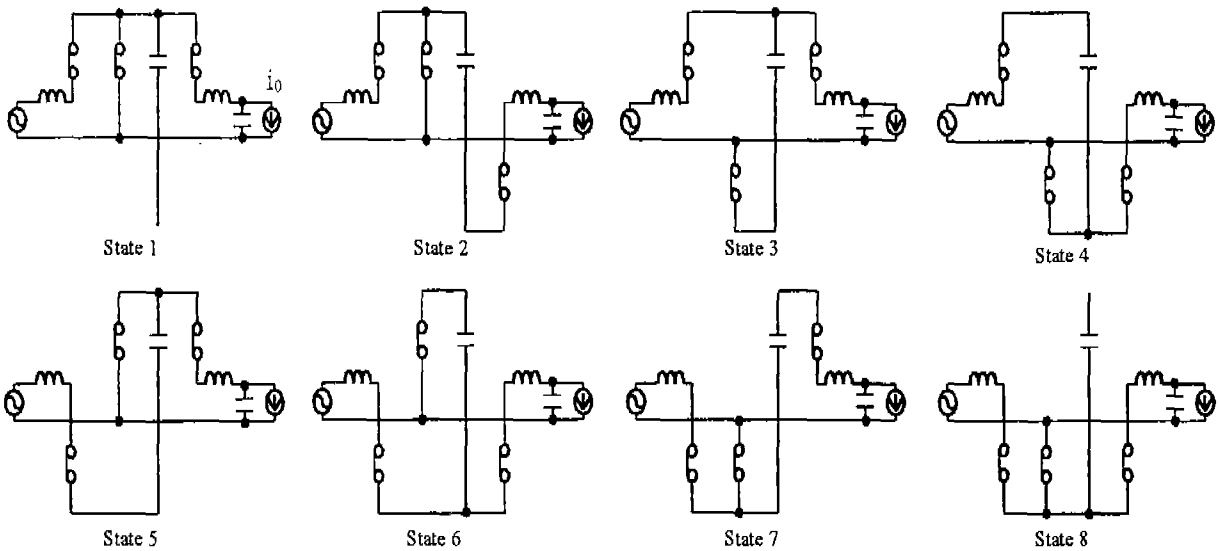

Fig.2 Equivalent circuit of each state

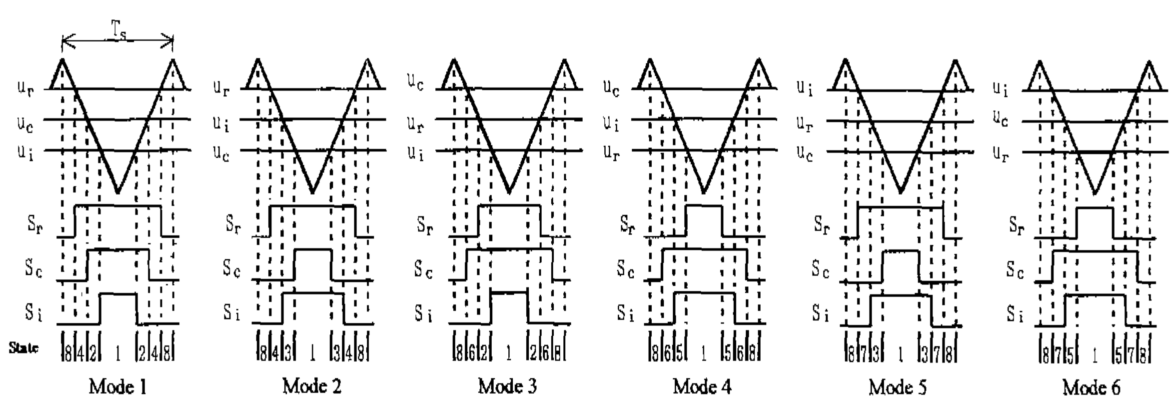

Fig.3 Operation modes

inverter in UPS, it is necessary that PWM converter connected PWM inverter is analyzed and that e_D is made no effect of the PWM inverter operation.

The static characteristic of e_D will be derived. The following assumption is used for the analysis. Now, the variables with hat are henceforth expressed without hat.

- The loss of the power circuit is ignored.
- The input current i_i and the output voltage e_O are controlled as

$$i_i = I_i \sin\omega t \text{ and } e_O = E_O \sin\omega t \quad \cdots\cdots\cdots(4)$$

which are synchronized with input voltage e_i ($= E_i \sin\omega t$)

The load of the PWM inverter is assumed a linear load as

$$i_O = I_O \sin(\omega t - \phi) \quad \cdots\cdots\cdots(5)$$

From (3.2), (4), and (5),

$$d_i - d_c = \frac{(1-\omega^2 L_I C_I)E_O \sin\omega t + \omega L_I I_O \cos(\omega t - \phi)}{e_D} \quad \cdots\cdots\cdots(6.1)$$

$$i_L = I_O \sin(\omega t - \phi) + \omega C_I E_O \cos\omega t \quad \cdots\cdots\cdots(6.2)$$

are derived. From (3.1) and (6.2),

$$d_r - d_c = \frac{E_i \sin\omega t - \omega L_C I_i \cos\omega t}{e_D} \quad \cdots\cdots(7.1)$$

$$e_D \frac{de_D}{dt} = \frac{K_{rip}}{C_D}\sin(2\omega t + \varphi) \quad \cdots\cdots\cdots(7.2)$$

where,

$$k_\alpha = \frac{1}{2}\{E_O I_O (1 - 2\omega^2 L_I C_I)\sin\phi - \omega C_I E_O^2 (1 - \omega^2 L_I C_I) - \omega L_I I_O^2 \cos 2\phi - \omega L_C I_i^2\}$$

$$k_\beta = \omega L_I I_O (I_O \sin\phi - \omega C_I E_O)\cos\phi$$

$$K_{rip} = \sqrt{k_\alpha{}^2 + k_\beta{}^2}$$

$$\varphi = \tan^{-1}(k_\beta / k_\alpha)$$

are derived. Considering the DC voltage component in e_D is E_D, (7.2) is solved as

$$e_D^2 = E_D^2 - \frac{K_{rip}}{\omega C_D}\cos(2\omega t - \varphi) \quad \cdots\cdots\cdots(8)$$

Here, C_D is determined by $E_D >> K_{rip} / \omega C_D$, because ripple voltage is small value. Therefore, the approximate equation of e_D is obtained as

$$e_D = E_D - \frac{K_{rip}}{2\omega C_D E_D}\cos(2\omega t - \varphi) \quad \cdots\cdots\cdots(9)$$

L_I, C_I, and L_C of the single phase UPS rating a few kVA are from 100 to 150μ. And if e_O is RMS 100V, E_D will be set to nearly 200V. Therefore, the amplitude of the ripple voltage (e_{Drip}) of e_D, E_{Drip} is given approximately

$$E_{Drip} = \frac{K_{rip}}{2\omega C_D E_D} \approx \frac{E_O I_O \sin\phi}{2\omega C_D E_D} \quad \cdots\cdots\cdots(10)$$

From (10), when C_D is large capacitance, (6.1) and (7.1) become the following equations.

$$d_i - d_c = \frac{(1-\omega^2 L_I C_I)E_O \sin\omega t + \omega L_I I_O \cos(\omega t - \phi)}{E_D} \quad \cdots\cdots\cdots(11.1)$$

$$d_r - d_c = \frac{E_i \sin\omega t - \omega L_C I_i \cos\omega t}{E_D} \quad \cdots\cdots\cdots(11.2)$$

Well, we examine the design method of d_C. It becomes clear that d_C have an effect on the wave form control of i_i and e_O from (11.1) and (11.2). Considering to make simple control system, d_C may be unrelated to the control of them. Therefore, d_C is decided as

$$d_C = \frac{1}{2}\left(1 - \frac{2E_M \sin\omega t}{E_D}\right) \quad \cdots\cdots\cdots(12)$$

where, E_M is constant.

The summary of the analytical results is shown below. PWM converter is composed of Arm 1 and 2 and PWM inverter is composed of Arm 2 and 3. When e_D is regarded as DC voltage source, PWM converter can be controlled only by Arm 1 and PWM inverter can be controlled only by Arm3.

III. OPERATION CONTROLLER

The operation controller of a UPS consists of the system controller which controls system operation, and the wave form controller which adjusts the wave form of output voltage, and so on. Generally, system control is performed by a micro computer. Further, in most case, a micro processor (MPU) is used for the wave form control also, for changing the set voltage easily, for monitoring operation state, and for improving the reliability due to integrated circuits.

The wave form controller of a UPS is required to control the input power factor, the DC voltage, the battery voltage drooping, the synchronization and the output voltage. The battery voltage drooping controller controls the battery charging current under the permitted value. The Output controller consists of the average value and the instantaneous value controllers. The average value controller controls the RMS value of e_O and the instantaneous value controller corrects its wave form.

In case of realizing a precise the wave form control, a digital signal processor (DSP) is usually used for its excellent calculation ability. But, the DSP wave form controller is much more expensive than the analog circuit wave form controller.

So, considering the response frequency of controller, we determined that the quick response controller should be realized by analog circuit, while the slow response controller should be realized by MPU. This combination, analog circuits and MPU, reduces the cost without expensive DSP and the performance is as excellent as DSP. The control block diagram is shown in Fig. 4. Accordingly, the input power factor controller and the instantaneous value controller should be analog circuit. The digital controller is realized by a program of MPU. The digital control algorithm is obtained by dispersing the mathematical controller models which are designed using Laplace transformation.

Ⅳ. DC VOLTAGE CONTROLLER

Except DC voltage control, the controller designed just like a single PWM converter and a single PWM inverter[4][5] as stated these controller in section Ⅳ. As to PWM converter, the load is resistance when PWM converter is analyzed alone, but load of PWM converter in the three-arm PWM UPS is PWM inverter. Therefore, DC voltage controller is different. In this section, DC voltage controller of the three-arm PWM UPS is analyzed.

From (3.1), the differential equation of e_D is obtained as

$$C_D \frac{de_D}{dt} = (d_r - d_C)i_i - (d_i - d_C)i_L \quad \cdots\cdots(13)$$

In case that L_I , C_I, and L_C are from 100 to 150μ, the conditions are given the following: 1>>$\omega L_I C_I$, E_O>>$\omega L_I I_O$ and E_i>>$\omega L_C I_i$. And the output voltage contoller controls $E_i = E_O$. Therefore, we can obtain,

$$d_r - d_C = d_i - d_C = \frac{E_O \sin \omega t}{e_D} \quad \cdots(14.1)$$

$$i_L = i_O \quad \cdots(14.2)$$

(14.1) and (14.2) are substituted for (13), it is obtained

$$C_D \frac{de_D}{dt} = \frac{E_O \sin \omega t}{e_D}(i_i - i_O) \quad \cdots\cdots(15)$$

To e_D can be regarded as DC voltage source, C_D is usually selected to a large value. The response frequency of e_D is lower than the frequency of commercial source. When the right side of (13) is approximated to DC component and the low frequency response is investigated, we obtain,

$$\frac{de_D}{dt} = \frac{E_O}{2C_D E_D} I_i - \frac{1}{C_D E_D} W_O \quad \cdots\cdots(16)$$

Where W_O is the output power. Therefore, the plant model of e_D is,

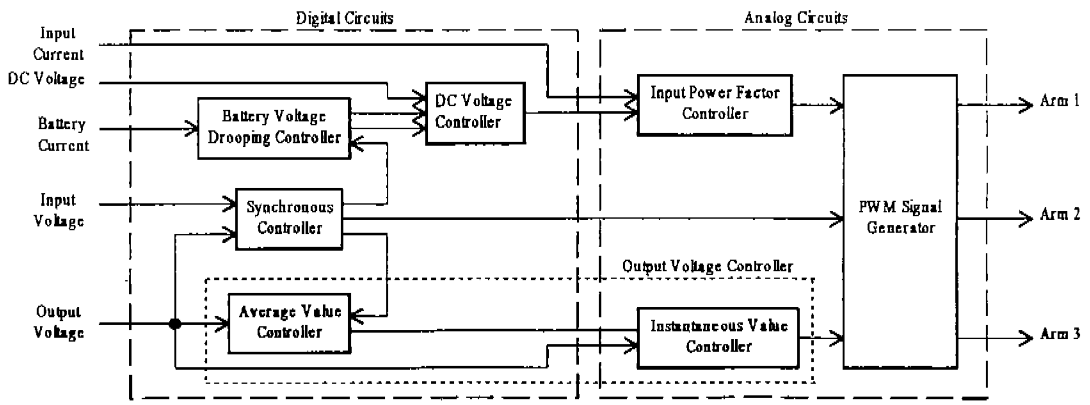

Fig.4 Control block diagram

$$e_D(s) = P_D(s) I_i(s) - D_D(s) W_O(s) \quad \cdots\cdots(17)$$

where,

$$P_D(s) = \alpha / s \quad D_D(s) = \beta / s$$

$$\alpha = \frac{E_O}{2C_D E_D} \quad \beta = \frac{1}{C_D E_D}$$

The second term of right side of (17) is a disturbance. When the effect of a disturbance is clear, the feedfowerd control[6] is effective. W_O is calculated using a multiplier and a integrater realized analog circuits or a fast signal processing unit realized digital circuits. But a multiplier, a integrater and a fast signal processing unit are expensive. Therefore, DC voltage controller is realized in Fig. 5 without the feedfowerd control. In this figure, K_D is a gain, E_{Dref} is a DC voltage reference and $f_D(s)$ is a filter as

$$f_D(s) = \frac{1}{1 + s/\omega_{Df}} \quad \cdots\cdots(18)$$

And Bang is the Bang-Bang compensator. The Bang-Bang compensator has no effect on the stability of it, because the response frequency of the Bang-Bang compensator is set up much lower than $f_D(s)$. The detail of the Bang-Bang compensator is described later.

From Fig. 5, e_D is

$$e_D = \frac{(1 + s/\omega_{Df})(\alpha K_D E_{Dref} - \beta w_O)}{s(1 + s/\omega_{Df}) + \alpha K_D} \quad \cdots(19)$$

A denominator of (19) is a quadratic equation of s and all coefficients of its are positive. Therefore, the system is stable. From (19), the steady-state error ΔE_D is obtained as

$$\Delta E_D = \frac{2}{K_D E_O} W_O \quad \cdots\cdots(20)$$

If K_D increases value, ΔE_D decreases from (20). But K_D can not be made a large value, because the conpensator is realized by a 16 bit integer MPU.

So, the Bang-Bang compensator is used for minimization of ΔE_D. The processing of Bang is described as follows: First step is the filtering process u_B. Second step is determination of the output y_B. If u_B polarity after first process is positive, y_B is $(y_B - \lambda)$. If u_B polarity after first process is negative, y_B is $(y_B + \lambda)$. λ is like a gain of Bang-Bang compensator. This process is a suspected integration. Therefore, ΔE_D is zero.

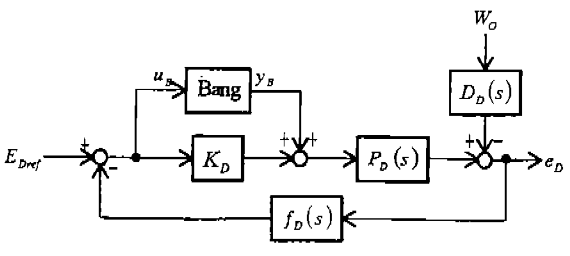

Fig.5 DC Voltage controller

V. THREE-ARM PWM UPS REALIZATION

Based on the study in section II, III and IV, a three-arm PWM UPS is manufactured for trial. The specification of the trial product is as follows: input and output voltages 100[Vrms], DC Voltage E_D=218[V] and output capacity W_O=5[kW]. The trial product is operated by single MPU which controls the system and monitors operating state, and operates a part for the mentioned wave control. The specification of the MPU is one chip micro computer for motor drive, integrated 16bit, and 16 megahertz operating frequency. The circuit parameters are L_C and L_I=120[μH], C_D=20.4[mF], and C_I=60[μF]. The DC control parameters are K_D=4 and ω_{Df}= 18.9 [rad/s]. The performance wave forms are shown in Fig.6. As the result for the examination of the trial product, it was found that a three-arm PWM UPS is realized.

VI. CONCLUSIONS

In this paper, the three-arm PWM UPS is analyzed and a trial product is realized, and it was found that the trial product UPS achieved basic performance. And attention paid for the fact that the operation models of PWM inverter and PWM converter of UPS are different from a single PWM inve rter and a single PWM converter

As the future theme, the UPS performance in case of rapid change of the input frequency must be investigated.

ACKNOWLEDGMENT

The authors would like to thank Messrs. Sugimori of Nippon Electric Industry for valuable support.

REFERENCES

[1]D. M. Divan; "A New Topology for Single Phase

UPS Systems",IEEE-IAS Conf. Rec., pp931-936,(1989)
[2]I.Ando, et. al., "Development of a High Efficiency Flywheel UPS us ing 3 Arms Inverter/Converter", T. IEE Japan,Vol.116-D,No.11,pp1153-1158,(1996)
[3]T.Uematsu, et. al. ,"Analysis of Three Arms PWM UPS", Technical Report of IEICE, EE97-74, (1998)
[4]Y.Komatsuzaki, et. al. ,"A Design Method of Control System for 3 Phase PWM Inverter", Technical Report of IEICE, PE92-44, (1992)
[5]T.Uematsu, et. al. ;" A Design Method for a 3 Phase PWM Converter", Trans. IEICE B-1, Vol. J78-B-1, No.11, pp621-627, (1995)
[6]K.Sakai, et. al. ,"Contr ol Method for Reduction of DC Link Capacitor and Restarting at Instantaneous Power Failure in PWM Converter", T. IEE Japan, Vol.112-D, No.1, pp29-37, (1992)

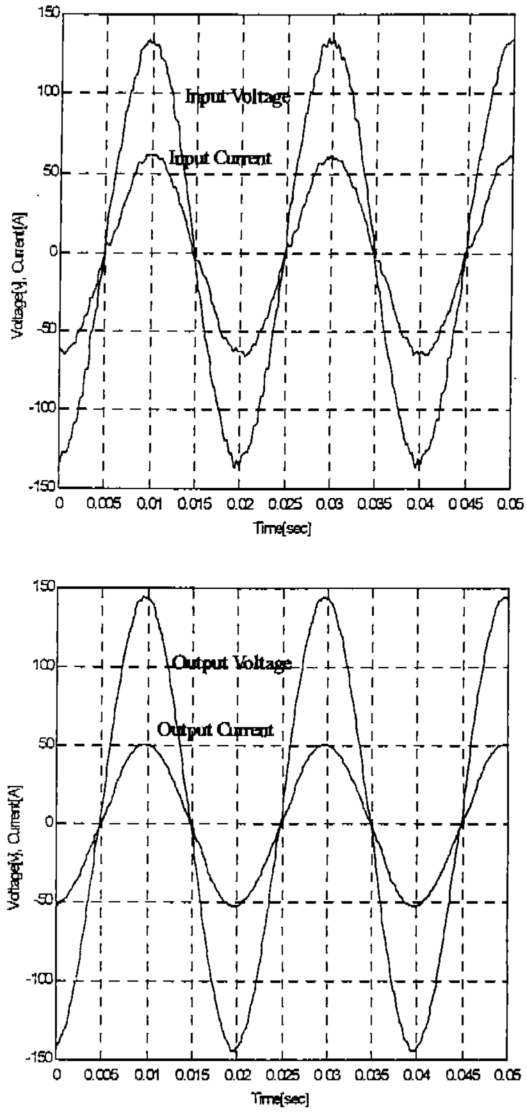

Fig.6. The performance waveform