Single Stage Power Factor Correction Using A New Zero-Voltage-Transition Isolated Full Bridge PWM Boost Converter

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ABSTRACT

A novel zero-voltage-transition (ZVT) isolated PWM boost converter for single stage power factor correction (PFC) is presented to improve the performance of the previously presented ZVT converter[8]. A simple auxiliary circuit which includes only one active switch provides zero-voltage-switching (ZVS) condition to all semiconductor devices. (Two active switches are required for the previous ZVT converter.) This leads to reduced cost and simplified control circuit comparing to the previous ZVT converter. The ZVS is achieved for wide line and load ranges with minimum device voltage and current stresses. Operation principle, control strategy and features of the proposed converter are presented and verified by the experimental results from a 1.5 kW, 100 kHz laboratory prototype.

I. Introduction

The conventional two stage power factor correction converter consists of a boost power factor correction circuit followed by an off-line dc/dc converter to provide a regulated and isolated dc output [1]. This approach, however, is inefficient and costly, since the power is converted twice. The overall system is rather complex because both need their control circuits, sensing circuits, protection circuits, etc. The single stage approach was suggested to achieve both input power factor correction and direct conversion from the ac line to the desired dc output[2-5,8]. By reducing one power stage, the overall system becomes simple, low cost and efficient comparing to the two stage approach. One disadvantage is that the low frequency ripple (twice of line frequency) exists in the output. So, this approach can be effectively used for the applications where the tight output regulation is not necessary, such as battery charger or dc bus in the distributed power systems.

A number of single stage PFCs have been suggested [2-5,8]. Most of them, however, show some disadvantages. A zero-current-switching (ZCS) quasi resonant SEPIC converter is used [2] to achieve single stage PFC however its available power range is very low because of very high device voltage and current stresses. A ZVS full bridge converter adopting an actively clamped resonant dc-link is used [3]. This converter also has disadvantages such as high device voltage and current stresses, and subharmonics in the line current. An IGBT based soft switching isolated converter with the help of MOSFETs is used [4] however the soft switching is not completely achieved. A ZVT full bridge PWM converter is presented [5,8] for single stage PFC (see Fig. 1(a)). Distinctive advantages including minimum device voltage and current stresses and wide ZVS range make it possible to use for high power applications (1-10 kW). The auxiliary circuit, however, includes two active switches and four diodes for blocking the body diodes of the MOSFETs. This leads to the considerable increase of the cost of the proposed converter.

In this paper, a novel ZVT full bridge PWM boost converter is presented (see Fig. 1(b)) for single stage PFC to improve the performance of the previously presented ZVT full bridge PWM converter. The basic topology and most of the switching characteristics are the same as those of the previous ZVT converter. A simple auxiliary circuit [7,10] which includes only one

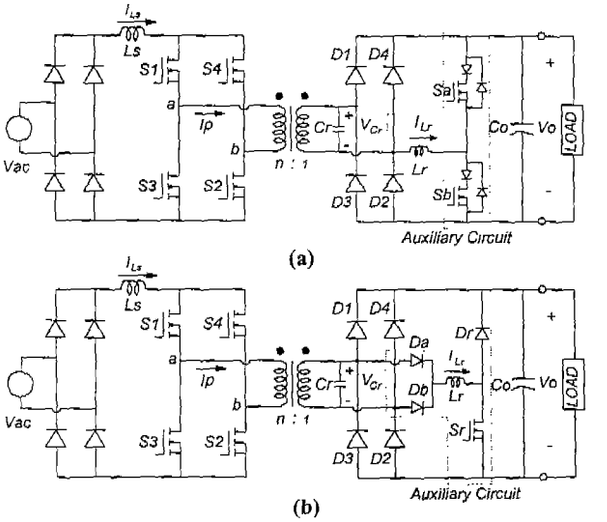

Fig. 1 Circuit topology of the proposed ZVT current fed full bridge PWM converter for single stage PFC: (a) previous converter[8], (b) proposed converter.

active switch and three diodes is added to provide ZVS condition to all semiconductor devices. This leads to lower cost and simpler control circuit. The PWM operation of the proposed converter can be achieved under minimum device voltage and current stresses. The ZVS is achieved for almost all line and load ranges.

Operation, control strategy and features of the proposed converter are presented and verified by the experimental results from a 1.5 kW, 100 kHz prototype.

II. Principle of Operation

To simplify the operation of the proposed converter, all devices and components are assumed ideal (zero transformer leakage inductance) and the ac input voltage is treated as a constant dc source during a switching period. Fig. 2 shows operational mode diagrams of the proposed converter. One operating half-cycle can be divided into seven modes and conduction paths in the converter circuit for each mode are denoted by solid line. Fig. 3 shows the corresponding waveforms for each mode.

Mode 1: All primary switches are turned on and the input inductor current I_{Ls} is linearly increased with the initial current I_1 as follows:

$$I_{Ls}(t) = \frac{V_s}{L_s} t + I_1. \qquad (1)$$

The inductor current at the end of this mode can be given by

$$I_{Ls}(T_{M1}) \equiv I_2, \qquad (2)$$

where, T_{M1} is the time interval of mode 1.

Mode 2: After on-duty period, the cross part switches S2, S3 are turned off. The input inductor current charges the resonant capacitor C_r up to V_o. The resonant capacitor voltage is given by

$$V_{Cr}(t) = \frac{nI_2}{C_r} t, \qquad (3)$$

where, n is transformer turns ratio. The time interval of this mode T_{M2} is obtained from the condition of $V_{Cr}(T_{M2})=V_o$ as follows:

$$T_{M2} \equiv \frac{C_r}{nI_2} V_o. \qquad (4)$$

Mode 3: The resonant capacitor voltage is clamped by the output voltage with the conduction of secondary bridge diodes D1, D2. The input inductor current is linearly decreased as follows:

$$I_{Ls}(t) = I_2 - \frac{nV_o - V_s}{L_s} t, \qquad (5)$$

if the variation of the input current during mode 2 is negligible.

The inductor current at the end of this mode can be given by

$$I_{Ls}(T_{M3}) = I_2 - \frac{nV_o - V_s}{L_s} T_{M3} \equiv I_3. \qquad (6)$$

Mode 4: To terminate from the off-duty period, the off-state primary switches S2, S3 should be turned on. To provide ZVS conditions to the secondary diodes to be turned off as well as primary switches to be turned on, the auxiliary switch Sr is turned on and then the resonant inductor current is linearly increased up to nI_{Ls}. This turn-on process is not a hard switching rather a zero current swtching since there is no diode reverse recovery involved in the switch pair, Sr-Dr and no current in the switch during turn-on period. The I_{Lr} and I_{Ls} are given by

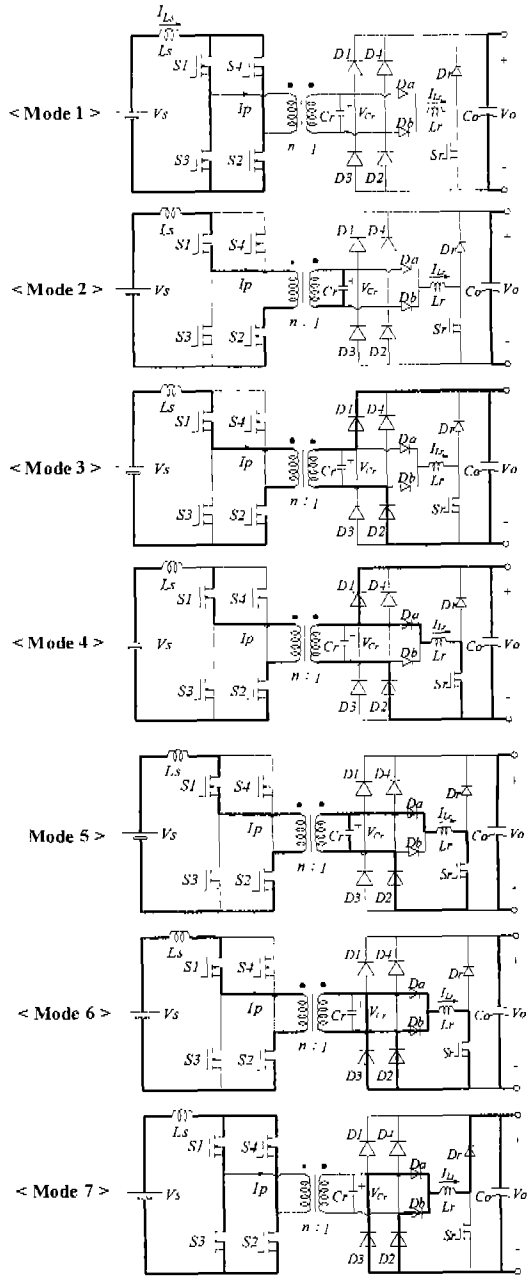

Fig. 2 Operation mode diagrams of the proposed converter.

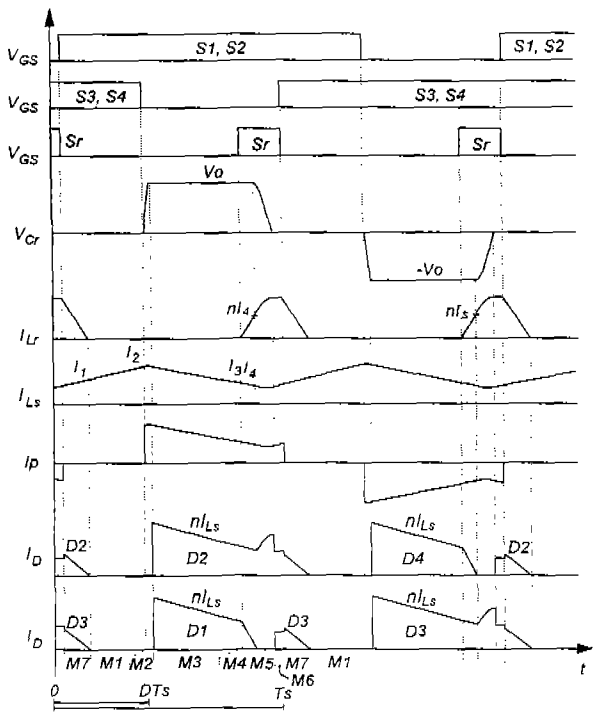

Fig. 3 Operation waveforms of the proposed converter.

$$I_{Lr}(t) = \frac{V_o}{L_r} t \,. \qquad (7)$$

$$I_{Ls}(t) = I_3 - \frac{nV_o - V_s}{L_s} t. \qquad (8)$$

The time interval of this mode T_{M4} can be obtained from the condition of $I_{Lr}(T_{M4}) = nI_{Ls}(T_{M4})$ and I_{Ls} at the end of this mode can be given by

$$I_{Ls}(T_{M4}) \equiv I_4 \,. \qquad (9)$$

Mode 5: When the I_{Lr} reaches nI_4, the secondary diode D1 is turned off with ZVS as shown in Fig. 2. Then, the L_r and C_r start to resonate and the V_{Cr} is decreased until it reaches zero. The I_{Lr} and V_{Cr} are given by

$$I_{Lr}(t) = \frac{V_o}{Z_r} \sin(\omega_r t) + nI_4 \,, \qquad (10)$$

$$V_{Cr}(t) = V_o \cos(\omega_r t) \,, \qquad (11)$$

where, $Z_r = \sqrt{L_r / C_r}$. $\omega_r = 1/\sqrt{L_r C_r}$. From the condition of V_{Cr} (T_{M5}) = 0, the T_{M5} is obtained as follows:

$$T_{M5} = \frac{\pi}{2} \sqrt{L_r C_r} \,. \qquad (12)$$

Mode 6: When the V_{Cr} reaches zero, the diode D3 starts to conduct. The resonant inductor current freewheels though D3-Da and D2-Db while the input inductor current I_{Ls} flows through D2-D3. During this mode, the primary voltage is always zero and the off-state switches S2, S3 can be turned on with ZVS condition. The time interval of this mode gives some margin for the switch gating signal. This interval has to be properly decided since long interval increases the conduction loss of the auxiliary circuit as well as the safety in switching.

Mode 7: The primary switches S2, S3 are turned on with ZVS condition. The I_{Ls} starts to increase again. The auxiliary switch Sr is turned off to recover the stored energy in the resonant inductor to the output capacitor. This turn-off process is the same as that of the ZVS. The resonant inductor current is recovered to the output capacitor through D3-Da-Lr-Dr and D2-Db-Lr-Dr until it dies out as follows:

$$I_{Lr}(t) = \frac{V_o}{Z_r} + nI_4 - \frac{V_o}{L_r} t \,. \qquad (13)$$

The time interval of this mode T_{M8} is obtained from the condition of $I_{Lr}(T_{M8}) = 0$ as follows:

$$T_{M8} = \frac{L_r}{V_o} \left(nI_4 + \frac{V_o}{Z_r} \right). \qquad (14)$$

One operating half-cycle is completed at the end of this mode.

III. Control Strategy

The main control object is to shape the line current into a sine wave keeping in phase with the line voltage and regulate the output voltage to the desired reference. The overall control block diagram is shown in Fig. 4. The ac line current is shaped to follow a sinusoidal reference current which is in phase with the line voltage and has correct magnitude to supply the necessary power to the load. Therefore, the current reference is obtained by sensing the line voltage as shown in Fig. 4. The regulation of output voltage is accomplished by varying the amplitude of the input current reference, which is done by using a multiplier.

The output voltage of the simple boost converter should be higher than the input. In the proposed converter, the output voltage can be controlled even lower than the input. The transformer turns ratio makes it possible.

There are a couple of control algorithms for PFC. Among them, nearly all algorithms can be used for the proposed converter. To test the performance of the proposed converter, one of the most popular algorithm, constant frequency PWM controller with average current mode control, is considered in this paper.

The output has a line frequency ripple which is determined by the capacitance of output capacitor. So, the output capacitor should be selected from the output voltage ripple requirement. The ripple voltage is obtained as follows:

$$V_{or} = \frac{2nI_{Lsp}}{3\pi^2 C_o} \,, \qquad (15)$$

where, I_{Lsp} is the peak value of I_{Ls}.

IV. Features of the Proposed Converter

A. Effective ZVS for Active and Passive devices

The feature of ZVS of the secondary diodes is somewhat different from that of the other ZVS converters [9], since the auxiliary circuit is inserted to the secondary rectifier side. The secondary rectifier diodes of the proposed converter are switched under both ZCS and ZVS conditions while the primary active devices are switched under ZVS condition only. This novel feature is very important for high voltage, high frequency applications because the dominant portion of switching loss in the high voltage, high frequency switching power supplies is generally generated from the diode reverse recovery loss rather than that of the active devices.

The switching waveforms of the diodes under several conditions are comparatively illustrated in Fig. 5. Fig. 5(a) shows the typical hard switching waveforms and it can be seen that the reverse recovery is quite serious problem, which results in a large amount of switching loss and EMI. Fig. 5(b) shows the switching waveforms under ZCS condition. The peak reverse recovery current is reduced but the some amount of switching loss is still remained. Rectifier diodes of most of ZVS full bride PWM converters are operated under ZCS. Fig. 5(c) shows the switching waveforms under ZVS condition. The peak reverse recovery current is high but the switching loss is decreased due to delayed reverse voltage. This happens when a snubber capacitor is added to the hard switching diodes. Fig. 5(d) shows the switching waveforms of the proposed converter which is turned off under both ZCS and ZVS conditions. For the upper two diodes, the diode current is slowly decreased to zero and the diode voltage is slowly increased after turn-off because of the resonance between Lr and Cr as shown in Fig. 5(d). For the lower two diodes, however, the turn-off mechanism is a little bit different, the diode currents in the both diode are also slowly decreased to zero and the diode voltage is also slowly increased after turn-off by the resonance between Lr and the equivalent junction capacitance of bridge diodes. In the actual circuit, the junction capacitances can be used for Cr without including additional capacitor. In this case, the turn-off waveforms of upper and lower diodes are exactly the same as shown in Fig, 5(d).

The switching loss is almost zero and EMI noise level is very low. So, the proposed converter can be operated in the range of high voltage, high frequency with high efficiency and low EMI noise.

The auxiliary circuit operates once a operating half-cycle, and its operation interval is very short comparing to the switching period. So, the rating of auxiliary devices can be small compared to the main devices and the conduction loss in the auxiliary circuit can also be small.

B. Simple Auxiliary Circuit

The auxiliary circuit [5,8] in the previous converter includes two active switches and four diodes for blocking the body diodes of MOSFETs. Even though the current rating of the auxiliary switches is much smaller than that of the main switches, usually 20-50%, adding two additional switches to achieve ZVS considerably increases the cost and the circuit complexity of the overall system. The auxiliary circuit adopted in this paper includes only one active switch and three diodes. Since one active switch and one diode with one gate driver are saved, the cost of overall system is much less than that of the previous.

C. Minimum Device Voltage and Current Stresses

The device voltage and current waveforms of the switches in the new converter are essentially square-wave except during the turn-on and turn-off switching

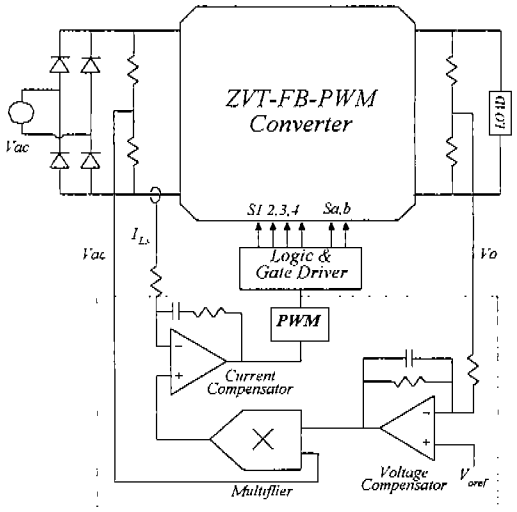

Fig. 4 Block diagram of the output voltage control with input power factor correction.

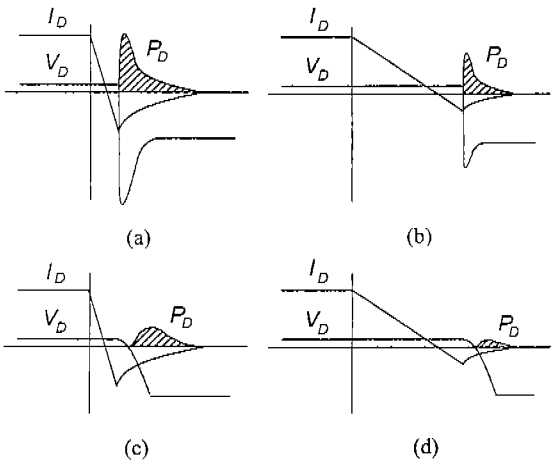

Fig. 5 Illustrative switching waveforms of diodes under the condition of (a) hard switching, (b) ZCS only, (c) ZVS only, and (d) both ZVS and ZCS.

intervals, when the zero voltage transition takes place. Both main switches and diodes are subject to almost minimum voltage and current stresses. The voltage stress of the auxiliary switch is also minimum. The peak current stress of the auxiliary switch is higher than the main switches however the RMS current stress is much lower.

D. Wide ZVS Range

For the most of ZVS full bridge converters, ZVS is achieved for rather narrow load ranges. Losing ZVS at light load usually generates considerable noise and EMI. This is one of the biggest drawback of the ZVS full bridge converters[9]. The proposed converter, however, is operated under ZVS for almost all line and load ranges due to the ZVT auxiliary circuit. The ZVS range of the proposed converter is the same as that of the original single ended ZVT boost converter.[11]

E. Circuit Variations

The proposed ZVT conversion concept shown in Fig. 1(b) can be extended for the center tapped transformer. According to the applications, low-voltage or high-voltage applications, the transformer structure can be changed as shown in Fig. 6. The original circuit shown in Fig. 1(b) is useful for high voltage input and high voltage output applications while the circuit of Fig. 6(a) is for the high voltage input and low voltage output applications; Fig. 6(b) is for the low voltage input and high voltage output applications; Fig. 6(c) is for the low voltage input and low voltage output applications. Most of operations of the these converters are the same as those of the original.

V. Experimental Results

A 1.5 kW, 100 kHz prototype has been built and tested to verify the operation principle of the proposed converter. The experimental circuit diagram with circuit parameters is shown in Fig. 7. A passive RCD clamp circuit is added in the primary side to clamp the primary switches voltage. A saturable reactor is also added in series with the resonant inductor to prevent the parasitic ringing between Lr and the output capacitance of the Sr. The transformer is designed with the turns ratio of 24:18 on the PQ5050 core and the measured leakage inductance is 1.3uH. UC3854N is used for the controller.

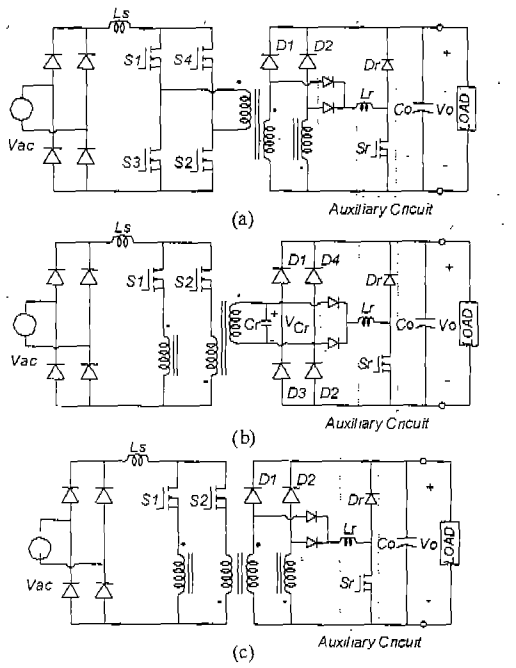

Fig. 6 Circuit Variations of the proposed converter.

Fig. 8 shows the experimental waveforms of the primary voltage and current, input inductor current, and resonant inductor current. It can be seen that all waveforms are quite clean due to complete ZVS and are well matched with the expected ones except the primary current waveform. The primary current waveform has rising and falling slops and looks a little different from that in the Fig. 3. This is caused by the uncounted transformer leakage inductance. The current handled by the auxiliary circuit is small comparing to the main switch current allowing a small power rating of the auxiliary circuit, about 20% of the full power. Fig. 9 shows the waveforms of the resonant capacitor voltage and secondary rectifier diodes currents. The diodes current waveforms also have rising and falling slopes but all waveforms are very clean. Fig. 10 shows the turn-on waveforms of a primary switch. It can be seen that the ZVS turn-on is completely achieved since the switch is turned on when the antiparallel diode is conducting. Fig. 11 shows the turn-off waveforms of a secondary rectifier diode. It can be seen that ZVS and ZCS are achieved at the same time and switching loss is almost zero.

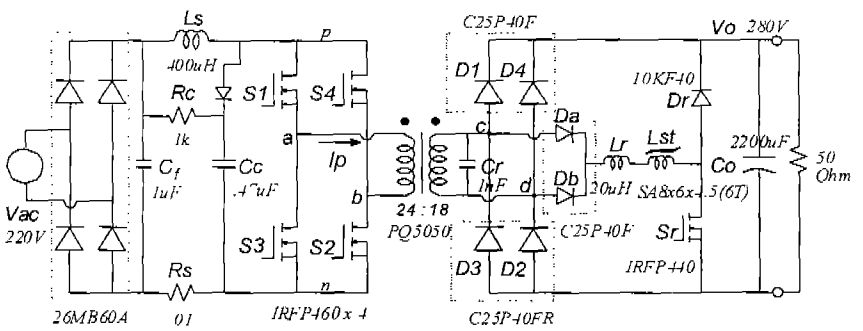

Fig. 7 Experimental circuit diagram of the proposed converter.

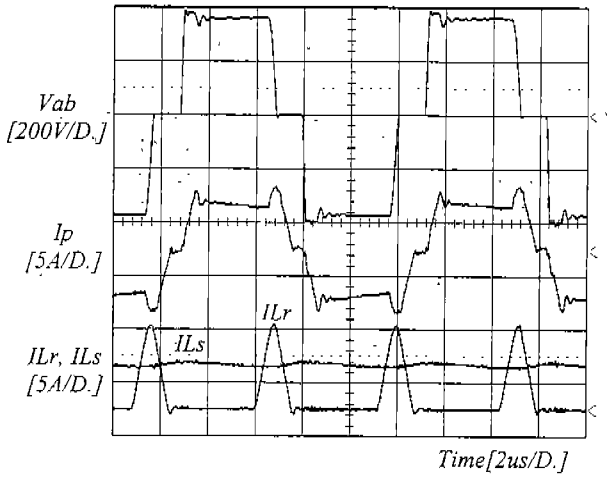

Fig. 8 Experimental waveforms of the primary voltage, input inductor current, and resonant inductor current.

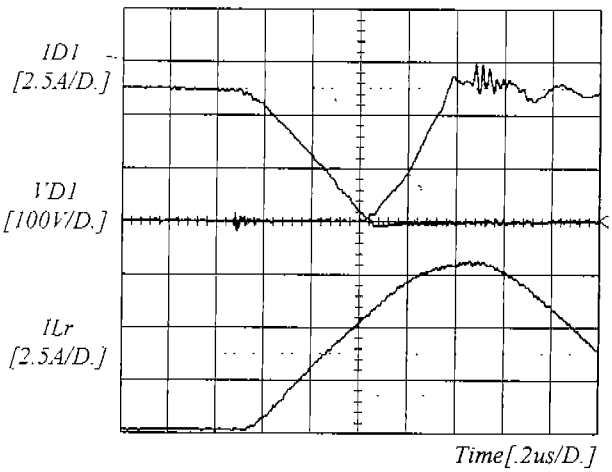

Fig. 11 Extended ZVS turn-off waveforms of the secondary rectifier diode (D2).

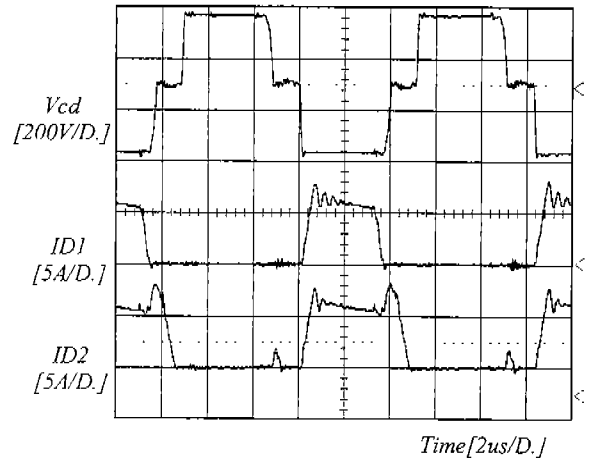

Fig. 9 Waveforms of the secondary voltage and rectifier diode currents.

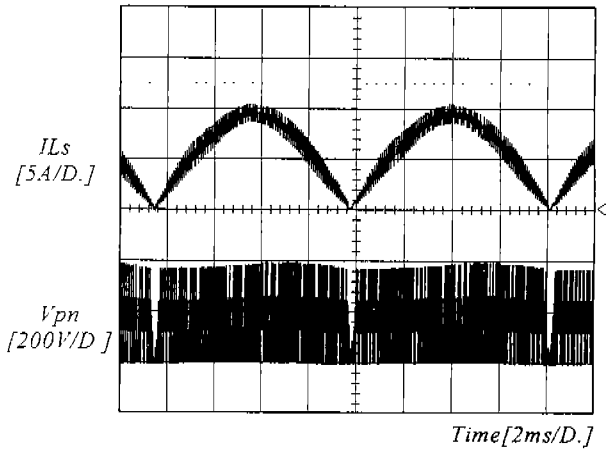

Fig. 12 Waveforms of input inductor current and voltage between p and n.

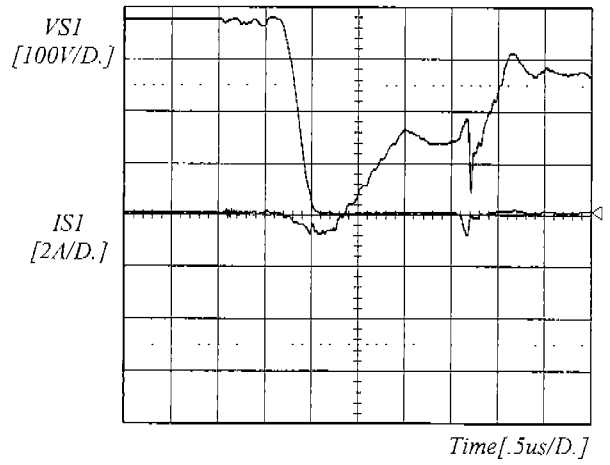

Fig. 10 Extended ZVS turn-on waveforms of the primary switch (S1).

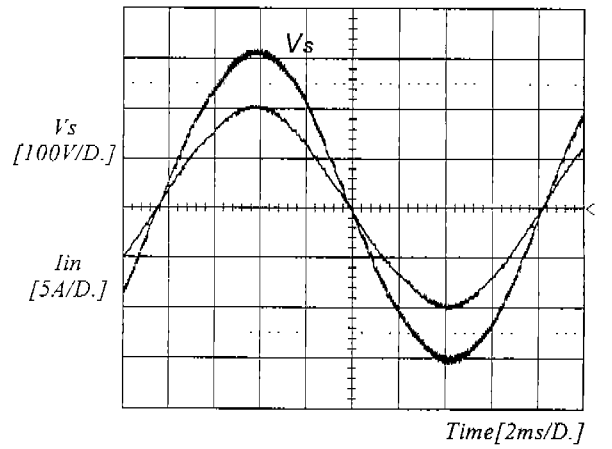

Fig. 13 Waveforms of input voltage and current.

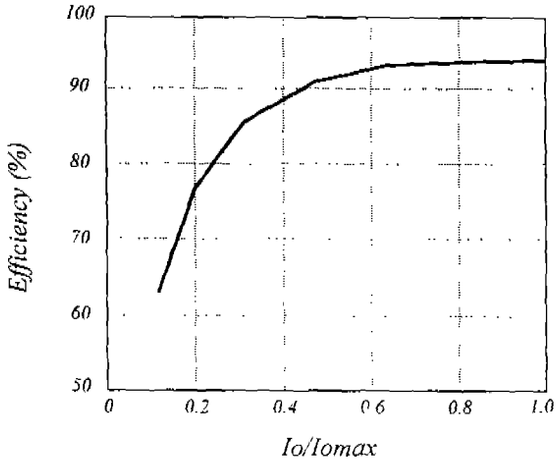

Fig. 14 Measured efficiencies according to the load variation.

Fig. 12 shows the waveforms of input inductor current and the voltage between p and n in the experimental circuit diagram. Fig. 13 shows the waveforms of input voltage and current. It can be seen that the input current waveform shows a sinusoidal in phase with input voltage and the crossover distortion is negligible. The measured input power factor is 0.99. Fig. 14 shows the measured efficiencies according to load variation. The efficiency at full load is about 93%.

VI. Conclusion

A novel zero voltage transition isloated PWM boost converter for single stage power factor correction is presented to improve the previously presented ZVT current fed full bridge PWM converter. Operation, analysis, control strategy, and features of the proposed converter are described and verified with the experimental results from the 1.5 kW, 100 kHz prototype. It is shown that the proposed converter provides both input power factor correction and direct conversion from ac line to the desired dc output with a single power stage. The modified circuits for the different applications are also presented.

By using a much simpler auxiliary circuit comparing to that of the previously presented ZVT current fed full bridge PWM converter, the overall system of the proposed converter becomes much simpler and the cost is considerably reduced. Distinctive advantages including ZVS for wide line and load ranges, low device voltage and current stresses, and simple circuit topology and low cost, the proposed converter can be effectively used for the applications where the tight output regulation is not necessary such as on board battery charger for electric vehicles or dc bus in the distributed power system.

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