Improved Zero Voltage and Zero Current Switching Full Bridge PWM Converter with Active Clamp

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ABSTRACT — An improved zero voltage and zero current switching (ZVZCS) full bridge (FB) PWM converter is proposed to solve the problems of the previously presented ZVZCS-FB-PWM converter with secondary active clamp such as narrow ZVS range of leading-leg switches [6]. By adding an auxiliary inductor in between the leading-leg and separated input source voltages, the ZVS of leading leg switches can be extended to the whole line and load ranges, which eliminates unwanted hard switching of clamp switch and simplifies its control. The principle of operation is explained and analyzed. The features and design considerations of the proposed converter are also illustrated and verified on a 3 kW, 100 kHz IGBT based experimental circuit.

I. Introduction

The performance of the IGBT has been improved continuously pursuing lower switching loss, lower conduction drop, and higher voltage and current ratings. The latest IGBTs can handle very high power rating (3300V/1200A) with low switching frequency (several kHz) [1] or low power rating (600V/50V) with high switching frequency (several tens kHz) [2]. Because of distinctive advantages such as easiness in drive and high frequency switching capability, IGBTs replaced most of BJTs. Moreover, IGBTs are replacing MOSFETs for the several or several tens kilo-watts power range applications since IGBTs have higher power density and lower cost comparing to MOSFETs. For the high frequency (about 100kHz) applications, MOSFETs are still superior to IGBTs since the maximum operating frequency of IGBTs, however, is usually limited by 20-30 kHz [1] because of their current tailing characteristic.

To apply IGBTs for high frequency applications, ZVS-FB-PWM converters can be considered. In these converters, the ZVS is simply achieved by introducing the phase shift between two legs (named leading-leg and lagging-leg) but the ZVS range of two legs is different. The ZVS range of leading-leg switches is wide enough while that of the lagging-leg switches is rather narrow. So, IGBTs can be effectively used for

leading-leg switches with additional snubber capacitors but not for legging-leg switches since the additional snubber capacitor further reduces the ZVS range and the ZVS may not be achieved even at full load.

To overcome this problem, a couple of ZVZCS-FB-PWM converter have been presented so far [4-8]. The ZVZCS means mixed mode operation of ZVS and ZCS, the ZVS is used for the leading-leg as the ZVS converters while the ZCS is used for the lagging-leg instead of the ZVS since the lagging-leg has narrow ZVS range. So, the ZVS mechanism of the leading-leg is exactly the same as that of the ZVS-FB-PWM converters. The ZCS of lagging-leg, however, is achieved by resetting the primary current during the freewheeling period. The primary current resetting is done with the different manners. In the first ZVZCS converter [4], the primary current is reset by using the dc blocking capacitor voltage and a saturable reactor. The saturable reactor loss and difficulty in cooling were found as disadvantages. In the converter [5], the primary current is reset by adding an active clamp in the secondary side. The primary current reset time can be minimized since high reverse voltage can be applied to the leakage inductance and thus, maximum controllable duty cycle can be increased. This is very important when the transformer can not be designed with low leakage inductance. In addition, there is no parasitic ringing in the rectifier. In spite of these advantages, this approach was known as unpractical since the clamp switch is operated twice of the rectifier frequency with hard switching. In the converter [7], a transformer auxiliary winding and auxiliary circuit is used to reset the primary current. Neither additional lossy components nor active switches are added. So, this circuit is efficient and cost effective but the secondary passive clamp circuit is still necessary. In the converter [8], a simple auxiliary circuit is added in the secondary side to reset the primary current and clamps the secondary rectifier voltage. Neither additional lossy components nor active switches are added. In addition, it is not necessary to add additional clamp circuit. So, this circuit is the most efficient and simple among the ZVZCS converters. For the converters [4-8], the primary current reset time is relatively long comparing to the converter with active clamp. So, the maximum

duty cycle will be considerably limited when the leakage inductance is large.

This paper proposes an improved ZVZCS-FB-PWM converter with the active clamp. By adding an auxiliary inductor in between in between the leading-leg and separated input source voltages, the ZVS of leading leg switches can be extended to the whole line and load ranges, which eliminates unwanted hard switching of clamp switch and simplifies its control. So, ZVS of clamp switch and rectifier diodes can be achieved and the operating frequency of the clamp switch is the same as that of the rectifier.

The basic operation and features of the proposed converter are described. A 3kW, 100 kHz prototype has been built using IGBTs (a MOSFET for the clamp switch) and tested to verify the principle of operation.
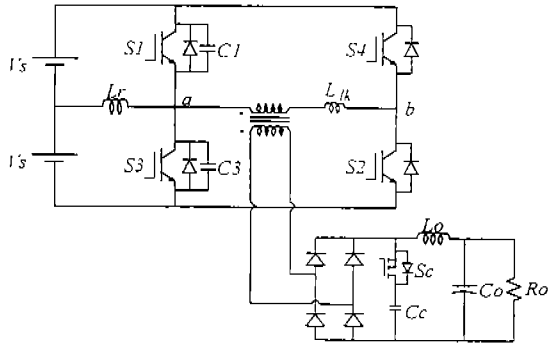

Fig. 1 Circuit topology of the proposed ZVZCS full bridge PWM converter.

II. Operation and Analysis

The basic structure of the proposed ZVZCS-FB-PWM converter is the same as that of the ZVZCS-FB-PWM converter with the active clamp[6]. The control of the primary switches is also the same, phase shift PWM control. To illustrate steady state operation, it is assumed that all components and devices are ideal and the output filter inductor current is constant and clamp capacitor is large enough to be treated as a constant voltage source during a switching period. The new converter has eight operating modes within each operating half-cycle. The equivalent circuits and operation waveforms are shown in Figs. 2 and 3, respectively.

Mode 1: S1 and S2 are conducting and the input power is delivered to the output. At the beginning of this mode, the rectifier voltage is clamped by Vc through the body diode of Sc. The stored energy in the leakage inductance which is generated by the resonance between the leakage inductance and parasitic capacitance of the rectifier diodes is recovered to the clamp capacitor. The primary current and the clamp capacitor current can be expressed as follows:

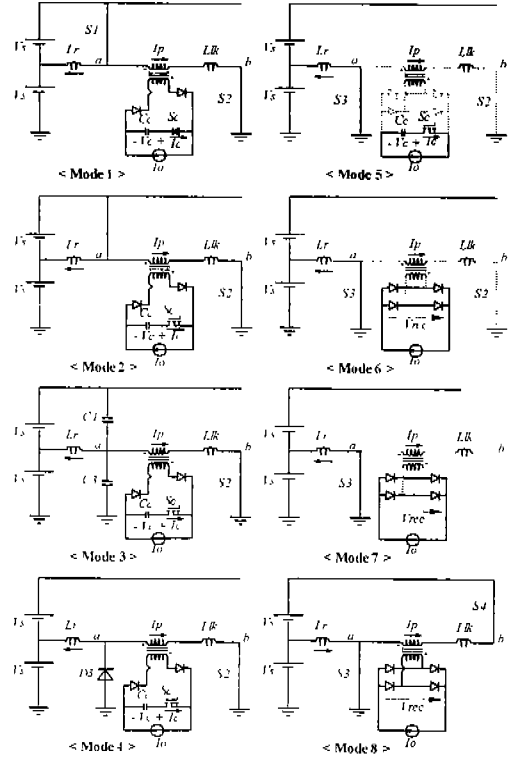$$I_p(t) = \frac{1}{L_{lk}}\left(V_s - \frac{V_c}{n}\right)\cdot t , \qquad (1)$$

Fig. 2 Operation mode diagrams for eight modes.

$$I_c = \frac{I_p}{n} - I_o , \qquad (2)$$

where, n is transformer turn ratio. The current of auxiliary inductor is also increased as follows;

$$I_{lr} = \frac{V_s}{L_r}\cdot t , \qquad (3)$$

The clamp switch can be turned on with ZVS during this mode.

Mode 2: The clamp switch current is decreased to zero and increased to the reverse direction for the charge balancing of clamp capacitor. The S1 and S2 are still on and the powering mode is sustained during this mode.

Mode 3: According to the given duty cycle, S1 is turned off and then, the stored energy in the leakage inductance and auxiliary inductor charges C1 and discharges C3. The secondary rectifier voltage is held by clamp capacitor voltage. So, the switch voltage is increased and the primary current is decreased as follows:

$$I_p(t) = \frac{A}{\omega_o^2} + \left[nI_o - \frac{A}{\omega_o^2}\right]\cos\omega_o t + \frac{V_s - \frac{V_c}{n}}{\omega_o L_{lk}}\sin\omega_o t , \quad (4)$$

where, $A = \dfrac{I_o}{nL_{lk}C_c} - \dfrac{I_{lr}}{L_{lk}(C_1 + C_3)}$, $n = \dfrac{n2}{n1}$,

$\omega_o = \sqrt{\dfrac{C_1 + C_3 + n^2 C_c}{L_{lk}(C_1 + C_3)n^2 C_c}}$, V_c is the initial voltage of Cc.

The turn-off process of S1 is almost loss less if the external capacitor is large enough to hold the switch voltage at near zero during the switch turn-off time.

Mode 4: After D3 starts conducting, S3 can be turned on with ZVS. The primary current freewheels through the D3 and S2 and the reflected clamp capacitor voltage is applied to the leakage inductance. Then, the primary current is linearly decreased with the slope of Vc/nL_{lk} and Ic is linearly increased satisfying (2). The primary current reaches zero at the end of this mode.

Mode 5: The rectifier diodes are turned off since the primary current is zero and Sc is still on. During this mode, the primary current sustained at zero and Cc supplies whole load current.

Mode 6: The Sc is turned off and then the rectifier voltage is dropped to zero. The load current freewheels through the rectifier itself. No current flows through the primary.

Mode 7: At the end of freewheeling mode, S2 can be turned off with ZCS. No tail current exists since all minority carriers are eliminated by recombination. This mode is dead time between S2 and S4.

Mode 8: To terminate from freewheeling mode, S4 is turned on. This turn-on process is also ZCS since the primary current can not be changed abruptly. The primary current Ip is linearly increased with the slop of Vs/L_{lk}. The rectifier voltage is still zero. At the end of this mode, the primary current reaches the load current nI_o and then the diagonal part of rectifier diodes are turned off with ZVS if a snubber capacitor is added to the rectifier. There is no diode reverse recovery in the rectifier. At the end of this mode, the rectifier voltage is abruptly increased. This is the end of an operating half-cycle.
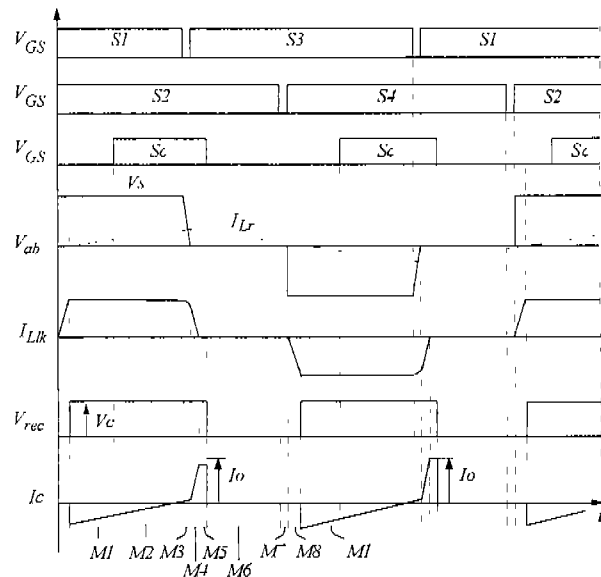
(Operation at Light Load)

At light load, the Mode 3 can be divided into two modes. The primary current can be reset before the resonant transition is completed, at light load. The

operation mode diagram is shown in Fig. 4 and detailed operation is as follows;

Mode 3a: After S1 is turned off, the currents in the leakage inductance and auxiliary inductor charges C1 and discharges C3 and the switch voltage is increased . The secondary rectifier voltage is held by clamp capacitor voltage. The primary current is decreased quickly and finally reset before the resonant transition is completed. The anti-parallel diode of S3 will not be turned on during this mode.

Mode 3b: After the primary current is reset, the snubber capacitors are charged/discharged by the auxiliary inductor current only. The rectifier voltage is still high and thus, there is no current in the primary. The anti-parallel diode of S3 will not be turned on during the end of this mode, providing ZVS condition to the S3.

Mode 4 : After D3 starts conducting, S3 can be turned on with ZVS.

Fig. 3 Operation waveforms.
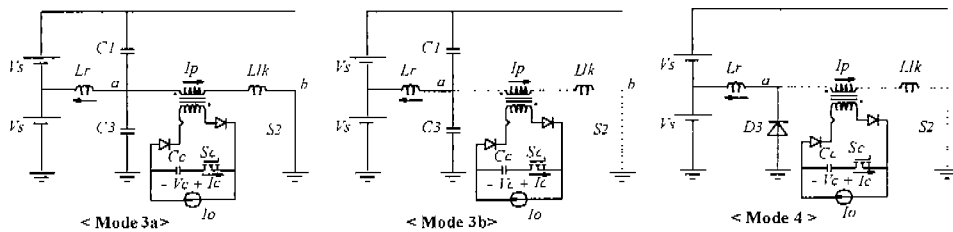
Fig. 4 Subdivided operation mode at light load.

III. Features of the Proposed Converter

A. Effective Soft Switching (ZVZCS)

In the previous ZVZCS-FB-PWM converter with an active clamp [5], the clamp switch can be turned on with ZVS during the powering mode and kept on after the power mode to reset the primary current. In this case, the ZVS range of leading-leg switches is quite

limited unless the stored energy in the leakage inductance is not enough to charge/discharge the snubber capacitors in the leading-leg. To obtain wide ZVS range of leading-lag switches, the turn-on of the clamp switch is delayed. During the powering mode, the clamp switch is kept off and then the clamp capacitor is charged through the body diode of clamp switch. If the charging is completed, the diode is off

and the rectifier voltage will be the nominal voltage. At the end of powering mode, the zero voltage transition of leading-leg is taken place by the same mechanism as that of the ZVS converters [3] and the other ZVZCS converters [4-8] and then the clamp switch is turned on to reset the primary current. Wide ZVS range can be achieved since the stored energy in the output filter inductor can be used. The clamp switch, however, is operated with hard switching and there is severe diode reverse recovery loss in the rectifier since the clamp switch is turned on during the rectifier diodes are conducting, that generates considerable noise and loss.

In the proposed converter, the clamp switch is turned on with ZVS during the powering mode and kept on until the primary current is reset and the ZVS of leading-leg switches is achieved mainly by the stored energy in the auxiliary inductor. So, the ZVS of leading-leg switches is achieved for whole line and load ranges. The clamp switch and the rectifier diodes are operated with ZVS by adding a snubber capacitor across the rectifier. So, the rectifier voltage waveforms are quite clean and low loss and low noise are achieved. Besides, the control of the clamp switch is quite simple, no sensing is required. Only a sacrifice is the increased conduction loss by the auxiliary inductor current.

B. Low Duty Cycle Loss

The waveforms of the primary and secondary rectifier voltages of the several converters are compared in Fig. 5.
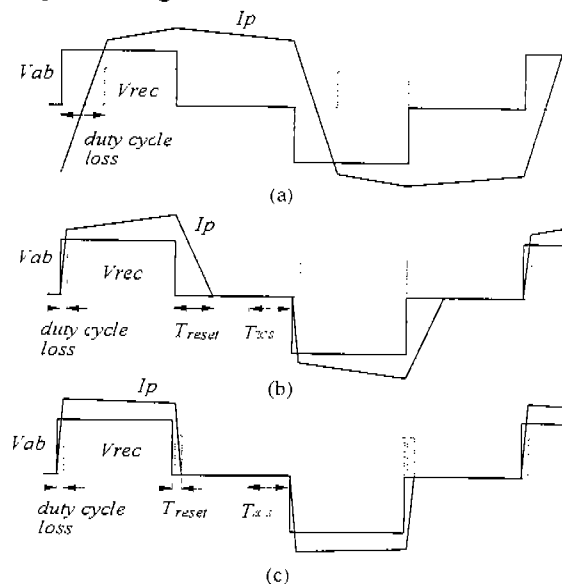

Fig. 5 Comparison of primary and secondary rectifier voltage waveforms: (a) ZVS-FB-PWM converter, (b) the other ZVZCS converters [4,6-8], (c) the proposed converter.

The ZVS-FB-PWM converters obviously have large duty cycle loss since the leakage inductance should be large enough to have reasonable ZVS range. In the ZVZCS converters, the maximum duty cycle is limited because of the primary current reset time and minimum dead time to achieve a complete ZCS of lagging-leg

switches, which is the minority carrier recombination time. The primary current reset time depends on the applied voltage to the leakage inductance during the freewheeling period. This reset time of the ZVZCS converters [4,6-8] is relatively long since low voltage (about 10-30% of Vs) is applied to the leakage inductance. In the proposed converter, the slightly higher voltage than Vs (nVc) is applied to the leakage inductance and very short reset time can be achieved. This allows increase of the maximum duty cycle and more reduced conduction loss. This is very important feature when the transformer can not be designed with low leakage inductance.

C. Duty Cycle Boost Effect

The secondary rectifier duty cycle is usually lower than that of the primary because of the duty cycle loss.
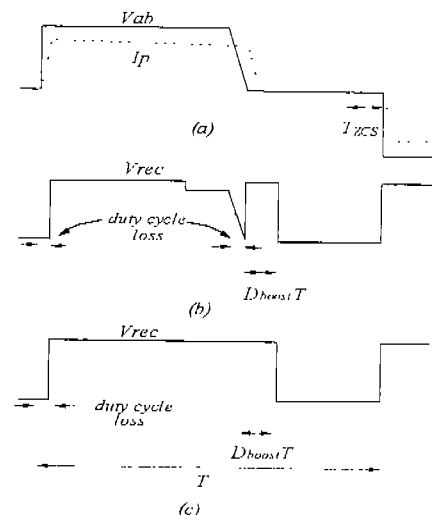

Fig. 6 Comparison of primary and secondary rectifier voltage waveforms between previous converter and proposed converter : (a) primary voltage, (b)secondary rectifier voltage of previous presented converter[5], (c) the proposed converter.

In the proposed converter, however, the rectifier duty cycle can be higher than that of the primary as shown in Fig. 6. This phenomenon is caused by the operation of the active clamp from the beginning of freewheeling period to provide ZCS condition to the lagging-leg switches. This means that the stored energy in the leakage inductance is recovered to the clamp capacitor and finally transferred to the load. The primary duty cycle can not be increased to near unity since the minimum dead-time is required to achieve a complete ZCS turn-off of the lagging-leg switches. The effective duty cycle of the proposed converter, however, can be increased to near unity due to the duty cycle boost effect. The effective duty cycle of the proposed converter can be expressed as follows:

$$D_{eff} = D_{prim} - \Delta D + D_{boost}, \qquad (5)$$

where, ΔD is the duty cycle loss. The D_{boost} is determined directly by the turn-on time of the clamp

switch. The duty cycle boost effect also helps to improve the overall efficiency.

D. Conduction loss by auxiliary inductor current

The current through auxiliary inductor is approached to maximum value when duty cycle is near to unity. So, the conduction loss by the auxiliary inductor current is also maximum value at this time. It can be estimated approximately as follow;

$$P_{loss} = \frac{I_{peak} \cdot S_{drop}}{2}, \qquad (6)$$

where, P_{loss} is the loss by auxiliary inductor, I_{peak} is the peak value of inductor current and S_{drop} is conduction voltage of primary switch. Since the voltage drop of IGBT is lower than a few volts and I_{peak} is also a few A, it can be seen that the conduction loss by the auxiliary inductor current is minor.

IV. Design Considerations

A. Decision of Dead Times

An appropriate dead time is required for leading and lagging-leg switches to achieve maximum performance.

Dead time for leading-leg switches: The dead time for leading-leg switches is determined by ZVS condition at minimum load. The dead time should be minimized since large dead time reduces the maximum controllable duty cycle, which reduces the overall efficiency in turn.

Dead time for lagging-leg switches: The minimum dead time of lagging-leg switches is determined by the time T_{ZCS} to achieve a complete ZCS of the lagging-leg switches as follows:

$$T_{d,lag} \geq T_{ZCS}, \qquad (7)$$

where, the T_{ZCS} is the minority carrier recombination time of IGBTs. The maximum dead time is also limited by the maximum duty cycle of the primary side.

B. Decision of auxiliary inductor value

The minimum current value of auxiliary inductor is determined by primary current, dead time, external capacitor and input voltage to obtain ZVS for leading-leg switches at the light load as follow;

$$I_{Lr} = \frac{(C_1 + C_3) \cdot V_s}{t_{dead}} - I_{p,avg}, \qquad (8)$$

where, C1 and C3 are additional snubber capacitors in the leading-leg, and $I_{p,avg}$ is the average value of reflected load current to primary during dead time. Therefore, auxiliary inductor value can be designed as follow;

$$L_r = \frac{V_s \cdot T_{on,min}}{8 \cdot I_{Lr}}, \qquad (9)$$

where, $T_{on,min}$ is the minimum turn-on time of leading leg switches. To guarantee complete ZVS for leading leg switches, the auxiliary inductor must be selected lower value than calculated one.

V. Experimental Results

A 3 kW, 100 kHz prototype of the proposed ZVZCS-FB-PWM converter has been built and tested to verify the principle of operation. Fig. 7 shows the experimental circuit diagram with the part numbers of components used. Fig. 8 shows the waveforms of the primary voltage and current and the secondary rectifier voltage at full load (nominal duty cycle of 0.74) and Fig. 9 shows the extended waveforms at the switching transitions of leading and lagging-legs. All waveforms are well matched with the expected ones. The primary current is quickly reset after the primary voltage is dropped to zero and sustained during the freewheeling period. The primary current falling slope is almost same as that of the rising which allows very short reset time. The duty cycle loss is about 0.3us, which can be clearly read from Fig. 9(b). Fig. 10 shows the auxiliary inductor current. The peak to peak inductor current is only 5A in this circuit. Fig 11 shows the extended waveforms of leading leg switches. A complete ZVS turn-on is achieved with the help of the auxiliary inductor current. During turn-off, the switching loss is remarkably reduced comparing to hard switching since the rising slope of the switch voltage is considerably reduced by adding external snubber capacitors. The ZVS for the leading-leg switches is achieved even at no load. Fig 12 shows the waveforms of leading leg switches at the 5% load with and without including the auxiliary inductor. A complete ZVS is obtained with the inductor at light load but ZVS is lost without the inductor, which results in considerable ring and loss. Fig. 13 shows the extended switching waveforms of lagging-leg switches. It can be seen that a complete ZCS turn-off is achieved since the primary current is zero during the freewheeling period. Small pulse current during turn-on transition is the charging current of the switch output capacitor. Fig. 14 shows the waveforms of the secondary active clamp. All waveforms are the same as the expected. The maximum measured efficiency is about 94 %.
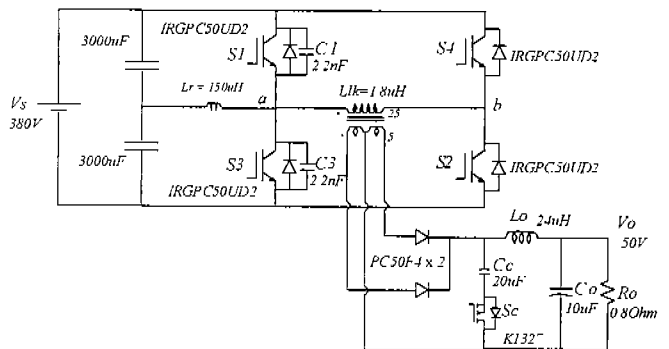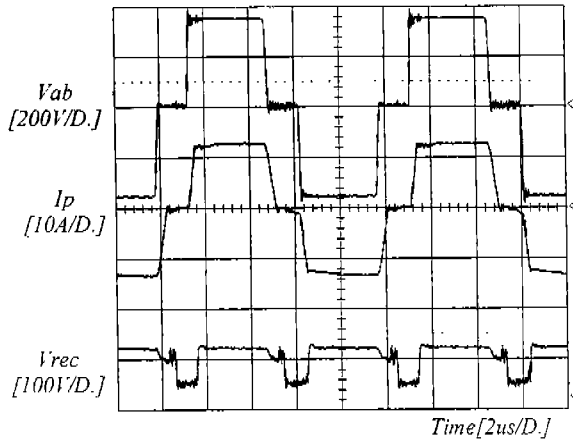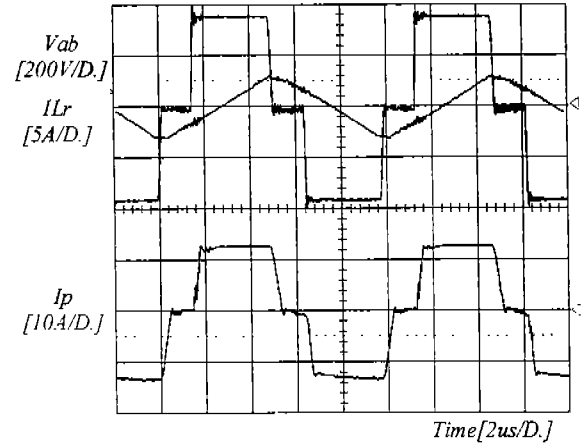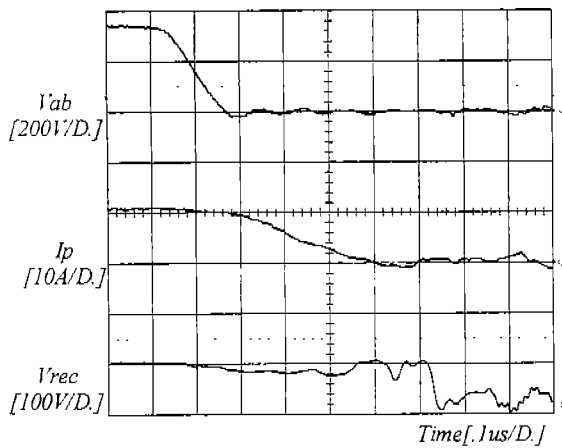

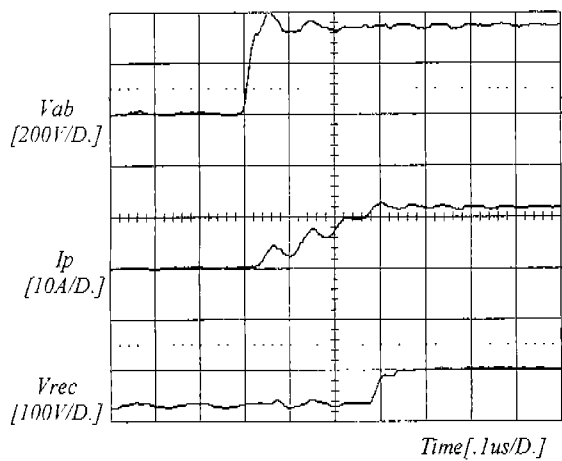**Fig. 7** Experimental circuit diagram of the proposed converter.

Fig. 8 Experimental waveforms of primary voltage and current and secondary rectifier voltage.

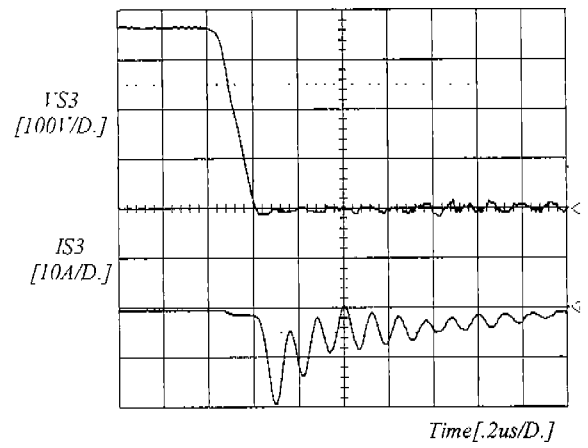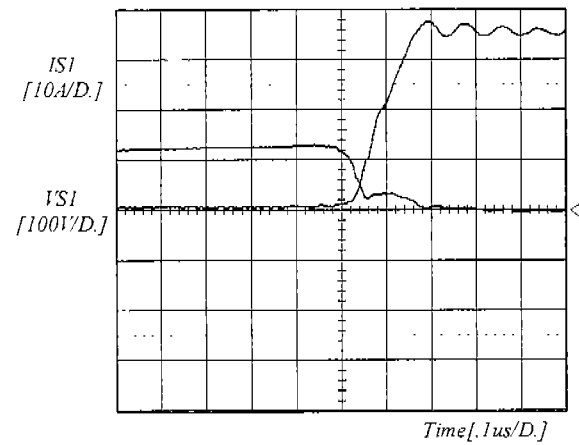**Fig. 10** Experimental waveforms of primary voltage and current and auxiliary inductor current.

(a)

(b)

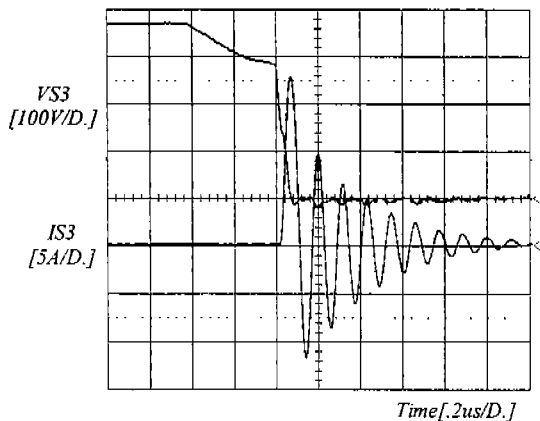**Fig. 9** Extended waveforms at switching transitions: (a) leading-leg, (b) lagging-leg.
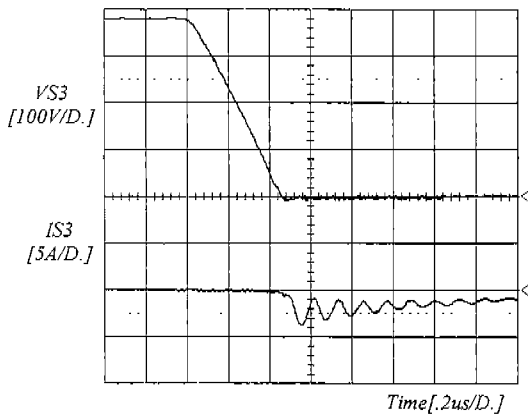

(a)

(b)

Fig. 11 Extended ZVS switching waveforms of leading leg switches: (a) turn-on, (b) turn-off.

(a)

(b)

Fig. 12 Extended ZVS switching waveforms of leading
leg switches at the light load (5%):
(a) without Lr (b) with Lr

Fig. 13 Extended ZCS waveforms of lagging-leg
switches.
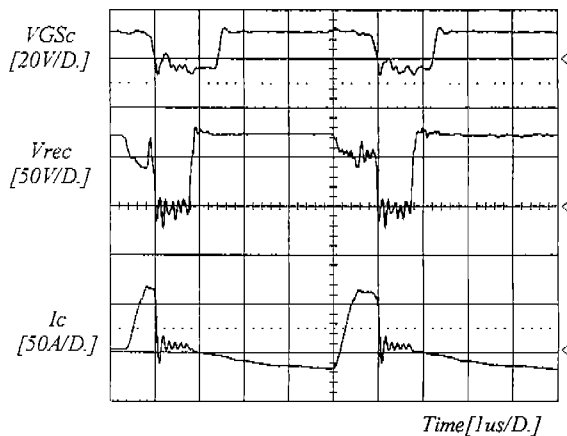
Fig. 14 Waveforms of secondary active clamp.

VI. Conclusion

An improved ZVZCS-FB-PWM converter using secondary active clamp is presented. The operation, analysis, features and design considerations are illustrated and verified by the experimental results on a 3 kW, 100 kHz IGBT based prototype. It is shown that ZVS for leading leg switches is achieved at the full load range by adding an auxiliary inductor and ZCS for lagging leg switches are achieved by the help of the active clamp. The proposed converter has distinctive advantages over the previously presented ZVZCS converters as follows: ZVS and ZCS without any lossy components, soft switching of secondary active switch, wide ZVS and ZCS range, low duty cycle loss, more reduced conduction loss in the primary, no parasitic ringing in the secondary rectifier. Many advantages of the new circuit makes the proposed converter very promising for high voltage, high power (> 1 kW) applications.

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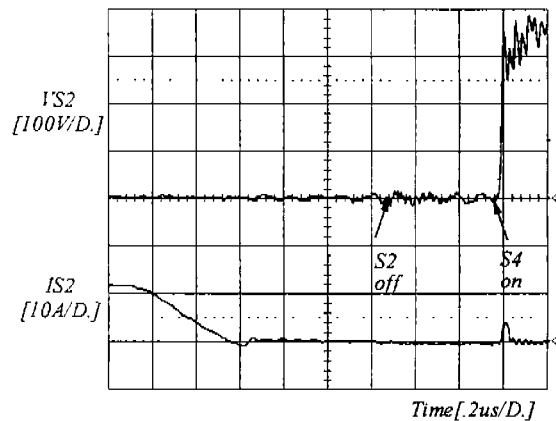[2] IGBT "Designers Manual", International Rectifier, El Segundo, CA, 1994.

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