SINGLE -PHASE ACTIVE RECTIFIER WITH HIGH POWER FACTOR CAPABILITY FOR INVERTER AIR-CONDITIONER

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ABSTRACT - A Single-phase Active Rectifier (SAR) [4-6] with high power factor capability is adopted to satisfy the international harmonic current standards such as IEC 1000-3-2. To minimize the input current distortion and to apply the control IC, such as FA5331, UC3854, ML4821 and so forth, the new adequate sensing circuits of the input voltage and current are proposed. There are two methods applicable the SAR to inverter air-conditioner from the viewpoint of both efficiency and cost. The selecting methods of the passive components are presented for the two approaches. Using the determined components, the loss analyses are carried out. The prototype SAR circuits of these two approaches with 3kW power consumption are built and the operation and performance of the circuits with power factor correction capability are verified through the experimental results.

1. INTRODUCTION

Recently, the international activities for energy saving has been intensively executed. To keep in step with this trend, the adoption of the inverter technology has been extensively expanded in the home appliance, such as air-conditioner, refrigerator, washing machine and so on.

However, because they operate by rectifying the input ac line voltage and filtering it with large electrolytic capacitor, the input current has poor power factor and rich harmonics. Although the power factor of the conventional inverter air conditioner can be improved about 0.9 using the LC passive filter, input current harmonics don't meet the forthcoming international standards, IEC 1000-3-2. To obtain the harmonic regulation capability and to improve the inverter performance through the stabilization of the DC link voltage, it is a trend to add the power factor correction circuit to the conventional inverter air-conditioner.

Several topologies are available for power factor correction and harmonic current reduction. Among them, the most popular topology is the boost circuit[1-3]. Although the boost topology has the enhanced performance, the total efficiency becomes lower due to adding the extra circuit.

Thus, in this paper, a Single-phase Active Rectifier (SAR) [4-6] with high power factor capability for the inverter air-conditioner is adopted to satisfy the international standards of input current harmonics, IEC 1000-3-2. Comparing the conventional boost power factor correction circuit, one diode drop is reduced in the power flow path of the SAR topology, so the system efficiency is improved. In this case, there are two approaches in order to apply the SAR to the inverter air-conditioner fed from single-phase ac source. One is the high efficiency approach and the other is the low cost approach, respectively. In the former case, the switching frequencies of the above-mentioned two topologies (SAR and Boost) are equalized. On the other hand, in the low cost approach, the switching frequency of the SAR is increased to reduce the additional cost in the latter and thereby the each size of choke inductor and filter components can be reduced.

To minimize the input current distortion, we propose the new detecting circuits of the input voltage and current. The selecting methods of the passive components are presented. Using the designed components, the loss analyses are performed. The proto-type SAR circuits of these two approaches with 3kW power consumption are built and tested to verify the operation and performance of the circuits with power factor correction capability.

2. OPERATIONAL PRINCIPLE

Fig. 1 shows the single-phase active rectifier and the

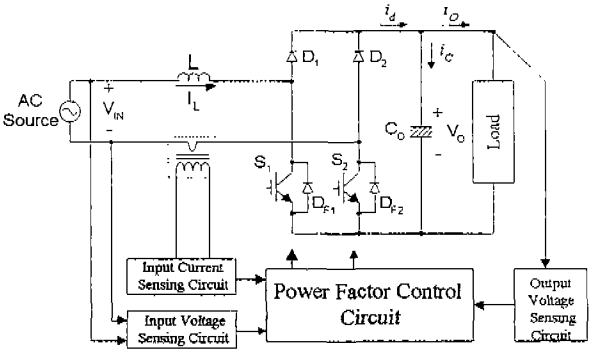


Fig. 1 The single-phase active rectifier with the control block diagram

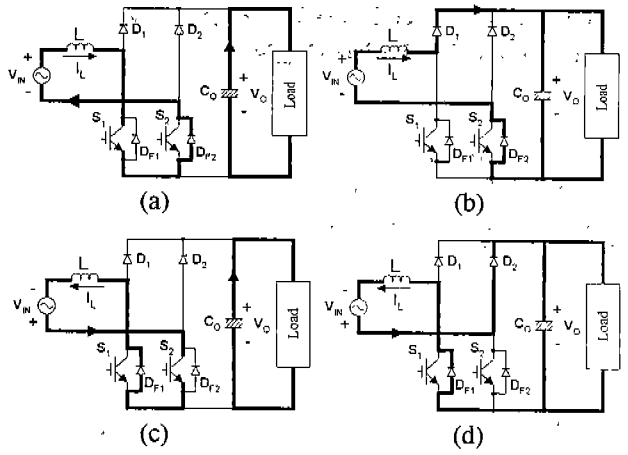


Fig. 2 The operational modes of the SAR

control block diagram. As can be seen the reference [4-6], according to the input voltage polarity, the power factor correction is attained by S_1, D_1, and D_{F2} for the positive value and S_2, D_2, and D_{F1} for the negative value, respectively.

First of all, consider the case that the input voltage is positive. If S_1 is turned on as shown in Fig. 2 (a), the input voltage V_{IN} appears across the choke inductor L through V_{IN}-L-S_1-D_{F2} path and the inductor current I_L increases linearly with the positive slope of V_{IN}/L. At the same time, the output capacitor is discharged to the load. If S_1 is turned off by the control signal as shown in Fig. 2 (b), the difference voltage (VO-V_{IN}) is applied in the opposite direction across the choke inductor L through V_{IN}-L-D_1-C_O-D_{F2} path and the inductor current I_L decreases linearly with negative slope of (VO-V_{IN})/L. In this case, the output capacitor is charged through the choke inductor.

When the input voltage is negative, the similar operations are achieved by S_2, D_2, and D_{F1} as shown in Fig. 2 (c) and (d).

3. THE PROPOSED SENSING CIRCUIT

The proper sensing circuits, such as input current, input voltage and output voltage, are indispensable for

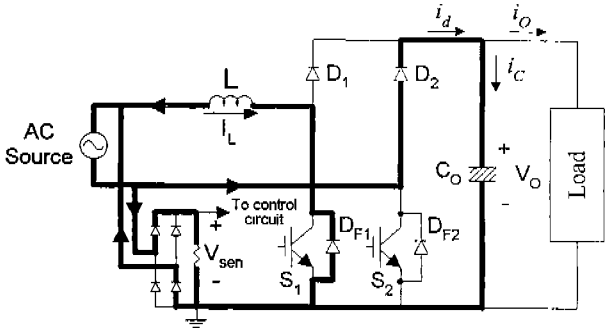


Fig. 3 The sensing path of the input voltage sensing circuit referred to [6]

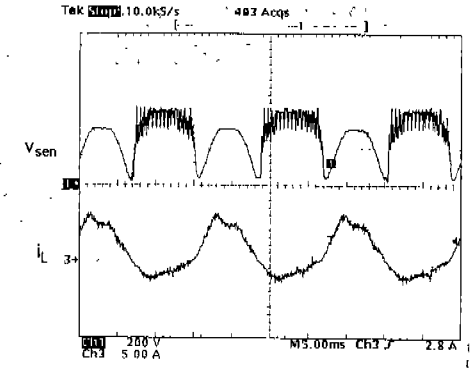
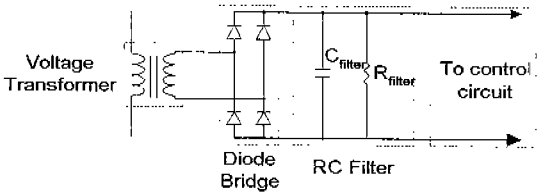


Fig. 4 The experimental waveforms in the case of Fig. 3

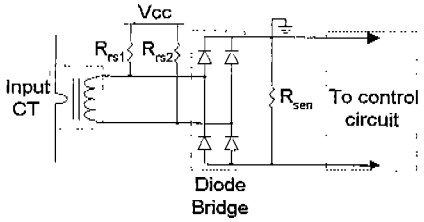
raising the power factor correction performance. As can be seen in Fig. 3, the input voltage sensing circuit referred to [6] has a severe problem. When the input voltage is negative, the sensing voltage V_{sen} has a ripple from zero to V_O and vice versa due to switching of S_2. The V_{sen} waveform in Fig. 4 is obtained by inserting the high frequency RC filter into the output of the sensing circuit.

Thus, to resolve the problem, we interpose the voltage transformer between the ac input line and the diode bridge as depicted in Fig. 5 (a). In this circuit, the high frequency RC filter is used to prevent the distortion of the sensing voltage.

Fig. 5 (b) shows the input current sensing circuit composed of current transformer (CT), offset resistors (R_{rs1}, R_{rs2}), diode bridge and sensing resistor (R_{sen}). To transmit favorably the high frequency sensing information, the turn ratio of the CT should be sufficiently enlarged. The offset resistors are twofold roles. One is to remove the noise components of the sensing voltage and the other is to force the SAR circuit to operate with maximum duty when the input voltage is in the vicinity of zero cross. The currents flowing through the offset resistors are constant as (V_{cc}-V_d)/R_{rs1} and (V_{cc}-V_d)/R_{rs2} where V_d is the on-



(a) Input voltage sensing circuit



(b) Input current sensing circuit

Fig. 5 The proposed sensing circuits

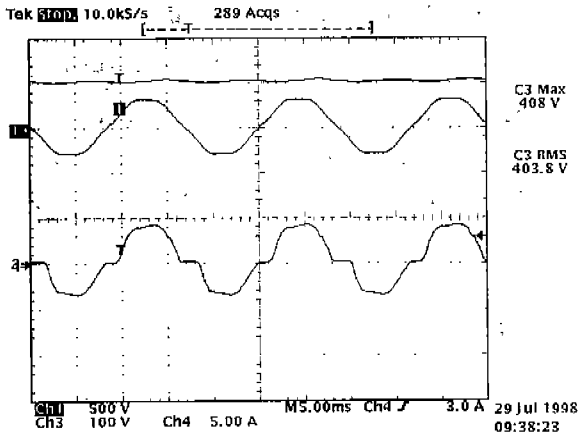


Fig. 6 The experimental waveforms without the offset resistors (Upper : Output voltage, Middle : Input voltage Lower : Input current)

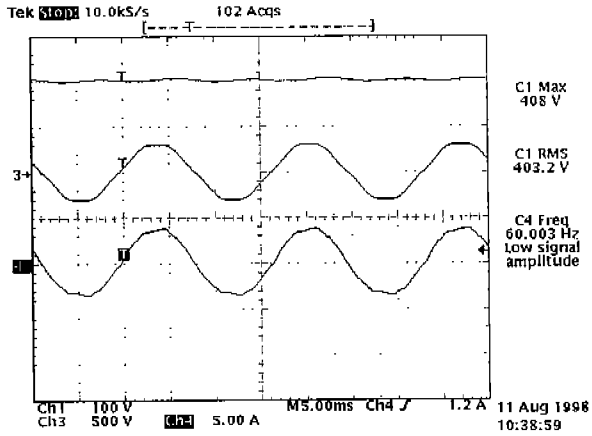


Fig. 7 The experimental waveforms with the offset resistors (Upper : Output voltage, Middle : Input voltage Lower : Input current)

voltage of diode. These currents are somewhat arbitrarily selected to about 1mA. To ascertain the effect of the offset resistors, Fig. 6 and 7 show the experimental results without and with these resistors, respectively. As can be seen in Fig. 7, the crossover distortion of the input current has been dramatically reduced.

4. THE SELECTION METHOD OF THE PASSIVE COMPONENTS

1) ***Choke Inductor*** [2-3] : To select the choke inductor, the peak inductor current (I_{pk}) should be calculated. This current can be expressed by :

$$I_{pk} = 2P_{IN} / V_{IN,\min} + \Delta I / 2 \tag{1}$$

where P_{IN} is the input power, $V_{IN,min}$ is the minimum input voltage and ΔI is the ripple current of the choke inductor. In this equation, the first term means the maximum rms input current. At the condition of (1), that is, the peak value of the minimum input voltage, the duty D can be calculated as follows :

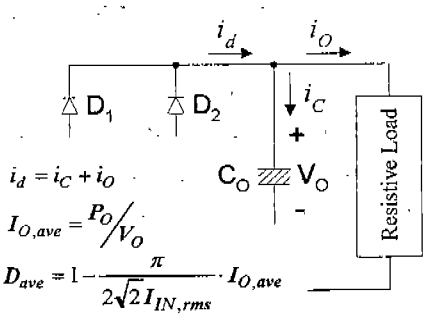


Fig. 8 Some notations and the related equations to calculate the capacitor ripple current

$$D = \frac{V_O - V_{IN,\min}(peak)}{V_O} \tag{2}$$

In this case, the inductance of the choke inductor can be determined by the following equation.

$$L = \frac{V_{IN,\min} \times D}{\Delta I \times f_s} \tag{3}$$

where f_s is the switching frequency.

2) ***Output Capacitor*** : To obtain the appropriate output capacitor, it is necessary to know both the permissible ripple current capability and the capacitance of the output electrolytic capacitor in advance. Although there is a somewhat difference for a motor load, to regard this result as a guide, we assume the load is resistive. In this case, the rms value of the load current i_O as shown in Fig. 8 is expressed by

$$I_{O,rms} = \frac{P_{IN} \cdot \eta_{PFC}}{V_O} \tag{4}$$

where η_{PFC} is the efficiency of the SAR circuit. The diode current is calculated as follows :

$$I_{d,rms} = \frac{P_{IN}}{V_{IN,\min}} \cdot \sqrt{1 - D_{ave}} \tag{5}$$

where D_{ave} is the average duty ratio of the switch for a period of 120Hz. Thus, using the above two equations, the permissible ripple current of the capacitor can be obtained by the following equation.

$$I_{c,rms} = \sqrt{I_{d,rms}^2 - I_{O,rms}^2} \tag{6}$$

Using the current, the required capacitance should be satisfied with the following condition.

$$C = \frac{I_{c,rms}}{\omega \cdot \Delta V} \tag{7}$$

where ω is the angular frequency of the rectified voltage and ΔV is the permissible output ripple voltage as can be expressed as follows :

$$\Delta V = \frac{\%ripple \times V_O}{2\sqrt{2}} \tag{8}$$

where *%ripple* is the ripple percentage defined by the user.

5. LOSS ANALYSIS

To verify the high efficiency property of the SAR, we perform the loss analysis in this section. IGBT and diode

Table 1 The calculated losses for two topologies

	Boost	SAR
Choke Inductor ESR Loss	12.62[W]	12.62[W]
Switch Conduction Loss	23.7[W]	23.7[W]
Switch Switching Loss	15.35[W]	15.35[W]
Total Switch Loss	39.05[W]	31.53[W]
Diode Loss	8.66[W]	8.66[W]
Bridge Diode Loss	36.7[W]	-
Total Loss	97.03[W]	84.34[W]
Efficiency	96.8[%]	97.2[%]

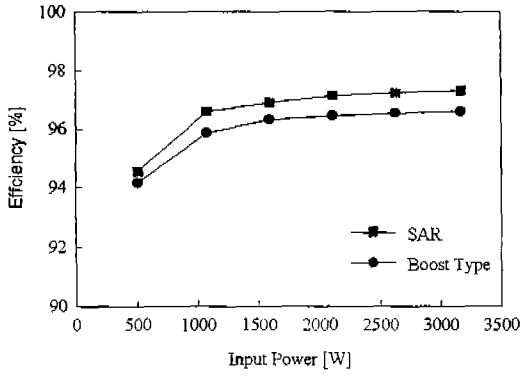


Fig. 9 The efficiencies according to the input powers by the test results

losses can be calculated by a manufacturer specified model that includes an offset voltage in series with a resistance. Each loss equation can be expressed as follows.

$$P_{BD} = I_{in,rms} \cdot V_F \cdot 2 = \frac{P_{IN}}{V_{IN}} \cdot V_F \cdot 2 \text{ -- Bridge diode loss} \quad (9)$$

$$P_{off} = \sum_{n=1}^{T_{IN}/T_{sw}} \frac{i_{C,n}^2 \cdot t_{off}^2}{48 \cdot C_O} \text{ --- Turn-off switching loss} \quad (10)$$

$$P_{con,sw} = \frac{1}{T_{IN}} \int_0^{T_{IN}} (V_{O,sw} + R_{s,sw} \cdot i_C) \cdot i_C dt \quad (11)$$

--- Switch conduction loss

$$P_{con,d} = \frac{1}{T_{IN}} \int_0^{T_{IN}} (V_{O,d} + R_{s,d} \cdot i_d) \cdot i_d dt \quad (12)$$

--- Diode conduction loss

$$P_L = \frac{1}{T_{IN}} \int_0^{T_{IN}} i_L^2 \cdot R_L dt \text{ --- Choke inductor ESR loss} \quad (13)$$

where V_F is the diode forward voltage, T_{IN} and T_{sw} are periods of the rectified voltage and the switching frequency, i_C, t_{off} and C_O are the collector current, the turn-off time and the output capacitance of the switch, $V_{O,sw}$ in series with $R_{s,sw}$ are the manufacturer specified model of the switch, $V_{O,d}$ in series with $R_{s,d}$ are the manufacturer specified model of the diode and i_L and R_L are the inductor current and the effective series resistance of the choke inductor, respectively. Table 1 shows the calculated losses through the computer simulation using

Table 2 The experimental conditions

	High Efficiency SAR	Low Cost SAR
Switching Frequency	25[kHz]	40[kHz]
Choke Inductance	530[μH] / 30[A]	354[μH] / 30[A]
Output Capacitance	680[μF] / 450[V]	680[μF] / 450[V]
Output Voltage	400[V]	400[V]

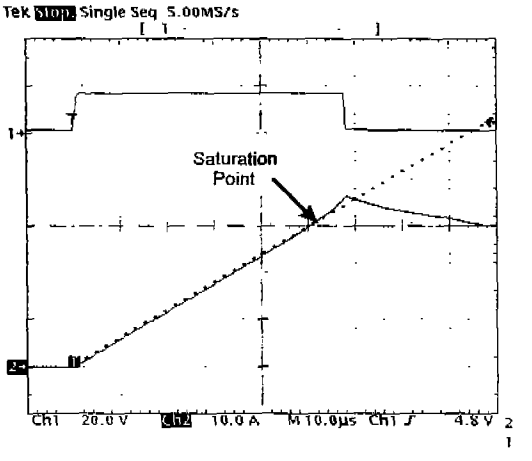


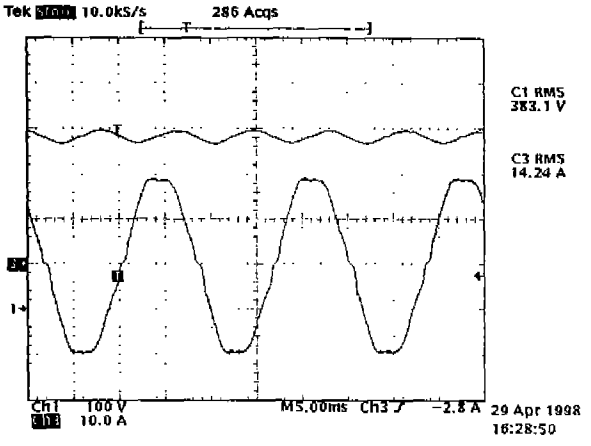
Fig. 10 The saturation test for the choke inductor

the above equations assuming that the turn-off loss and the turn-on loss of the switch are the same. Moreover, Fig. 9 shows the experimental results for the comparison between the SAR and the boost topologies. As can be seen in these table and figure, the efficiency of the SAR is about 0.5% greater than one of the boost. Therefore, to attain the low cost approach, the switching frequency can be increased to 40kHz with the similar efficiency. In this case, since the each size of the choke inductor and the filter components can be reduced, the additional cost can be minimized.

6. EXPERIMENTAL RESULTS

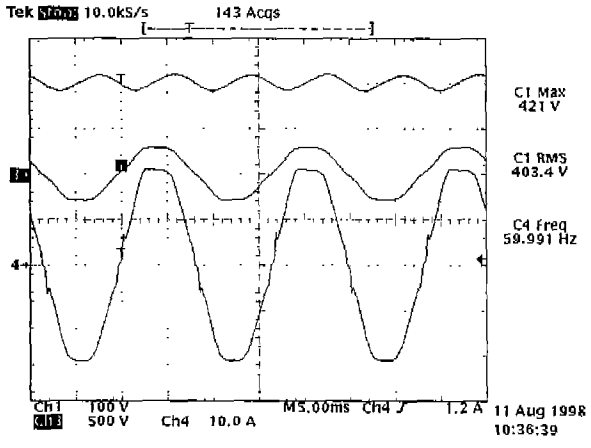
To verify the above mentioned operation and to assure the performance of the power factor correction, the prototype SAR circuits with operation at the 25kHz and 40kHz switching frequency are manufactured and tested with the experimental conditions as shown in Table 2.

Fig. 10 show the saturation test result of the choke inductor. The safe operation up to 30[A] has been ensured as shown in this figure. Fig. 11 shows the experimental waveforms at the rated power for the two SAR circuits. Fig. 12 and Fig. 13 show the performance of the power factor correction such as power factor and THD. As can be seen in these two figures, they have been thoroughly satisfied with the international standards, IEC 1000-3-2.



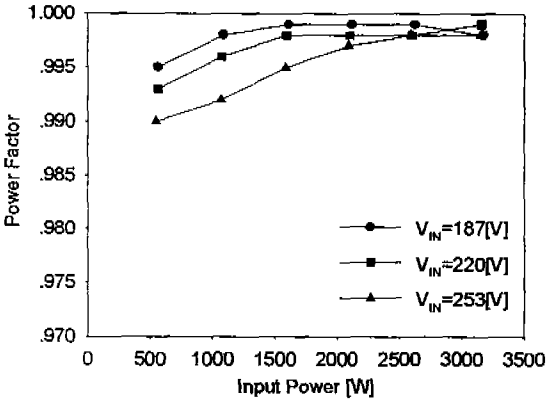
(a) 25kHz SAR

(Upper : Output voltage, Lower : Input Current)

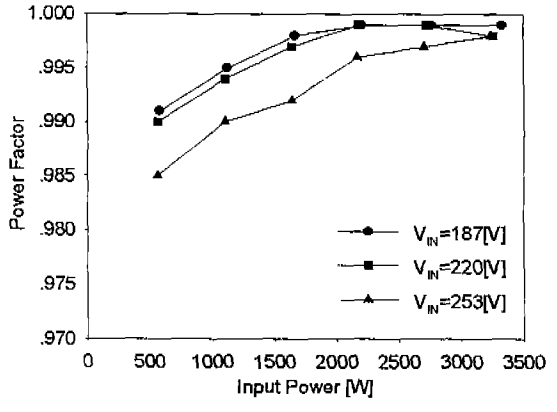


(b) 40kHz SAR (Upper : Output voltage, Middle : Input Voltage, Lower : Input Current)

Fig. 11 The experimental results at the rated power for the two SAR circuits



(a) 25kHz SAR



(b) 40kHz SAR

Fig. 12 The power factor according to the input power for the two SAR circuits

7. CONCLUSION

In this paper, to meet the international standards of the input current harmonics for the inverter air-conditioner system, we adopt the single-phase active rectifier [4-6] with high power factor capability. The new proper sensing circuits of the input voltage and current are proposed to reduce the input current distortion and to apply the available control IC, such as FA5331, UC3854, ML4821 and so on. Also, we present the design methods of the passive components. Using the designed components, the loss analyses are performed. As a result, it has been established that the SAR topology has a good efficiency more than the conventional boost circuit. To ascertain the operation and performance of the two circuits, the proto-type SAR circuits with operation at the 25kHz and 40kHz switching frequency have been built and tested. Through the experimental results, we have verified the capability of both the high efficiency approach and the low cost approach of the SAR topology.

8. REFERENCES

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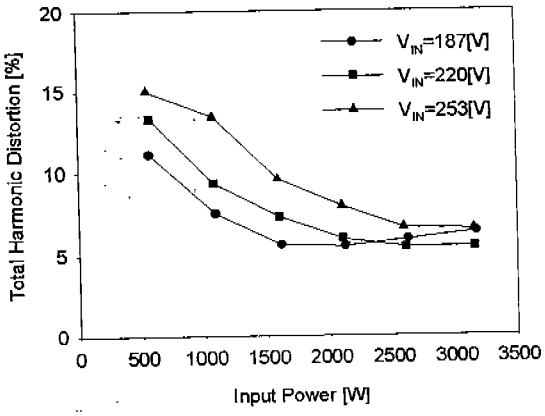
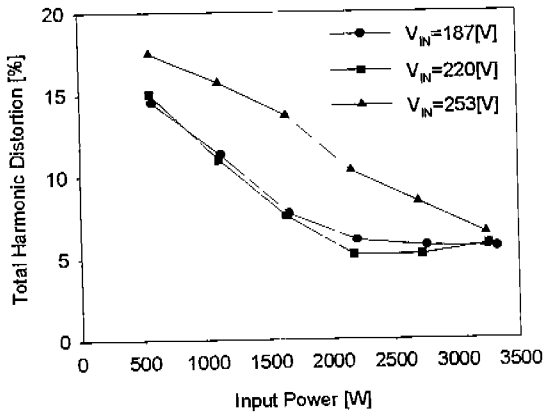


(a) 25kHz SAR



(b) 40kHz SAR

Fig. 13 The total harmonic distortion for each approach