SMALL-SIGNAL MODEL FOR A CONTROLLED ON-TIME BOOST POWER FACTOR CORRECTION CIRCUIT

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ABSTRACT - A new small-signal model for the controlled on-time boost power factor correction (PFC) circuit is presented. The proposed small-signal model is valid up to high frequencies over 1kHz. The model can be used in designing the voltage feedback compensation of PFC circuits, the control bandwidth of which is maximized with auxiliary means of removing the low-frequency ripple from the output. The accuracy of the model is confirmed by a 200W experimental hardware.

1. INTRODUCTION

One of the popular PFC circuits suitable for low-power applications is the boost converter operating at the boundary of the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM), commonly known as the controlled on-time boost PFC circuit [1]. While dc characteristics of the controlled on-time boost PFC circuit are well documented [1-3], research results on the small-signal dynamics of the PFC circuit are limited. The small-signal model that predicts low-frequency dynamics of generic PFC circuits was proposed in [4], and adapted to the control design for the controlled on-time boost PFC circuit having a narrow loop gain crossover frequency, far less than the line frequency [1]. On the other hand, the high-frequency small-signal model for the controlled on-time boost PFC circuit, that predicts high-frequency dynamics and thereby enables the loop gain crossover frequency to be maximized, has not been presented yet.

This paper presents a new small-signal model for the controlled on-time boost PFC circuit, valid up to high frequencies over 1kHz. In deriving the new model, the rectified line voltage is replaced with its rms value, as was initially practiced in [5] and has been justified by other researchers [6,7]. With this substitution, the PFC circuit can be considered as a regular boost dc-to-dc converter with an input voltage identical to the rms value of the rectified line voltage.

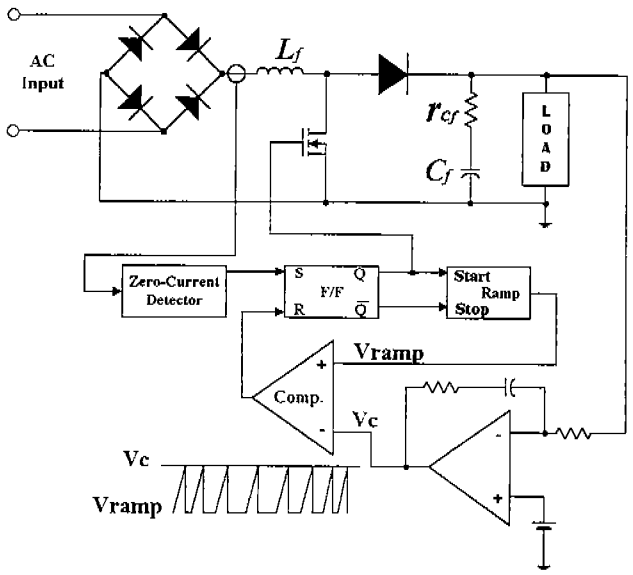

Fig. 1. Controlled on-time boost PFC circuit.

The small-signal model for the power stage of the PFC circuit is derived from the small-signal model of the boost power stage by incorporating the duty-ratio constraint unique to the controlled on-time boost PFC circuit. The small-signal model for the duty-ratio modulator is developed using the method similar to that used for the conventional voltage mode control. The complete small-signal model for the PFC circuit is obtained by combining the small-signal models for the power stage and the modulator.

In order to assess the accuracy of the new model, a 200W prototype circuit is built, and its control design is optimized using the new model. The accuracy of the model is verified by comparing measured small-signal dynamics of the prototype with predictions of the new model.

2. NEW SMALL-SIGNAL MODEL FOR CONTROLLED ON-TIME BOOST PFC CONVERTER

I. Operation of PFC circuit

Figure 1 shows the schematic diagram of the controlled on-time boost PFC circuit.

Initially the MOSFET is assumed to be on state. The output of the ramp generation circuit, v_{ramp}, is fed to the (+) terminal of the comparator, and the output of the voltage feedback compensation, v_c, is connected to (-) terminal of the comparator. For the time period when $v_c > v_{ramp}$, the output of the comparator is low and the flip-flop retains set state.

When the magnitude of v_{ramp} reaches to that of v_c, the output of comparator becomes "high" and resets the flip-flop. This turns the MOSFET off, and resets v_{ramp} to zero.

When the inductor current, which increases during on state, decays to zero, the zero-crossing detector sets the flip-flop and the PFC circuit resumes the on-time operation.

II. Development of small-signal model

The small-signal modeling is divided into two parts: the first is development of the small-signal model for the power stage of the PFC circuit, and the other is development of the small-signal model for the modulator.

1) Power stage modeling

The input voltage is replaced by the rms value of the rectified line voltage, and thereby the PFC circuit can be considered as a regular boost dc-to-dc converter operating at the boundary of CCM and DCM. With the substitution, the small-signal model of the power stage of the PFC circuit is derived from that of the DCM dc-to-dc converter, using the duty-ratio constraint unique to the PFC circuit.

Since the power stage of the PFC circuit is considered as that of a boost dc-to-dc converter, the active and passive switches of the converter can be lumped together in a single functional block, known as the PWM switch, as shown in Fig. 2.

The terminal currents and voltages of the PWM switch are defined in Fig.3, where $\tilde{i}_a(t)$, $\tilde{i}_p(t)$ and $\tilde{v}_{ac}(t)$, $\tilde{v}_{cp}(t)$ represent the instantaneous terminal currents and voltages respectively.

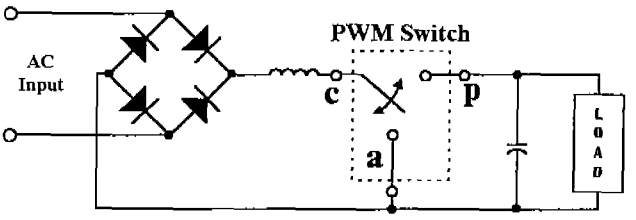

Fig. 2. Power stage of the PFC circuit with PWM switch.

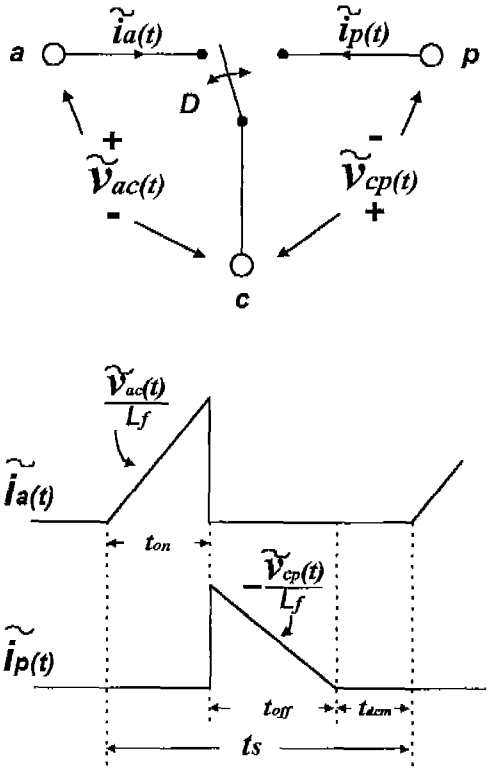

Fig. 3. Voltages and currents of PWM switch in DCM.

From Fig. 3, the following expressions for the average terminal currents and voltages can be deduced [8] as:

$$i_a = \frac{d}{d_2} i_p \tag{1}$$

$$v_{ac} = \frac{d_2}{d} v_{cp} \tag{2}$$

$$d_2 = \frac{2L_f}{d\,t_s} \frac{i_p}{v_{ac}} \tag{3}$$

where,

$$d = \frac{t_{on}}{t_s}$$

$$d_2 = \frac{t_{off}}{t_s}.$$

When d_2 is replaced with $1 - d$ in (1) considering the operational principles of the converter, the equation becomes:

$$(1 - d)\, i_a = d\, i_p . \tag{4}$$

By perturbing (4), we can obtain:

$$\hat{i}_p = \frac{I_p}{I_a}\hat{i}_a - \frac{I_a}{D^2}\hat{d} . \tag{5}$$

By applying the same procedure to (3), it follows

$$(1 - d)\, v_{ac} = k\, i_p \tag{6}$$

where,

$$k = \frac{2L_f}{d\, t_s} = \frac{2L_f}{t_{on}} .$$

By perturbing (6), it can be shown:

$$\hat{i}_p = \frac{I_p}{V_{ac}}\hat{v}_{ac} - \frac{I_p}{1-D}\hat{d} . \tag{7}$$

From (5) and (7), we can obtain:

$$\frac{I_p}{I_a}\hat{i}_a - \frac{I_a}{D^2}\hat{d} = \frac{I_p}{V_{ac}}\hat{v}_{ac} - \frac{I_p}{1-D}\hat{d}$$

which can be rearranged as:

$$\hat{v}_{ac} = \frac{V_{ac}}{I_a}\hat{i}_a + \frac{V_{ac}}{I_p}\left(\frac{I_p}{1-D} - \frac{I_a}{D^2}\right)\hat{d} . \tag{8}$$

Finally, from (2) and (3), it can be shown:

$$d\, v_{ac} = d_2\, v_{cp}$$

$$d\, v_{ac} = k\, \frac{i_p}{v_{ac}}\, v_{cp} . \tag{9}$$

By perturbing (9), the final form of the equation becomes:

$$\hat{v}_{cp} = \frac{2V_{cp}}{V_{ac}}\hat{v}_{ac} + \frac{V_{cp}}{D}\hat{d} - \frac{V_{cp}}{I_p}\hat{i}_p . \tag{10}$$

The small-signal model of the power stage, based on (8) and (10), is shown in Fig. 4.

The circuit components in Fig. 4 are defined as:

$$E_{bi} = \frac{V_{ac}}{I_p}\left(\frac{I_p}{1-D} - \frac{I_a}{D^2}\right)$$

$$r_{bi} = \frac{V_{ac}}{I_a}$$

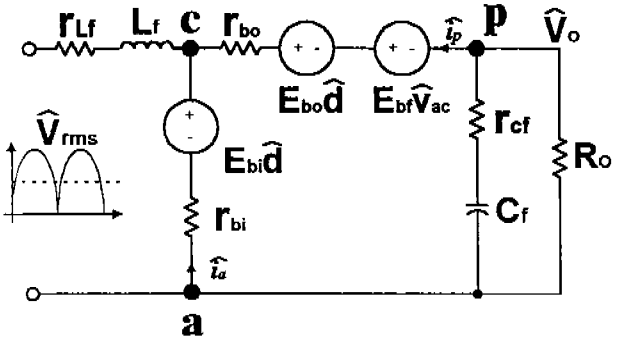

Fig.4. The small-signal model of the power stage

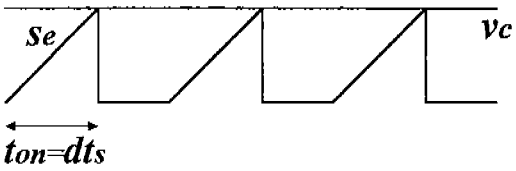

Fig. 5. Controlled on-time control scheme.

$$r_{bo} = -\frac{V_{cp}}{I_p}$$

$$E_{bo} = \frac{V_{cp}}{D}$$

$$E_{bf} = \frac{2V_{cp}}{V_{ac}}$$

where the variables with capital letters represent the dc components of the corresponding currents and voltages.

2) Modulator modeling

Since the input to the PFC circuit is replaced by the rms value of the rectified line voltage, the small-signal model of the modulator is derived using the same method as that used for the conventional voltage mode control.

Figure 5 shows the control scheme of a dc-to-dc converter operating at the boundary of CCM and DCM.

From Fig. 5, it can be shown:

$$d\, t_s\, s_e = v_c \tag{11}$$

where s_e is the slope of the external ramp.

By perturbing (11), we can obtain:

$$s_e\, t_s\, (D + \hat{d}) = (V_c + \hat{v}_c) . \tag{12}$$

By equating the small-signal components of (12), the modulator gain, F_m, can be derived as:

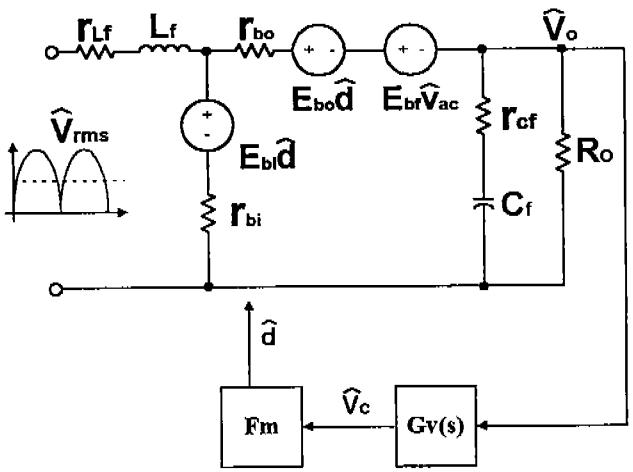

Fig. 6. The new small-signal model.

$$F_m = \frac{\hat{d}}{\hat{v}_c} = \frac{1}{s_e\, t_s}.$$

Figure 6 shows the complete small-signal model, where $G_v(s)$ represents the voltage feedback compensation.

III. Model verification

Figure 7 compares the measured control-to-output voltage transfer functions with the prediction of the new model. The parameters for a 200W prototype are listed in Table 1.

The new model approximates the control-to-output voltage transfer function of the PFC circuit with AC input below 1kHz. On the other hand, the new model approximates the control-to-output voltage transfer function of the PFC circuit with DC input up to half the switching frequency.

It is very interesting to observe a dip at the high frequencies in the case with AC input. The location of the dip is influenced by the inductance, esr of the capacitor, and dominantly by capacitance.

Table 1. Parameters

INPUT	110 [V]rms ~ 220 [V]rms
OUTPUT	380 [V]
Lf	322.7 μH
r_{Lf}	100 mΩ
Cf	235 μF
r_{Cf}	200 mΩ

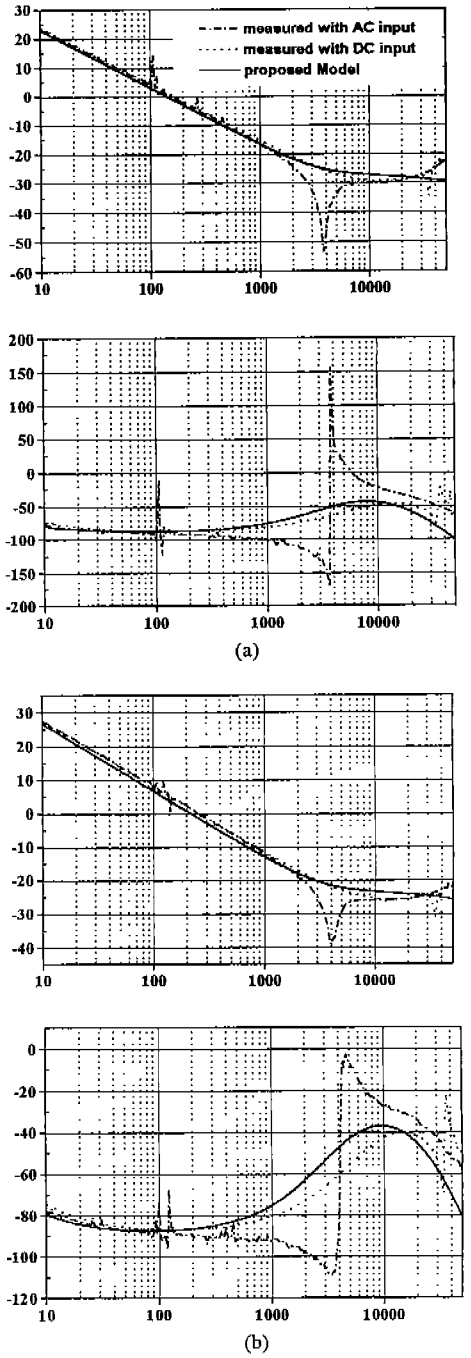

Fig. 7. Control-to-output voltage transfer function.
(a) Vin,rms = 130 [V] , Vo = 380 [V].
(b) Vin,rms=160 [V] , Vo = 380 [V], 150W.

3. VOLTAGE FEEDBACK COMPENSATION USING THE NEW MODEL

For the voltage feedback compensation, an integral-and-lead compensator shown in Fig. 8 was used:

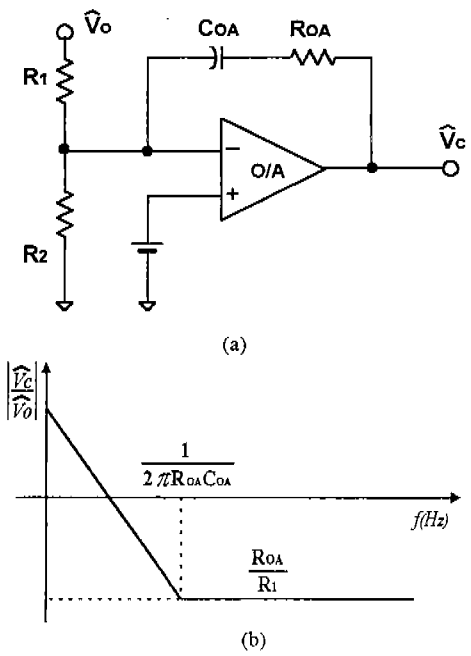

Fig. 8. Voltage compensator. (a) circuit diagram. (b) gain characteristics.

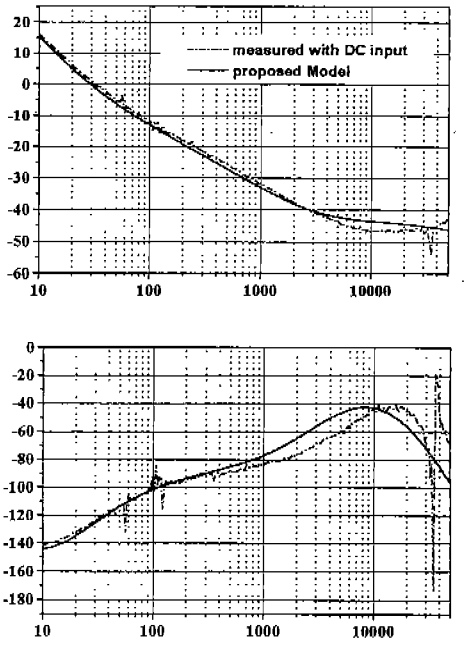

Fig. 9. The loop gain: input = 160[V]rms, ouput = 380 [V] , 200W.

$$G_v(s) = \frac{1 + sC_{oa}R_{oa}}{sC_{oa}R_1} = \frac{1 + s/\omega_z}{s/\omega_p}$$

This provides the optimum compensation for both resistive and constant power loads over the full input voltage and output load range [4].

For a resistive load, the zero should be placed at the same frequency as the loop gain crossover frequency:

$$\omega_z = \frac{1}{C_{oa}R_{oa}}. \qquad (13)$$

From the high frequencies flat gain, the value of R_{oa} is calculated:

$$\left| \frac{\hat{v}_c}{\hat{v}_o} \right|_{s\to\infty} = \frac{R_{oa}}{R_1} \qquad (14)$$

where, R_1 is determined in advance.

The value of C_{oa} can be calculated from (13) and (14), and the pole is determined as:

$$\omega_p = \frac{1}{C_{oa}R_1}.$$

In gain characteristics, the flat gain at high frequencies will transmit a considerable output ripple back to the control voltage $\hat{v}_c$, which would distort the input waveforms. This ripple, however, can easily be removed by using a 120Hz notch filter.

Figure 9 shows the loop gain of the PFC circuit. In this experiment, a 120Hz notch filter was not used. Thus, the crossover frequency of the loop gain was placed at 30Hz in order to minimize the effects of the output ripple on the control voltage.

Due to the technical difficulty in measuring the loop gain with AC input, the loop gain was measured only with DC input and compared with simulation obtained from the proposed model. The close agreement in Fig. 9 verifies the accuracy of the model.

4. CONCLUSIONS

This paper presented a new high-frequency small-signal model, which agrees up to high frequencies, over 1kHz. The small-signal model was derived from that of the DCM dc-to-dc converter, by incorporating the duty-ratio constraint unique to the PFC circuit, and adapting the method used in deriving the modulator gain for the voltage mode control.

The control-to-output voltage transfer functions with AC input and with DC input were compared with the prediction of the model. Also the loop gain with DC input was compared with the prediction of the new model.

The single-phase boost PFC circuit commonly contains a 120Hz output ripple. Thus, the crossover

frequency of the loop gain is designed to be very narrow, usually 10 ~ 30Hz, to minimize the distortion in the inductor current. However, if a 120Hz notch filter is used, the loop gain crossover frequency can be increased to improve the dynamics of the output voltage. In this case, the new small-signal model will be useful for the control design for the controlled on-time boost PFC circuit.

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