

# A New Low Loss Snubber Circuit Suitable for Multilevel Inverter and Converter

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**Abstract** --This paper proposes a new snubber circuit for multilevel inverter and converter. The snubber circuit makes use of Undeland snubber as basic snubber unit and can be regarded as a generalized Undeland snubber. The proposed snubber keeps such good features as fewer number of components, improved efficiency due to low loss snubber, capability of clamping overvoltage across main switching devices, and no unbalance problem of blocking voltage. Furthermore, the proposed concept of constructing a snubber circuit for multilevel inverter and converter can apply to any kind of basic snubber unit such as Holtz nondissipative snubber, McMurray efficient snubber, Lauritzen lossless snubber, etc which have been utilized for two-level inverter.

## 1 Introduction

Recently the multilevel inverter and converter have drawn tremendous interest for high voltage and high power applications [1]-[5]. The general structure of the multilevel inverter and converter is to synthesize sinusoidal voltage waveforms from several levels of voltages typically obtained from capacitor voltage sources. As the number of levels increase, the synthesized output waveform adds more steps, producing staircase waveform which approaches the sinusoidal wave with minimum harmonic distortion. More levels also mean that higher DC link voltage than voltage rating of device itself can be handled by series device without device voltage sharing problem and without the use of bulky and heavy transformer for multiple connections.

Until now, for multilevel inverter and converter, conventional RCD and RLD snubber as turn-off snubber and turn-on snubber, respectively, have been used widely and exclusively because

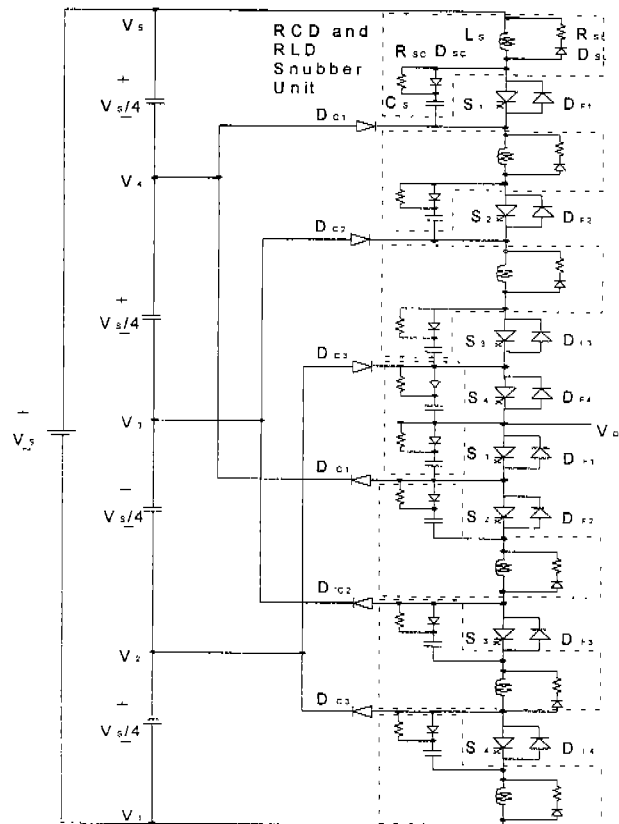


Fig. 1 Five-level inverter with conventional RCD and RLD snubber (within the dotted line).

it is easy to apply to multilevel inverter and converter as shown in Fig. 1 [4]-[5]. But this kind of snubbers need separate snubber circuit unit for each GTO which are composed of turn-off capacitors, turn-on inductors, resistors and diodes. Thus the total number of snubber components become considerably high and complex, thus resulting in highly costly multilevel inverter and converter. And since the large amount of snubber energy is fully dissipated in snubber resistor, system power loss can be very high, which causes

system efficiency to become very low. Furthermore, during turn-off process, the overvoltage of GTO can be very high, usually about 1.8 times higher than DC link voltage because there is only one small turn-off capacitor for each GTO to absorb the stored inductor energy. In addition, unbalance problem of the overvoltage, which results from combination of multilevel structure and RCD/RLD snubbers, makes voltage stresses of the switching devices worse[5].

To overcome the above-mentioned disadvantage of RCD/RLD snubber for multilevel inverter and converter, a new snubber topology suitable for multilevel inverter and converter are proposed. The proposed snubber utilizes Undeland snubber as basic snubber unit and can be regarded as a generalized Undeland snubber for multilevel structure converter. Its good features include fewer number of component, improved efficiency due to low loss snubber, capability of clamping overvoltage across switching main device and no unbalance problem of blocking voltage. This paper also explains in detail how to construct a snubber circuit for multilevel inverter and converter.

## 2. Review of Undeland Snubber as Basic Snubber Unit for Multilevel Inverter and Converter

Fig. 2(a) shows one inverter pole with the conventional Undeland snubber. In this paper, the Undeland snubber is to be utilized as basic snubber unit for multilevel inverter and converter [6]. The modified Undeland snubber, that is, the complementary snubber of the original Undeland snubber can be derived as shown in Fig 2(b) and its principle of operation is the same as the original Undeland snubber. The complementary snubber will also be used as basic snubber unit for negative arms of multilevel inverter and converter poles. As shown in Fig. 2(a) and (b), the snubber circuit consists of fewer components, which includes turn-off capacitor  $C_S$  for  $dv/dt$  limitation, turn-on inductor  $L_S$  for  $di/dt$  limitation, capacitor  $C_O$  for overvoltage clamping and snubber energy recovery normally about

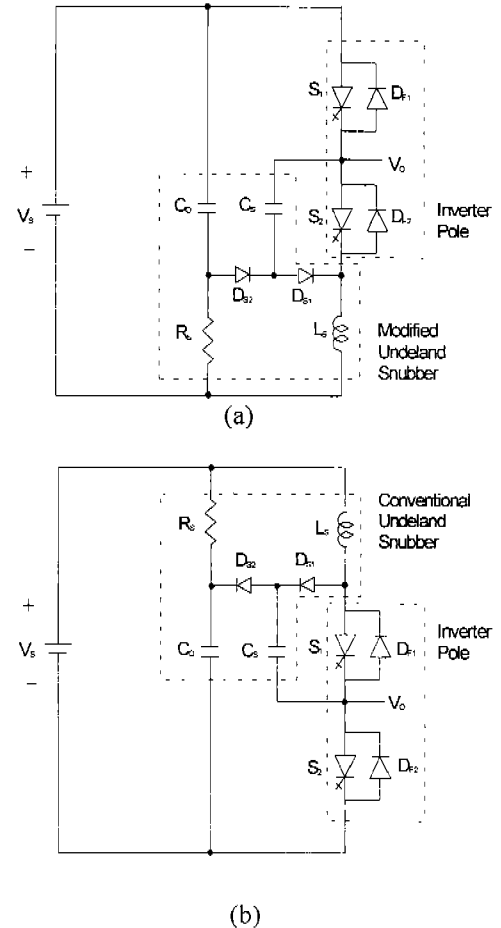


Fig. 2 (a)Conventional Undeland snubber circuit[8] , (b)Modified Undeland snubber.

ten times larger than  $C_S$ , resistor  $R_S$  for resetting snubber inductor and capacitor, and diodes. Such a simple circuit topology of Undeland snubber make itself good candidate for multilevel inverter and converter which essentially include a number of main switching device. In addition since the resistor  $R_S$  is not directly involved in snubbing action unlike RCD and RLD snubber, mechanical arrangements of components and cooling are much easier and simpler. In particular, Thanks to capability of clamping overvoltage at turn-off and no unbalance problem of overvoltage, the Undeland snubber is selected as the best basic snubber unit for multilevel inverter and converter.

## 3. The Proposed Snubber for Multilevel Inverter and Converter

An m-level multilevel inverter typically

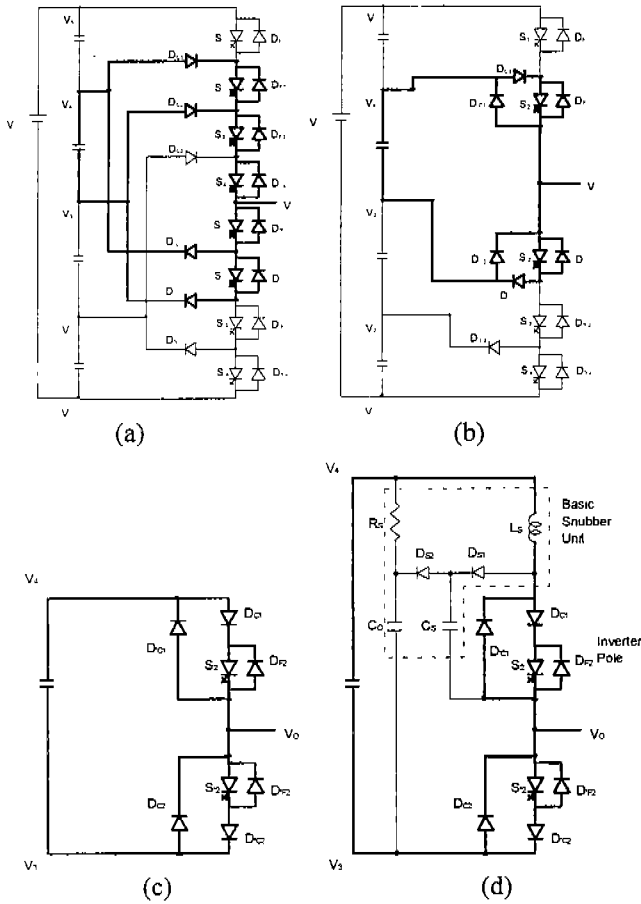


Fig. 3 Derivation of the proposed snubber for multilevel inverter (a)the operating part of circuit (thick line) during level changes between  $V_4$  and  $V_3$ , (b) Redrawn circuit of (a), (c)Equivalent two-level inverter during level changes between  $V_4$  and  $V_3$ , (d)Equivalent two-level inverter with a basic snubber unit.

consists of  $m-1$  capacitors on the DC bus and produces  $m$ -levels of the phase voltage. Fig. 3(a) shows one pole of five-level inverter in which the DC bus consists of four capacitors,  $C_1$ ,  $C_2$ ,  $C_3$ , and  $C_4$ . For a DC bus voltage  $V_S$ , the voltage across each capacitor is  $V_S/4$  and each device stress will be limited to one capacitor voltage level,  $V_S/4$ , through clamping diodes. Table 1 lists the voltage levels and their corresponding states. State condition 1 means the switch is on, and 0 is off. There exists four complementary switch pairs in each phase. The complementary switch pair is defined such that turning on one of the pair switches excludes the other from being turned on. In case of five-level inverter,

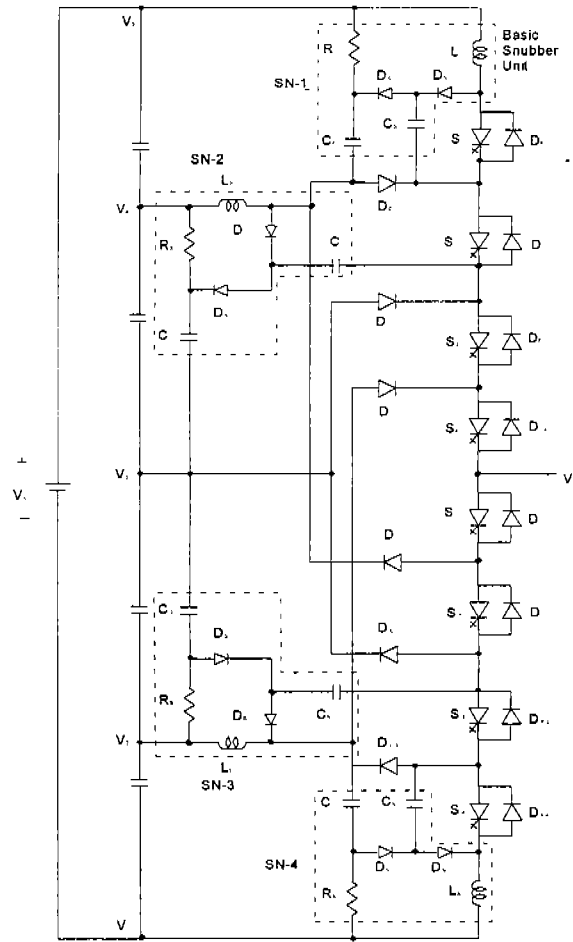


Fig. 4 Five-level inverter with the proposed snubber(within the dotted line).

the four complementary pairs are  $(S_1, S_1')$ ,  $(S_2, S_2')$ ,  $(S_3, S_3')$ , and  $(S_4, S_4')$  which, respectively, correspond to each level change, that is, between  $V_5$  and  $V_4$ ,  $V_4$  and  $V_3$ ,  $V_3$  and  $V_2$ , and  $V_2$  and  $V_1$ . Notice that the level changes occur only between adjacent levels. When investigating all level changes, we can find the operating part of circuit during each level change to converge to equivalent two level inverter which is composed of complementary pair switches and corresponding clamping diodes. For example, as shown in Fig. 3, consider level changes between  $V_3$  and  $V_4$ . The corresponding complementary pair is  $(S_2, S_2')$ . If  $S_2$  is on and  $S_2'$  is off, output level is  $V_4$ .

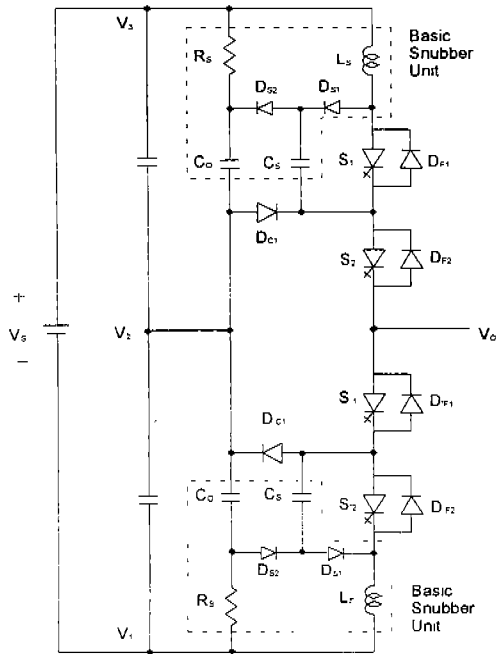


Fig. 5 Three-level inverter with the proposed snubber(within the dotted line).

Convesely, If  $S_2$  is off and  $S_2$  is on, output level is  $V_3$ . During these level changes the operating components of five-level inverter can be drawn with thick line as shown in Fig. 3(a). The thick-lined part of operating circuit can be transformed into Fig. 3(b) and can also be redrawn as Fig. 3(c) since switches  $S_3$ ,  $S_4$ , and  $S_1$  are always turned on irrespective of on/off condition of  $S_2$  and  $S_2$ . Fig. 3 (c) shows that the operating part of circuit is equivalent to the conventional two-level voltage source inverter. It follows that for the equivalent two-level inverter related to switching devices ( $S_2, S_2$ ), the basic snubber unit which have been used in two-level inverter can be applied as shown in Fig. 3(d). In the same way, all the equivalent two-level inverter corresponding to each level change, that is, each complementary pair in multilevel inverter can be derived, and the same basic snubber units can apply to them. So, we can obtain five-level inverter equipped with a snubber circuit as shown in Fig. 4. When using the same principle, we can get the snubber circuits for 3-level, 4-level like Fig. 5 and 6. Furthermore, a generalized snubber for any multilevel inverter and converter can be achieved. The generalized snubber has the same good features as the

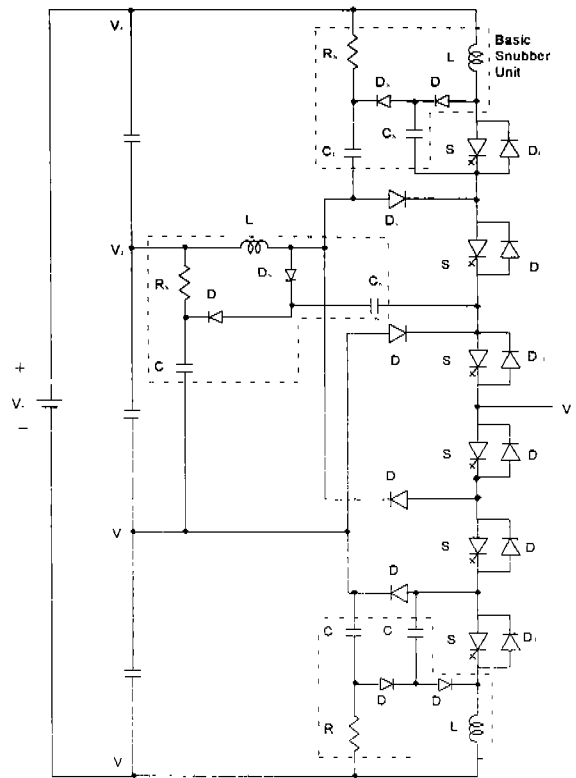


Fig. 6 Four-level inverter with the proposed snubber(within the dotted line).

basic snubber unit. In this paper since we use the Undelmand snubber as the basic snubber unit, the characteristics of the generalized snubber are such as fewer number of component, improved efficiency due to low loss snubber, capability of clamping overvoltage across switching main device and easy arrangements and mounting of snubber circuit. Furthermore thanks to the snubber structure, the generalized snubber has no unbanlance problem of overvoltage unlike RCD/RLD snubber, thus resulting in equal voltage stress to all main switching devices except clamping diodes.

#### 4. Simulation Results

In order to prove the effectiveness of the proposed snubber circuit, we adopt 5-level inverter as an example inverter for application of the proposed snubber. We simulated one pole of the 5-level inverter shown in Fig. 4 with the output terminal  $V_o$  connected to the midpoint of input source voltage  $V_s$  through series-connected RL load. The simulation tool we used is PSPICE 6.3a version. The simulation

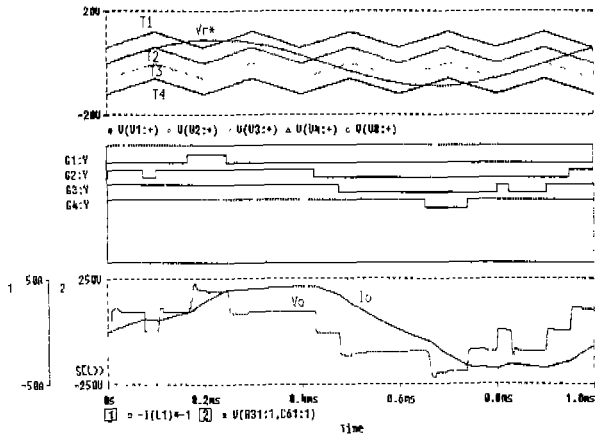
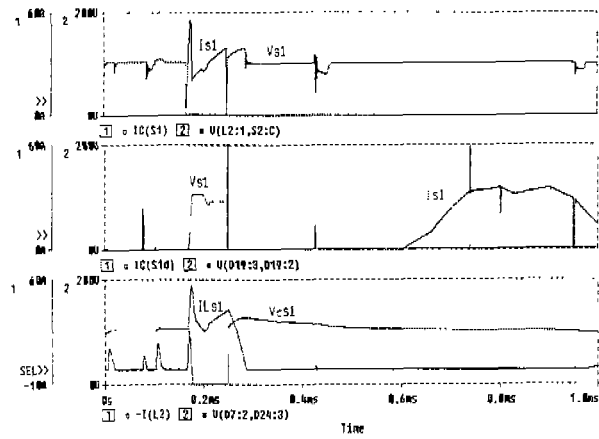


Fig. 7 PWM generation-related signals(first plot and second plot) and overall output voltage  $V_o$  and current  $I_o$  waveforms during one fundamental period(third plot).

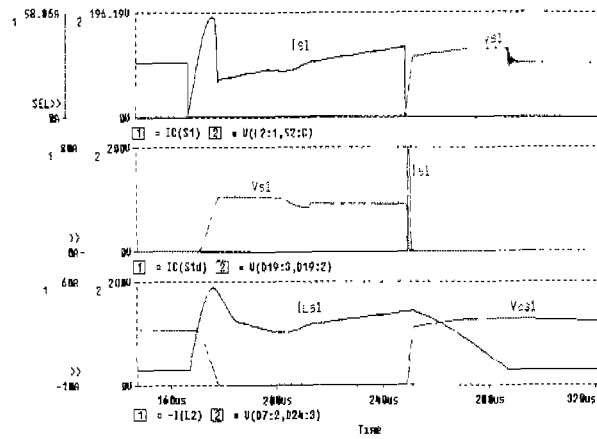
conditions are as follows

$$\begin{aligned}
 V_s &= 400 \text{ [V]} \\
 I_{o \max} &= 50 \text{ [A]} \\
 L_s &= 10 \text{ [\mu H]}, \quad R_s = 5 \text{ [\Omega]} \\
 C_s &= 1 \text{ [\mu F]}, \quad C_o = 40 \text{ [\mu F]}
 \end{aligned}$$

Fig. 7, 8 and 9 are the obtained simulation results under the same time base so that the overall operation of the proposed snubber can be understood very well. Fig. 7 shows PWM-related reference signal  $V_r^*$ , triangular waveforms  $T_1 - T_4$  and overall output voltage and current waveforms. The PWM signals  $G_1, G_2, G_3,$  and  $G_4$  which are generated by comparing reference signal and triangular signals apply for switches  $S_1, S_2, S_3,$  and  $S_4$ , respectively, and their complemented signals also apply for switches  $S'_1, S'_2, S'_3,$  and  $S'_4$ , respectively. The output voltage and current waveforms shown in the third plot have good waveforms with no adverse effects of the proposed snubber. Fig. 8 and 9 show voltage and current waveforms of switches  $S_1, S_2, S'_1, S'_2$ , and snubber components  $L_s$  and  $C_s$  of basic snubber circuits SN1 and SN2 and show their detailed(zoomed) waveforms before and after switching instants of switches. It proves that the proposed snubber circuit have good snubbing effects on main switches in terms of transient switching peak values, dissipative power and snubber losses.



(a)

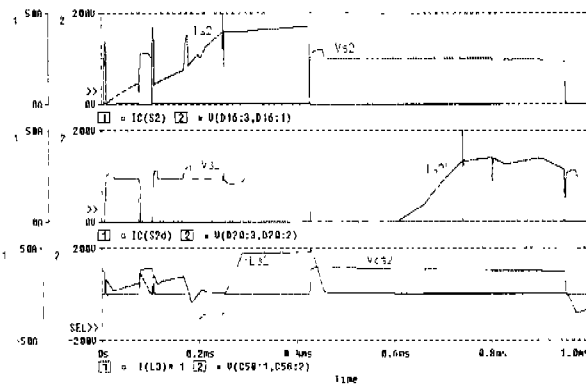


(b)

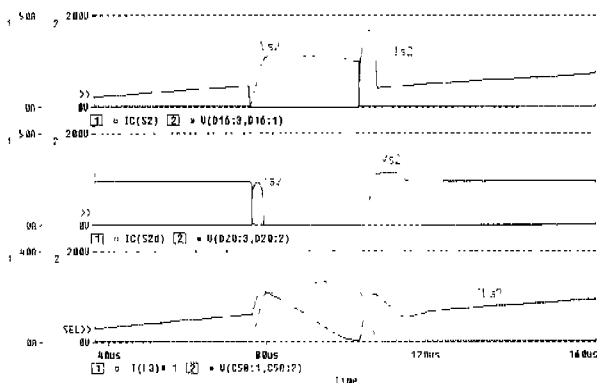
Fig. 8 (a) voltage  $V_{s1}, V_{s1}'$  and current  $I_{s1}, I_{s1}'$  of switches  $S_1$  and  $S'_1$ , and snubber inductor current  $I_{Ls1}$  and capacitor voltage  $V_{cs1}$  of  $L_s$  and  $C_s$  in snubber circuit SN-1, (b) their zoomed waveforms around time point 0.2 msec.

## 5. Conclusion

This paper proposes a new snubber circuit for multilevel inverter and converter. The snubber circuit makes use of Undeland snubber as basic snubber unit and can be regarded as a generalized Undeland snubber. The proposed snubber keeps such good features as fewer number of component, improved efficiency due to low loss snubber, capability of clamping overvoltage across switching main device and no unbalance problem of blocking voltage.



(a)



(b)

Fig. 9 (a) voltage  $V_{s2}$ ,  $V_{s2}'$  and current  $I_{s2}$ ,  $I_{s2}'$  of switches  $S_2$  and  $S_2'$ , and snubber inductor current  $I_{Ls1}$  and capacitor voltage  $V_{Cs1}$  of  $L_s$  and  $C_s$  in snubber circuit SN-2, (b) their zoomed waveforms around time point 0.1 msec.

Furthermore, the proposed concept of constructing a snubber circuit for multilevel inverter and converter can apply to any kind of basic snubber unit such as Holtz nondissipative snubber, McMurray efficient snubber, Lauritzen nondissipative snubber, etc which can be utilized for two-level inverter.

### References

[1] Nam S. Choi, Jung G. Cho and Gyu H. Cho, "A General Circuit Topology of Multilevel Inverter," IEEE PESC, pp96-103, 1991.  
 [2] C. Hochgraf, R. Lasseter, D. Divan and T. A. Lipo, "Comparison of Multilevel Inverter for Static Var Compensation," IEEE IAS Annual

Meeting Conf. Record, pp. 921-928, 1994.

[3] J.-S. Lai and F. Z. Peng, "Multilevel Converters-A New Breed Power Converters," IEEE IAS Annual Meeting Conf. Record, pp. 2348-2356, 1995.  
 [4] G. Sinha, C. Hochgraf, R.H. Lasseter, D.M. Divan T.A. Lipo, "Fault Protection in a Multilevel Inverter Implementation of a Static Condenser," IEEE IAS Annual Meeting Conf. Record, pp. 2557-2564, 1995.  
 [5] B. S. Suh, D. S. Hyun and H. K. Choi, "A Circuit Design for Clamping an Overvoltage in Three-level GTO Inverters," IEEE IECON, pp651-656, 1994.  
 [6] T. Undeland, F. Jensen, A. Steinbakk, T. Rogne and H. Hernes, "A Snubber Configuration for Both Power Transistor and GTO PWM Inverters," IEEE PESC, pp42-53, 1984.

**Table 1** Five-level inverter voltage levels and corresponding switch states

Output $V_o$	Switch State							
	$S_1$	$S_2$	$S_3$	$S_4$	$S_1$	$S_2$	$S_3$	$S_4$
$V_5=V_s$	1	1	1	1	0	0	0	0
$V_4=3V_s/4$	0	1	1	1	1	0	0	0
$V_3=2V_s/4$	0	0	1	1	1	1	0	0
$V_2=V_s/4$	0	0	0	1	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

( 1 : On , 0 : Off)