Analysis of Multi Level Current Source GTO Inverter for Induction Motor Drives

Takayuki ARASE and Kouki MATSUSE
Department of Electrical Engineering, Meiji University
1-1-1 Higashi-mita, Tama-ku, Kawasaki 214-8571, JAPAN
Phone: +81-44-934-7298 Fax: +81-44-934-7298

Abatract- This paper discusses a triple stage current source GTO inverter system for high power motor drives.The energy rebound circuit of the triple stage inverter not only controls the spike voltage of the GTO inverter but also facilitates PWM control of the thyristor rectifier operated at unity fundamental input power factor. Based on Pspice simulation and experiments, the principles and PWM pulse pattern for removing specific lower harmonics in the inverter's output current are discussed in detail.

1. INTRODUCTION

Current source inverters are widely used to drive high power induction motors because they have full four quadrant and short circuit proof capabilities. However, the current source inverter unit cannot cope with extremely high loads requiring several thousand volts and amperes, because of the device's capacity rated. The authors have previously proposed a double stage current source GTO inverter system which can control the peak spike voltage, thus increasing the capacity and decreacing harmonics. [1]-[3]

Generally, the current source inverter output voltage includes spike voltages generated by switching devices.The spike voltages constitute invalid power and shorten the life span of load devices.

In this paper, to enlarge the capacity and improve the voltage pulsation, the authors propose a triple stage current source GTO inverter system with an energy rebound circuit that limits and controls the peak spike voltages, and analyze and discuss its basic characteristics and waveforms.

2. MAIN CIRCUIT CONFIGURATION

Figure 1 shows the proposed main circuit configuration (triple stage current source GTO inverter). It is composed of the thyristor converter section, the GTO inverter section, and the energy rebound circuit. The energy rebound circuit is composed of diode bridge (D1-D6), one capacitor (C) and two GTO's (G7,G8). The converter and inverters are connected to the dc link filter inductors (Ld) in parallel. If a leakage inductance (L0) exists in the supply line, a capacitor (C0) is required to assist in turning off the thyristors and as a filter. Generally, an additional rectifier or a transformer is connected to the inverter output terminals to maintain a good current balance between the unit inverters, but this increases the size and weight of the inverter equipment. In this main circuit therefore, the terminals of the inverter output connect directly to the induction motor in parallel without a transformer.

The energy rebound circuit performs the following important roles:

(1) Stores the commutation energy in the inverter circuits.

(2) Supplies voltage for turning off all thyristors in the converter.

(3) Controls the spike voltage.

The reactive power in the induction motor is stored temporarily in the dc capacitor C during commutation in the inverter circuit and is discharged into the dc part by turning on or off G7 and G8 synchronously. At this time, the peak spike voltage in the inverter output voltage is lower than the capacitor voltage Ec. The capacitor voltage Ec can be adjusted by controlling the discharge period $\omega\tau$ as shown in Fig.2. This means that the output spike voltage can also be restricted and controlled. During the discharge period $\omega\tau$,

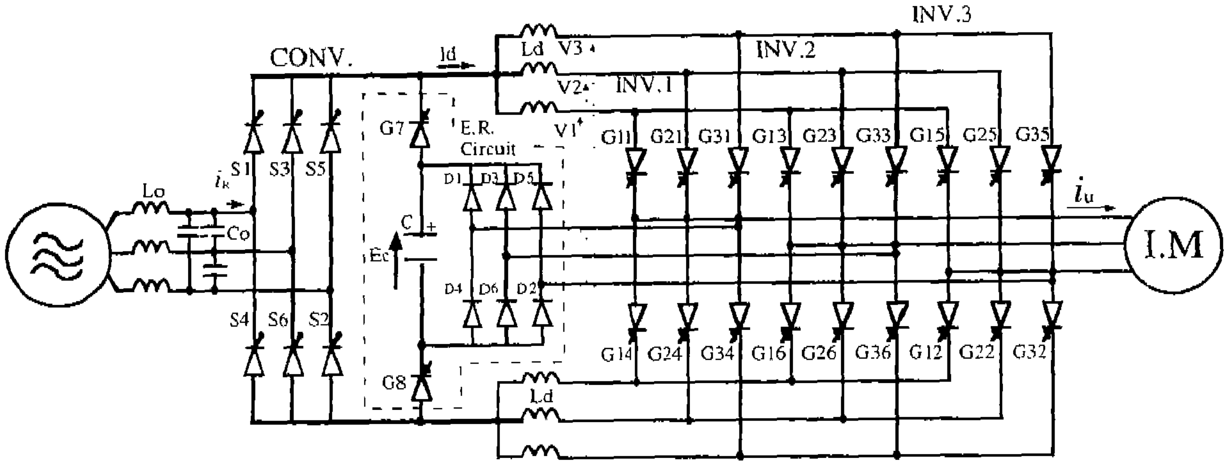

Fig.1 : Main circuit configuration of Triple current Source GTO Inverter System

all thyristors in the rectifier are in the reverse-biased state and turned off.

3. CONVERTER CONTROL METHOD AND PRINCIPLE

When applying PWM control techniques to a thyristor bridge rectifier, some means is necessary to turn it off forcibly at any time, since it cannot automatically turn itself off. In our method, PWM control of the thyristor converter is done by discharging the reactive power stored in the energy rebound circuit, so there is no need for some complicated circuitry for turning off the thyristor.

Figure 2 shows waveforms of the thyristor rectifier section operating at unity fundamental input power factor. It shows the waveforms of the supply phase voltages, V_R, V_S, V_T, gate signals for the thyristors S1-S6 and GTO's G7, G8 in the energy rebound circuit, the dc output voltage E_d, and the ac input current i_R consisting of six pulses. Ec is the capacity voltage in the energy rebound circuit, τ is the discharge period, and Vp is the maximum value of the line-to-line supply voltage. The gate signals shown in the block (▨) are pulses for switching on the thyristors in the same phase to make the dc link current flow, and called short circuit pulses. During the period when the thyristors are operated at the same phase, the dc output voltage is zero as shown in Fig.2. This short circuit period is given by $(1-\lambda)T$, where λ is a modulation factor (0 to 1), and T is equal to 1/12 of the supply frequency. The dc link current, or inverter output current, is controled by adjusting λ. The input current i_R is composed of 1/3 λ T, 2/3 λ T, and λ T, but since the pulse for λ T occurs during the discharge period $\omega\tau$ it actually consists of 1/3 λ T and 2/3 λ T.

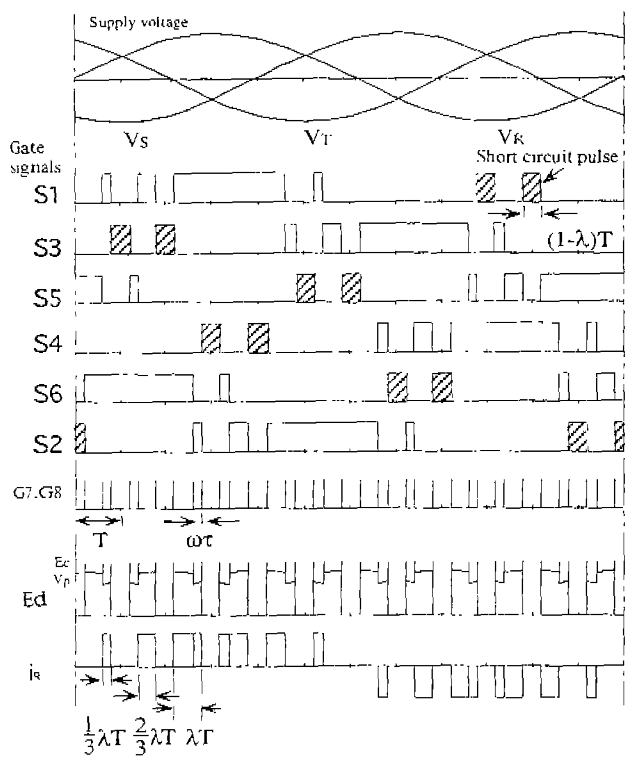

Fig.2 : Converter PWM pattern operating at unity fundamental input power factor

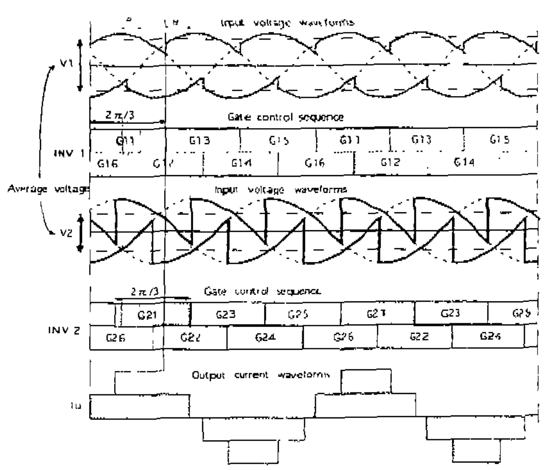

Fig.3: Waveforms of a conventional double stage GTO inverter

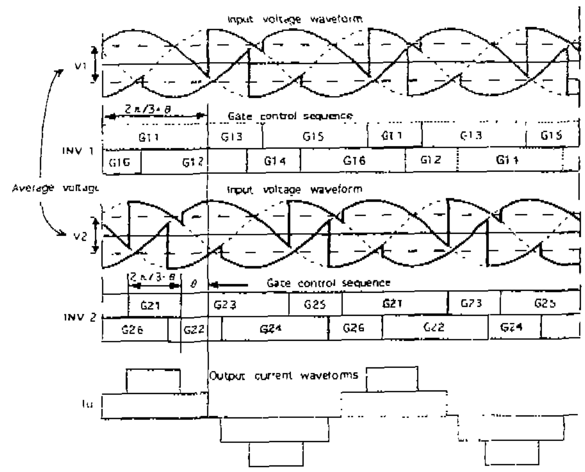

Fig.4: Waveforms of double stage inverter supplied by a common dc source

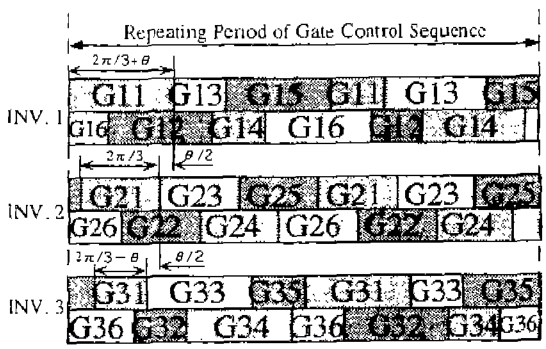

Fig.5 : Gate control sequence of triple stage inverter supplied by a common dc source

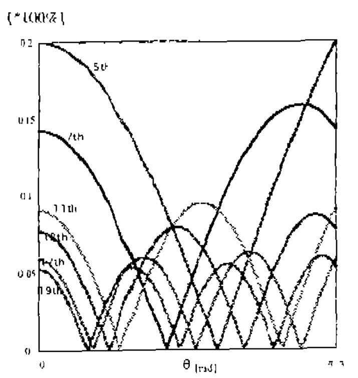

Fig.6(a) : Harmonic components of double stage inverter

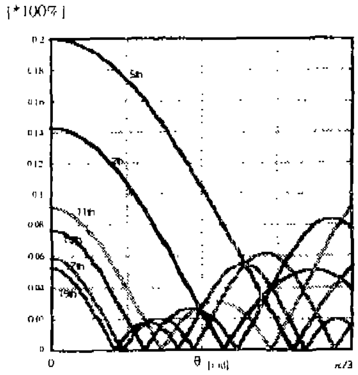

Fig.6(b) : Harmonic components of triple stage inverter

For PWM control of the rectifier, two conditions must be met: the capacitor voltage Ec must be higher than the line-to-line peak voltage, and the discharge period $\omega\tau$ must be longer than the turn-off time of the thyristors.

4. INVERTER CONTROL METHOD

Figure 3 shows the conventional control method for a double stage inverter, each unit of which is supplied by a separate dc source. Here, there are five levels of the inverter output current, done by shifting each unit inverter, which has the same pulse length ($2/3\,\pi$), by a phase difference of θ. The relation between the input dc voltages V1, V2 and the gate pulse difference θ is given as follow:

$$V1 = 1.35E_M \cos(\phi - \theta/2) \tag{1}$$

$$V2 = 1.35E_M \cos(\phi + \theta/2) \tag{2}$$

where ϕ denotes the phase of the power factor, E_M is the output line-to-line voltage on the I.M side, and the suitable phase difference θ ($0 < \theta < \pi/3$) is determined from Fourier Series analysis as shown later.

When this gate pulse pattern is applied to a double stage inverter supplied by a common dc source, one cannot obtain a balanced output current or voltage. That is, the problem of power imbalance between inverters exists, because V1 and V2 are not equal. To solve this problem, the pulse pattern shown in Fig.4 is used. The gate sequence consists of short pulses ($2/3\,\pi - \theta$) and long pulses ($2/3\,\pi + \theta$). The input dc voltage is given as follow:

$$V1 = V2$$

$$= 0.816E_M\left\{\frac{2\cos\phi}{4\pi^2/9-\theta^2}\left(\frac{2\pi}{\sqrt{3}}\cos(\theta/2)-\theta\sin(\theta/2)\right)\right\} \quad (3)$$

Because the average voltages V1 and V2 with respect to the motor neutral point are equal, the double stage inverter can be driven from a common dc source.

The problem of power imbalance must be solved when driving the triple stage inverter as well. Figure 5 shows the gate control sequence applied to the proposed main circuit. Note that the gate control sequences for INV.1 and INV.3 are similar to that for the double stage inverter, while that for INV.2, which is set at $2\pi/3$, is independent of the others. The gate sequences of Fig.5 produce a balanced output current and voltage.

The relations between the phase difference θ and the harmonic components (n-th order harmonics/1st order harmonics) of the output current are shown in Fig.6(a)(b). From this figure, we can see that it is possible to reduce certain harmonics by adjusting θ, and that the triple stage inverter's harmonics are lower than those of the double stage across the border.

5. EXPERIMENTAL AND SIMULATION RESULTS

Figure 7 shows the equivalent models of the GTO and thyristor, and the per phase equivalent circuit of the induction motor for the Pspice simulation. Each GTO is connected in parallel to a snubber circuit composed of a diode Ds, a resistor Rs, and a capacitor Cs. Another snubber circuit, com-

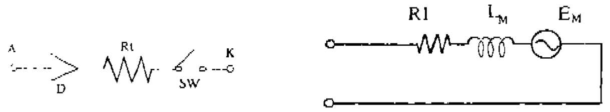

Fig.7 : Equivalent circuit model of switching device and I.M

TABLE.1 : Parameters for the simulation

ac supply voltage	E_R = 50 V
Supply Capacitor	C0 = 40 μF
Supply inductance	L0 = 998 μH
Discharging period	τ = 30 usec
DC link inductor	Ld = 200 mH
E R C. Capacitor	C = 600 μF
Snubber Capasitor and Resistor	Cs = 0 22μF Rs = 150 Ω
Per-phase parameters of I.M	L_M = 390 μH R_l = 42.5 mΩ EM = 28.8 V
Modulation factor	λ = 07

TABLE.2 : Ratings of tested motor

5.5 kW	400 Hz
200 V	8 pole
25 A	5950 rpm

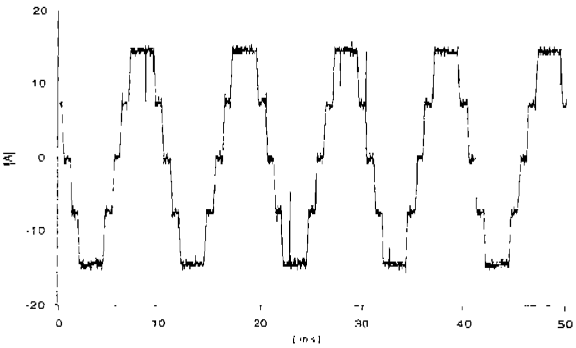

Fig.8: Experimental result of double stage inverter output current

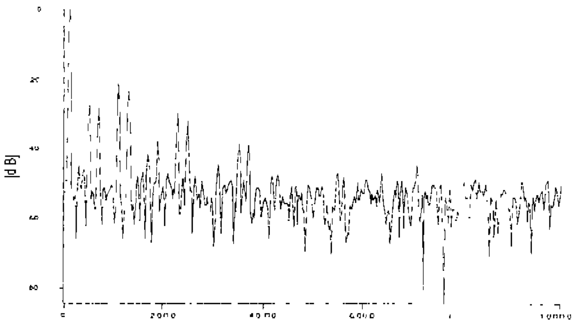

Fig.9: Harmonic spectrum of double stage inverter output current

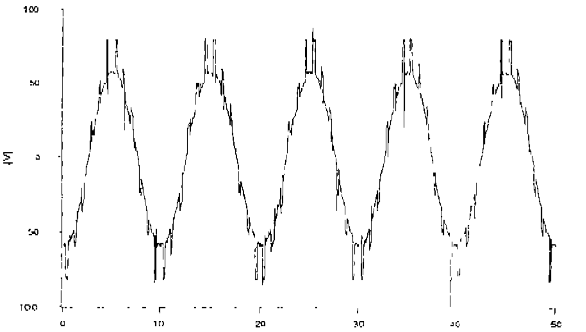

Fig.10 : Experimental result of double stage inverter output voltage Vuv

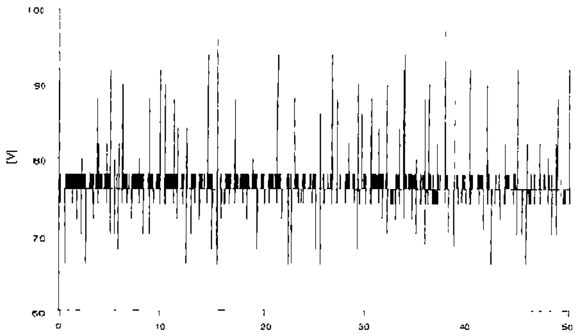

Fig.11: Experimental result of double stage inverter capacitor's voltage Ec

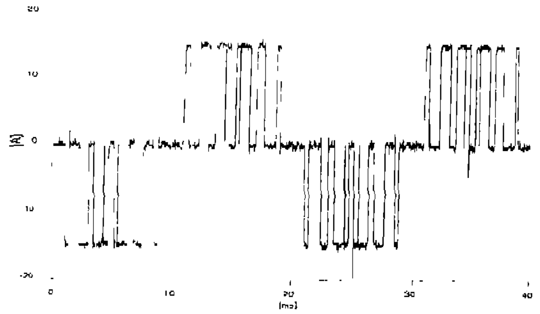

Fig.12: Experimental result of converter input current

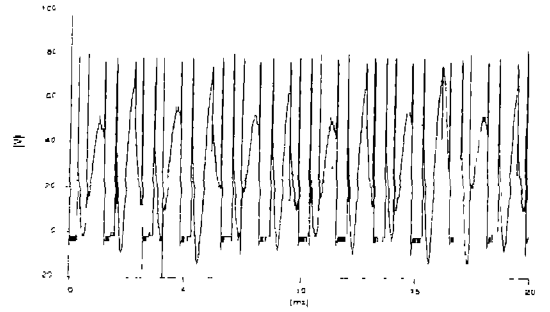

Fig.13: Experimental result of converter output voltage

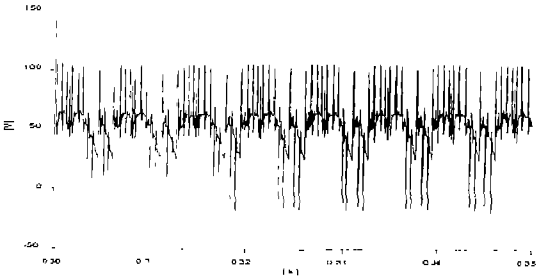

Fig.14(a): Simulation results (input voltage of INV.1)

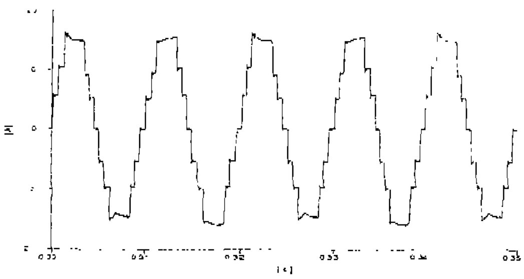

Fig.15(a): Simulation results
(triple stage inverter outpuu current)

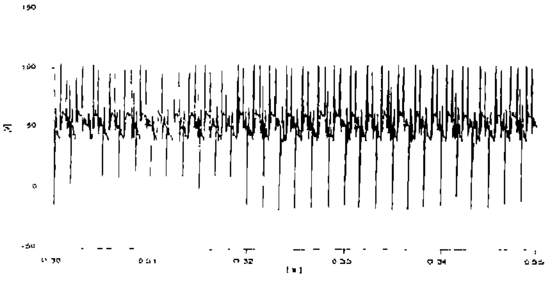

Fig.14(b): Simulation results (input voltage of INV.2)

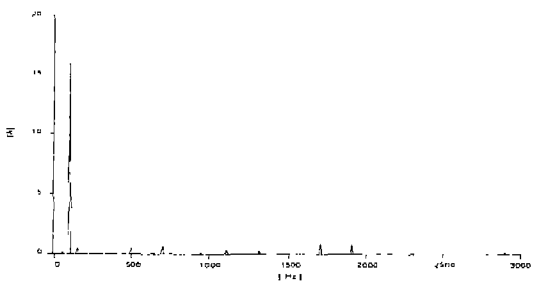

Fig.15(b): Simulation results
(output current FFT analysis)

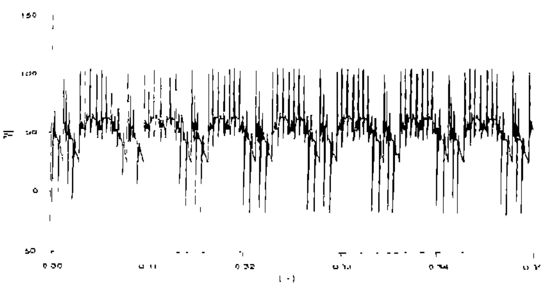

Fig.14(c): Simulation results (input voltage of INV.3)

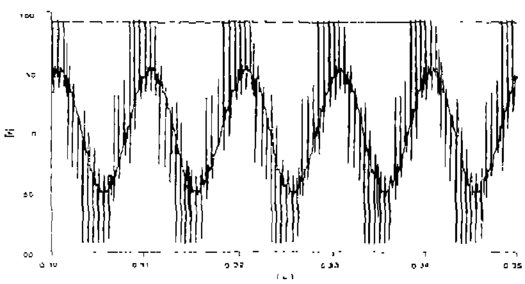

Fig.15(c): Simulation results
(output current voltage and capacitor's voltage)

posed of a resistor and a capacitor, is attached to each thyristor. Table 1 shows the parameters and variables for the simulation and experiment, and Table 2 shows ratings of the tested motor.

The experimental results for the double stage inverter output current and voltage are shown in Figs.8 and 10, where θ is set at $\pi / 6$ and the inverter frequency is 100 Hz. The capacitor's voltage Ec is shown in Fig.11. From Figs.10 and 11, we can confirm that the peak spike voltage is lower than the capacitor's voltage Ec.

The waveforms of the converter input current i_R and output voltage E_d in the experiment are shown in Figs.12 and 13. These figures confirm that the thyristors are completely turned off by the reactive power stored in the cnergy rebound circuit.

Figures 14 and 15 show simulation results of the triple stage inverter by the Pspice similator. From each input voltage of the triple stage shown in Fig.14(a)-(c), we see that the average input voltage is nearly equal, and from FFT analysis in Fig.15(b) that the 5th and 7th harmonics are about the same amplitude, as was designed in Fig.6(b). Here θ is set at $2\pi/9$ and the inverter frequency is 100 Hz.

6. CONCLUSION

From experimental and simulation results, we found that it is possible to control the triple stage inverter by a gate sequence similar to that of the double stage inverter. We also saw that the energy rebound circuit can function to control the peak spike voltage and by the reactive power stored in that circuit, turn off the thyristors.

REFERENCES

[1]K.Matsese,H.kubota and L.Huang : Performance of PWM-Controlled Thyristor Rectifier Operating at Unity Fundamental Power Factor in PWM Current Source GTO Inverter System for Induction Motor Drives,IEEE Trans.Ind.Appl,.vol.30,pp.699-706,1994

[2]T.Umeshita,T.Sekiya and K.Matsuse : Basic Characteristics and Analysis of Double Current Source GTO Inverter System,PEMC '96,Vol.2,pp287-290,2-4Sept.,1996

[3]A.Nabae,T.Shimamura,I.Shimizu and R.Kurosawa:Performance of Slip-Frequency-Controlled Induction Moters,TOSHIBA Review Vol.31 Nr.7,pp.599-604,1976