A NOBLE DEAD TIME MINIMIZATION ALGORITHM FOR REDUCING THE INVERTER SWITCHING LOSSES

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ABSTRACT - In this paper, a noble dead time minimization algorithm is presented for developing the outputs of inverters. The adverse effects of the dead time are examined. The principle of the proposed algorithm is explained with the conduction modes of the output currents. The H/W and the S/W construction method of the proposed algorithm are also presented. The validity of the proposed algorithm is verified by comparing simulation and experimental results with those of the conventional methods. It can be concluded from the results that the proposed algorithm have the virtue which is able to reduce the numbers of inverter switching and the harmonics in the output voltages, and which make the output voltage equal to the reference value.

1. INTRODUCTION

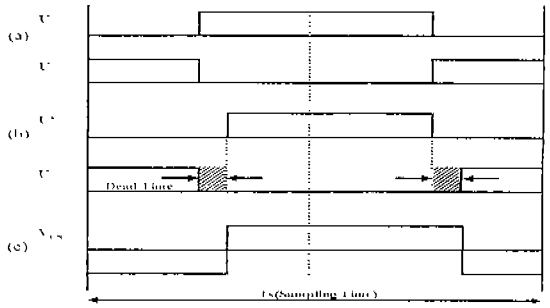
The inverters have been widely used in the motor drive systems. As a controllable source, the inverter can generate the desired current waveforms by pulse width modulation (PWM)[1]-[3] which varies the turn-on and turn-off times of switching devices. During the last few decades, there have been many researches and reports about PWM techniques and their effects. In order to reduce the level of low order harmonics and numbers of switching and to maximize the utilization of DC voltage, various modulation strategies have been developed and revised. As the switching device changes the switching state, a small blanking time exists to guarantee that both switches in an inverter leg never conduct simultaneously. Although each dead time is short, the accumulated delays during the entire cycle causes reduction of the desired fundamental output voltage and distortion of current waveforms. To compensate dead time in PWM, various industry approaches have been suggested. Most of the dead time compensations are based on the average theory that the reduced volt-seconds are averaged over entire cycle and then added to command value.[4] In [5], they compensate not only the magnitude but also the phase delay instantaneously for each impressed pulse. Seung-ki Sul et al considered the switching delay and voltage drop into the dead time compensation scheme.[6] These provide a more accurate compensation but increase the overhead on processors. The pulse based algorithm is also limited to the carrier frequencies because of the calculation time.

In this paper, an algorithm that minimizes the insertion of the dead time is proposed. The generation of the harmonics and the reduction of fundamental component according to the variation of the dead times are specified. The principle of the proposed algorithm is examined with the conduction modes of the inverter. The S/W and the H/W realization of the proposed algorithm are also presented. The validity of the proposed method is verified by experimental results comparing the distortion factor, the amplitude of the fundamental current and the numbers of switching with the conventional compensation method.

2. THE EFFECT OF THE DEAD TIME OF INVERTERS

Fig. 1 shows the ideal gate drive signals and actually impressed gate drive signals containing the dead time. To avoid the so-called shoot-through, the actual gate signals must be delayed by the dead time as Fig 1-(b). But the unwanted delay time makes the output current to contain

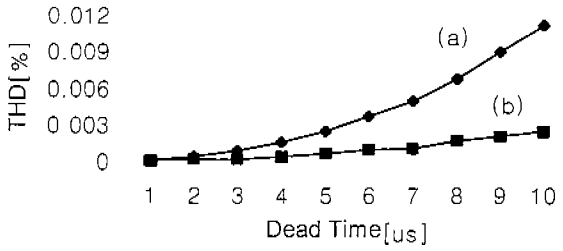
the harmonics. It had been reported



(a) ideal switch pattern
(b) gate drive signal with dead time
(c) impressed U phase voltage by (b)
Fig. 1 The gate drive signals of inverter

from [3] that the impressed pulse voltage in the middle of the sampling time has least harmonics. Although the voltage as a result of each gate drive pulse during the sampling time is not much affected, the resultant voltage during a cycle is significantly reduced owing to the dead time. And it distorts the waveform. When the modulation index is 0.9, the carrier frequency is 5kHz and the dead time is varied from 1μs to 10μs, Fig 2 shows the simulation results. As specified from (a), the more dead time is inserted, the more output current is distorted. Fig. (b) is simulation results of the dead time compensation described in [4]. By using the compensation method, the distortion is evidently reduced but using the compensation method also generates the harmonics in proportion to the dead time. The harmonics appeared at the motor terminals would induce the heat and the degradation of the efficiency of electrical machines.

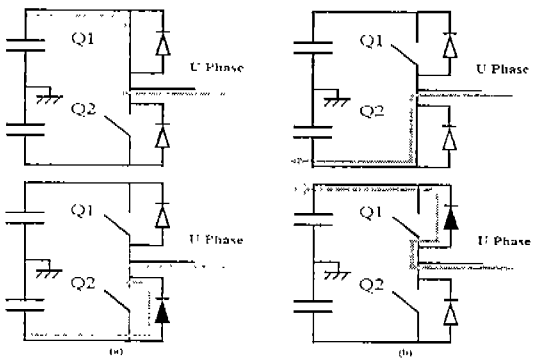
In the field of motor drives, the speed controller must adopt a voltage compensator or a dead time compensation algorithm to acquire the high performance torque control because the impressed voltage of the inverter is smaller than the reference one. In the mean while, the speed sensorless control of AC motors needs the terminal voltages to estimate the rotor speed, the reference voltage is used instead of measured one. But this leads estimation errors in the estimator due to the phase and the amplitude errors between the reference and the real ones. It causes a deterioration of the control performances.



(a) THD without a compensation of dead times
(b) THD with the compensation of dead times
Fig. 2 Simulation results about the THD(Total Harmonic Distortion Factor) of inverter output currents according to the variation of dead times

3. DEAD TIME MINIMIZATION ALGORITHM

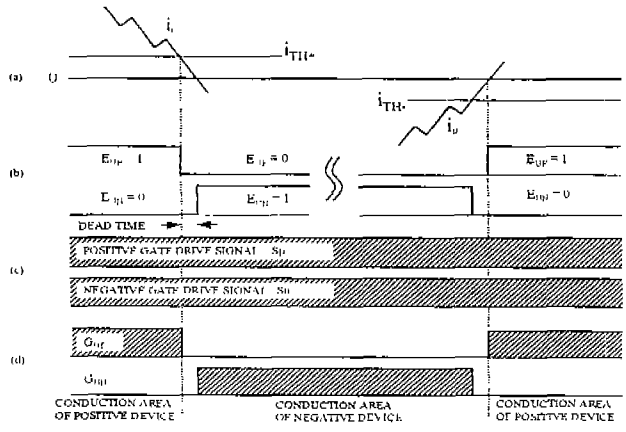
With an assumption that the polarity of the current is not changed during the sampling time at the inductive load just like induction motors, a switching device of one inverter leg should not turn-on although the gate drive signal is offered. Fig. 3 explains the possible conduction modes of one inverter leg. If we assume the current has the positive direction when the current flows from the source to the load, Fig. 3-(a) denote the two possible conduction modes under the condition of the positive current. When the gate drive signal as Fig. 1-(a) is offered to each switches, self-commutation device of the lower leg do not meet the turn-on condition even if U- signal is impressed because the current flows continuously to the load. But the anti-parallel diode conducts continuously



(a) Conduction modes of a positive current
(b) Conduction modes of a negative current
Fig. 3 Equivalent diagrams of the inverter and the conduction mode

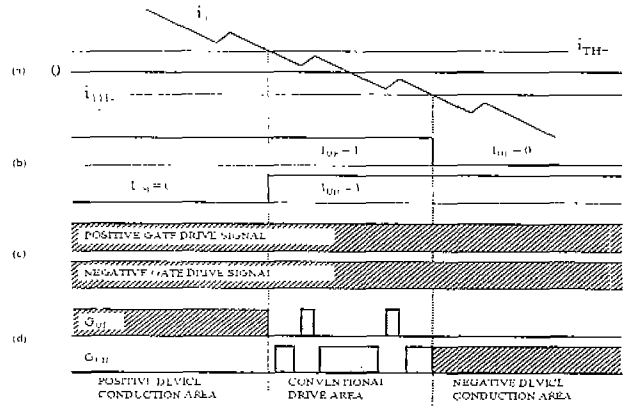
the current to load.

It does not need to offer a gate drive signal to self-commutation device. Therefore the dead time is also no need to be inserted as Fig. 1-(b). The case, negative current flows, is the same as the positive current flows. Whenever the polarity of the current is not changed, it can be driven by the gate signal without dead times. But the case, which the current changed to another polarity, must be considered. In Fig. 4, a method that inserts the dead time just once during the polarity change of the current is shown. The i_{IH+} and i_{IH-} denote the positive and the negative threshold of the current respectively. If the current is smaller than i_{IH+}, the selection signal of the positive device is zero. And then the current is naturally reduced to zero during the dead time. Thereafter the selection signal of the negative device is chosen as 1. The ideal gate signal of the PWM method is shown in Fig. 4-(c). The ideal gate signal takes a logical AND with the selection signal of the device to make the proposed gate drive signals. When the current flows to the negative direction, the logic is same as above. The proposed method will work well in the case of a large current with an inductive load. Though the inductive load has a continuous current, there may have current chattering and discontinuous conduction mode. And the case, that current sensors have a significant drift, might cause an offset problem. So, we suggest another method that has a bandwidth during the polarity change. We assume that the current flows to positive direction and that the current is lager than i_{IH-} and smaller than i_{IH+}, the gate drive signal follows the conventional gate drive signal with the dead time. In this band, the selection signals of the positive and the negative device are 1. During one cycle of the current, the gate drive signal follows the logical AND between the ideal gate signal and the selection signal of device. When the current flows from the negative to the positive direction, the logic is same as the case of the positive current. Even if the current is small one in the discontinuous conduction mode, using the bandwidth during the polarity change can also minimize the totally inserted dead time. Fig. 6 and Fig. 7 show the S/W implementation of Fig. 4 and Fig. 5, respectively.



(a) the threshold and current of the inverter
(a) the selection signals of the each device in one inverter leg
(b) ideal switching pattern of the upper and the lower device
(d) the proposed gate drive signal

Fig. 4 A method that insert the dead time just once during the polarity change of the current.



(a) the threshold and current of the inverter
(c) the selection signals of the each device in one inverter leg
(d) ideal switching pattern of the upper and the lower device
(d) the proposed gate drive signal

Fig. 5 A method having a bandwidth during the polarity change of the current.

4. THE SIMULATION RESULTS

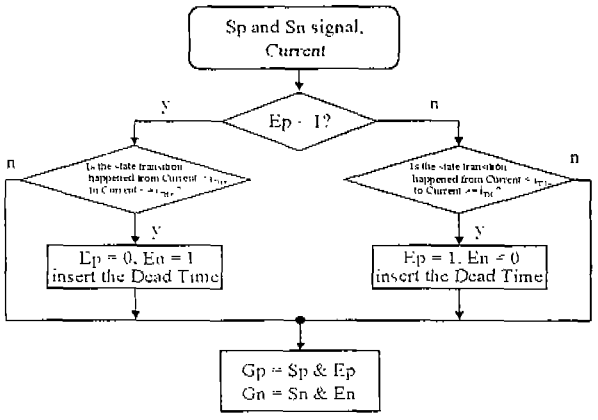


Fig. 6 Software flowchart of the method as shown in Fig. 4

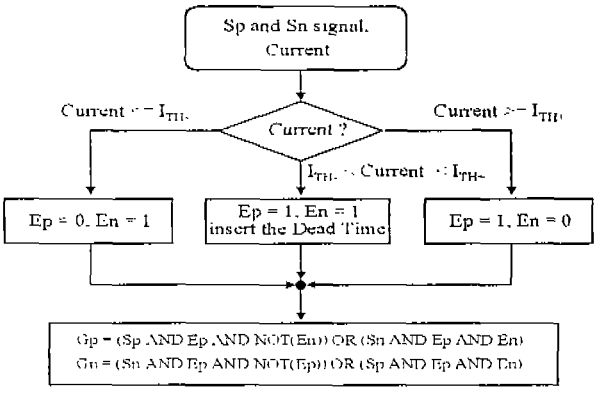
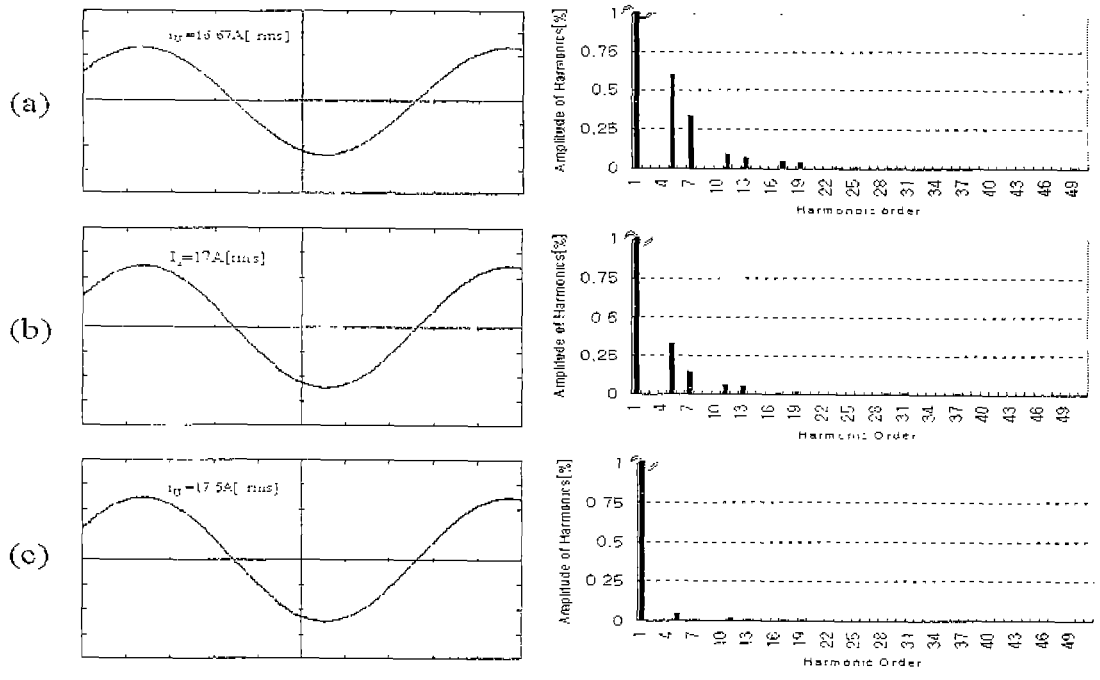


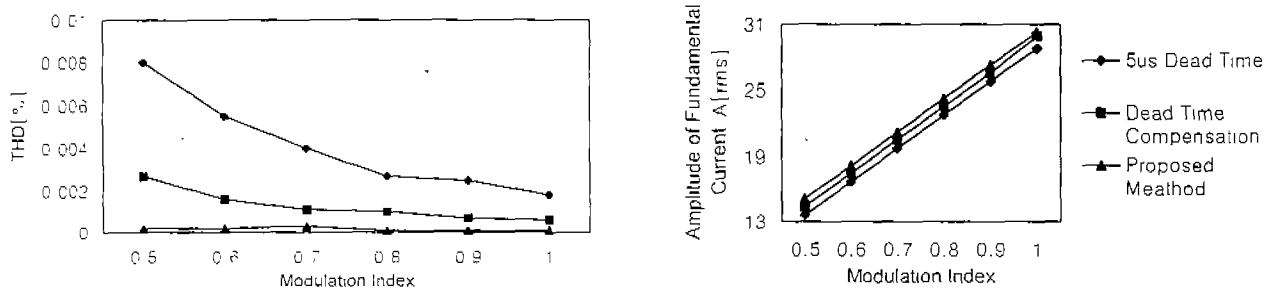
Fig. 7 Software flowchart of the method as shown in Fig. 5

The simulation is done with that Y-connected R-L passive component load as R is 4Ω and L is 10mH. And the carrier frequency of the inverter is 5kHz with DC link voltage as 314V. The inverters with 5μs dead time, with the dead time compensation algorithm[4] and with the proposed algorithm are specified and compared with each other. Fig. 8-(a) shows the results of the inverter with 5μs dead time. Due to the dead time, the waveform of the current is distorted slightly. The harmonic analysis shows that the current contains the 5th, 7th, 11th order harmonics significantly. Fig. 8-(b) also shows the results of the inverter with the dead time compensation algorithm. All the harmonics are reduced and the amplitude of the fundamental current is also increased. The simulation result of the proposed method is shown in Fig-(c). It is evident from the result that the current harmonics are near to zero and the fundamental component of the current is bigger than the previous two results. The result of the variation of the modulation index is shown in Fig. 9. The modulation index is varied from 0.5 to 1. The amplitude of the



(a) the result of the 5μs dead time inverter
(b) the result of the dead time compensation algorithm
(c) the result of the proposed method

Fig. 8. Simulation results comparing the proposed with the conventional methods



(a) Variation of THD (b) Variation of the fundamental current

Fig. 9. Simulation result with variation of the modulation index from 05. to 1

current and the distortion factor are shown (a) and (b), respectively. From simulation results, the inverters with the dead time and 5μs dead time compensation have gradually small harmonics when the modulation index is increased. The reason is that the fundamental amplitude of the current is relatively bigger than the sum of the harmonic generation. But the proposed algorithm maintains the distortion factor near to zero. By inspecting the amplitude of the fundamental current, we know the proposed algorithm can effectively use the modulation index of its maximum.

5. THE EXPERIMENTAL RESULTS

The proposed algorithm can be consisted of the H/W and S/W. To minimize the calculation time, the proposed algorithm as shown Fig. 4 is implemented with the hardware as shown in Fig. 10. The experiments are done with a Y-connected R-L load (R= 4Ω, L= 9.55mH).

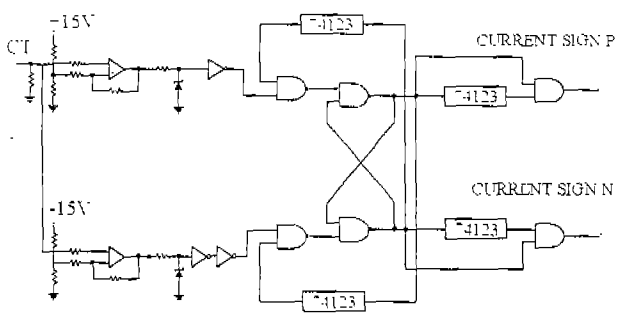


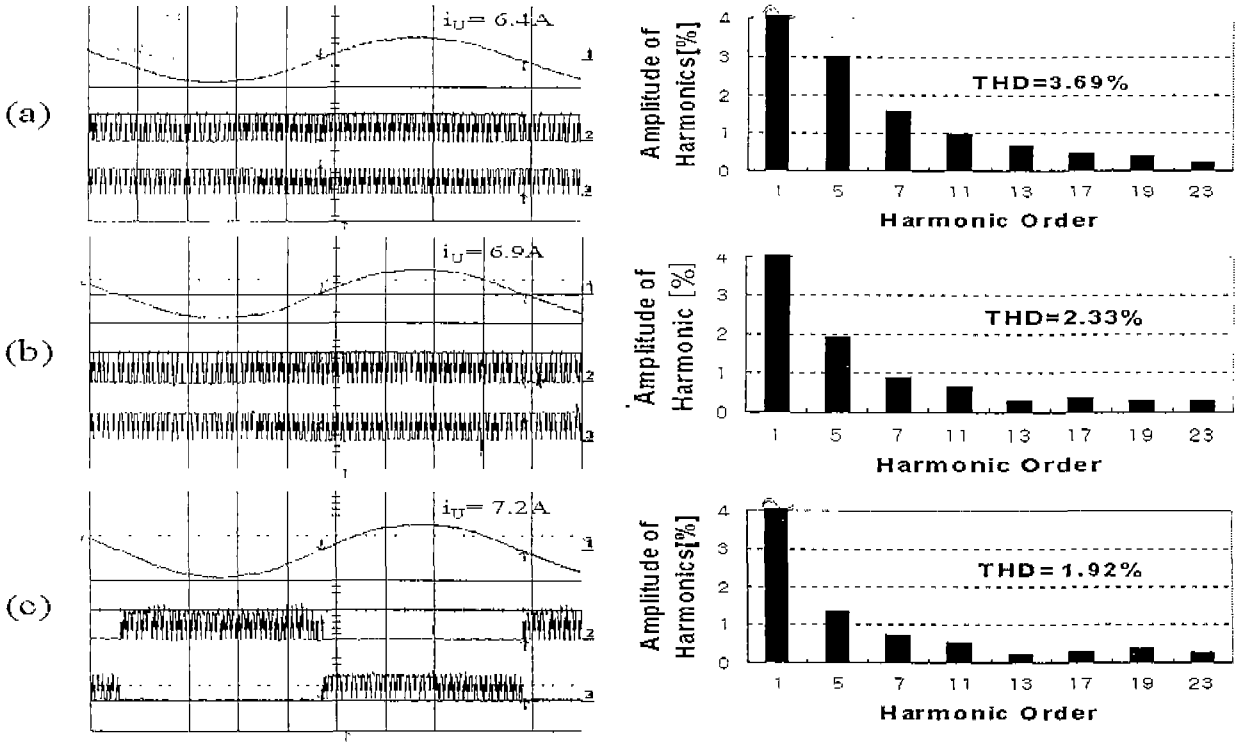
Fig. 10. The determination circuits of the sign of the current

The carrier frequency of the inverter system is 5kHz with DC link voltage as 314V. The PWM generation method is the space vector pulse width modulation (SVPWM). The experiments are done with the aforementioned three inverters as same as the simulations. Fig. 11-(a) shows the experimental result of the inverter with 5μs dead time. There are the output current waveform and the gate drive signals and the result of the harmonic analysis. The current is 6.4A[rms]. Fig. 11-(b) shows the experimental result of the inverter with the dead time compensation[4]. The amplitude of the output current is increased to 6.9A[rms] but the wave shape has a little distortion due to the harmonics. Fig. 11-(c) is the result of the proposed method. The gate drive signal is divided two as described at Fig. 4. Because there is only two dead times during a cycle, the wave shape is improved and the amplitude of the output current is also increased to 7.2A[rms]. The numbers of actually impressed gate drive signals are decreased to a half comparing with (a) and (b).

5. CONCLUSIONS

The dead time minimization algorithm is proposed from the observation that a switch of an inverter leg should not turn-on even if the gate drive signal is impressed. The S/W and the H/W approaches are suggested and the validity of the proposed algorithm is verified by the experimental results. The advantages of the proposed method are summarized as follows

1) The proposed algorithm can be used to both the converter and the inverter systems



(a) current waveform and gate drive signals and its harmonic analysis with 5μs dead time
(b) current waveform and gate drive signals and its harmonic analysis with dead time compensation
(c) current waveform and gate drive signals and its harmonic analysis with the proposed method
Fig. 11 Experiment results comparing the proposed method with the conventional methods

that composed with self-commutation device. And it can be used with all the conventional PWM techniques.

2) The utilization of the modulation index can be increased to almost 1 because there is nearly no dead times.
3) Because the proposed method can use the time corresponding to the dead time, it is adequate for a high frequency switching. So the current ripple can also be reduced.
4) It is no need to adopt any dead time compensation algorithm.
5) Because the actual switching times are reduced to a half, it also save the power of the gate drive sources.
6) The S/W and H/W implementation of this method is very simple.

Especially for the GTO inverters, it is hopeful because the GTO devices consume the large power. And because the turn-on and the turn-off delay times is relatively longer than other devices, the effects of the proposed method should be increased in the GTO inverters.

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6. REFERENCES

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