Digital-To-Phase-Shift PWM Circuit for Full Digital Controlled FB DC/DC Converter

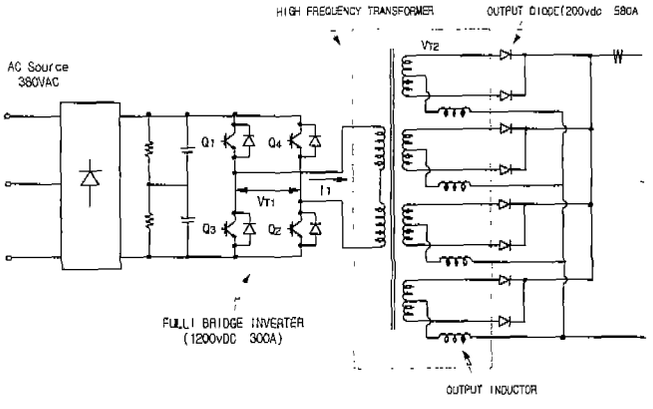
Eun-Soo Kim, Hae-Young Choi, Soon-Gu Park, Tae-Jin Kim
P.E Division, Korea Electrotechnology Research Institute,
Sungju dong 28-1, Chang Won, Kyung Nam, 641-120,
Korea Tel: 82-551-280-1413, FAX: 82-551-280-1406,
E-mail:eskim317@keri.re.kr

Yoon-Ho Kim, Jae-Hak Lee
Dept. of Electrical Engineering, Chung-Ang University
221, Huksuk-Dong, Dongjak-Ku,
Seoul, 156-756, South Korea
Tel:+82-2-820-5290, F AX: +82-2-812-1407

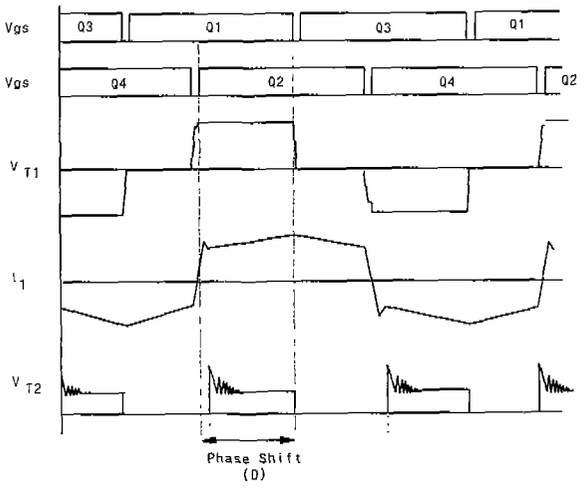
Abstract - With the advent of the high-speed microprocessor and DSP, the possibility of executing a control strategy in digital domain has become a reality. By the use of the DSP and microprocessor controller, many high power converters such as especially inverter and motor drive system may be enhanced resulting in the improved robustness to EMI, the ability to communicate the operating conditions and the ease of adjusting the control parameters. But, the digital controller using DSP or microprocessor is not applied in the high frequency switching power supplies, especially full bridge dc/dc converter. So, this paper presents the method and realization of designing a digital-to-phase shift PWM circuit for full digital controlled phase-shifted full bridge dc/dc converter with zero voltage switching. The operating principles, simulation and experimental results will be presented.

1. Introduction

Fig. 1 shows the basic topology of the ZVS FB dc/dc converter. IGBT pairs Q_1,Q_2 and Q_3,Q_4 are each operated at a fixed frequency with a 50% duty ratio. By controlling the phase shift between the pairs, a quasi-square wave PWM voltage waveform(V_{T1}) will be produced between each legs as shown in Fig. 1. By introducing a suitable delay between the turn-off and turn-on in a pair, this topology permits all switching devices to operate under zero-voltage-switching (ZVS) by using the circuit parasitic such as transformer leakage inductance and power device junction capacitance. Conventionally, full bridge dc/dc converters were controlled by monolithic IC UC3879 which is included the functions of oscillator, error amplifier and phase-shift Circuit



(a) Full bridge DC/DC converter

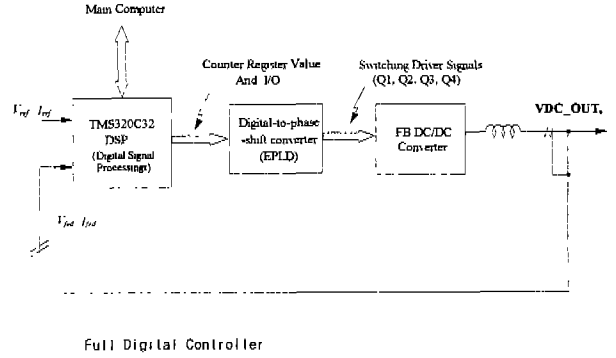


(b) Operating waveforms

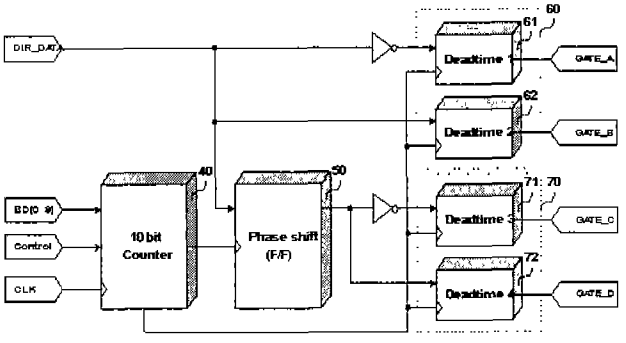
Fig. 1 FB dc/dc converter and its waveforms

Also, microprocessor and DSP have been widely used for the remote control and the LCD driver in the rectifier or FB dc/dc converter. However, the conventional microprocessor controlled FB dc/dc converter is complex and difficult to control because the controller consists of analog and digital parts. Also, the requirement for the output of digital controllers is an analog signal, usually held at a constant value for a complete sampling period. In the case of the control of FB dc/dc converter, the output is required of driving a direct signal to the switch drive circuits by the digital controller. In this paper, the digital-to-phase-shift circuit controlled by DSP(TMX320C32) and microprocessor(80196KC) is proposed for full bridge dc/dc converter. This converter is designed as low-voltage high-current power supply for an electroplating, providing a high current of 3,000A at the maximum power level of 45kW.

2. Digital to Phase-Shift Circuit for PS FB DC/DC Converter



(a) Full digital controlled FB dc/dc converter using DSP or u-processor



(b) digital-to-phase-shift circuit

Fig. 2 Control scheme of FB dc/dc converter

Referring to Fig. 1, 2, it can be seen that for the case of the FB dc/dc converter, the controller must produce two 50% duty ratio square waves at the primary switching frequency. The duty ratio of the converter equals to the phase-shift between these two signals; a duty ratio of zero is a phase-shift of 0°, a duty ratio of 0.5 is a phase-shift of 90° and a duty ratio of 1.0 is a phase-shift of 180°. Since the output of the DSP will be a digital number representing the duty ratio, some form of digital-to-phase-shift converter is required to produce the FB dc/dc converter drive signals. Fig. 2 shows the implementation of this.

2.1 Digital-To-Phase Shift PWM Circuit 1 Using DSP

Digital-to-phase shift generation circuit (figure 3) by using EPLD in the DSP controller is described as follows. First, DSP controller generates a periodic constant pulse(DIR-DATA) which has a half of sampling period due to the timer interruptΦ (TIMTΦ). The constant pulse (DIR-DATA) is divided into the positive and negative signal pulse, and theses signals are transmitted to the counter1, 2. Output signals of counter1, 2 are connected to GATE_A(Q_1) and GATE_B(Q_3). Therefore, two switches (Q_1, Q_3) of the left leg in the full bridge dc/dc converter can be controlled. At the same time, the data calculated by DSP controller is latched at 10bit counter and the 10bit counter starts count down the latched value, and then the phase-shifted 10bit counter output signal is entered into the D flip-flop CLK input pin. D flip-flop according to input control signal(DIR-DATA) generates output signal(CGA). Output signal(CGA) of D flip-flop is also divided into the positive and negative signal pulse and these signal are transmitted to the counter3, 4. Output of counter3, 4 are connected in the GATE_C(Q_2) and GATE_D(Q_4). Therefore, two switches (Q_2, Q_4) of the right leg in the full bridge dc/dc converter can be controlled. More detail operating description can be described as follows. Full bridge dc/dc converter's output voltage and current are converted to digital value by A/D converter (MAX 120) and the proper signal value to regulate the output voltage or current is calculated by DSP controller. The 10bit value calculated by DSP controller is latched at the 10bit counter composed of 8bit counter(41) and 2bit counter(42).

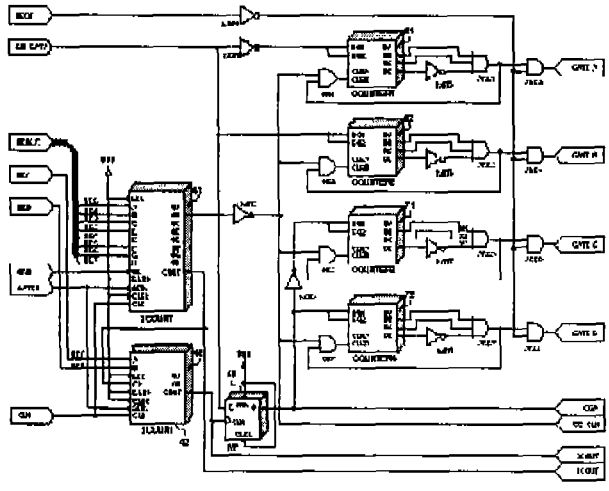
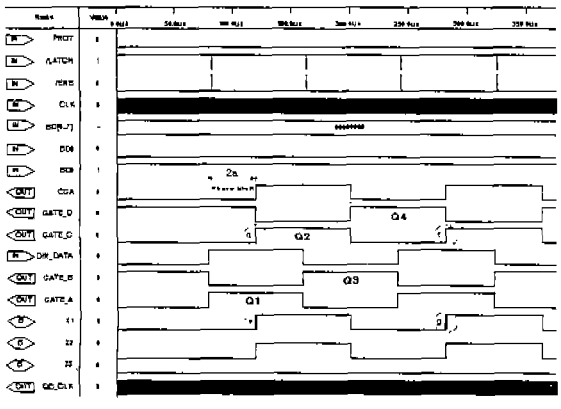
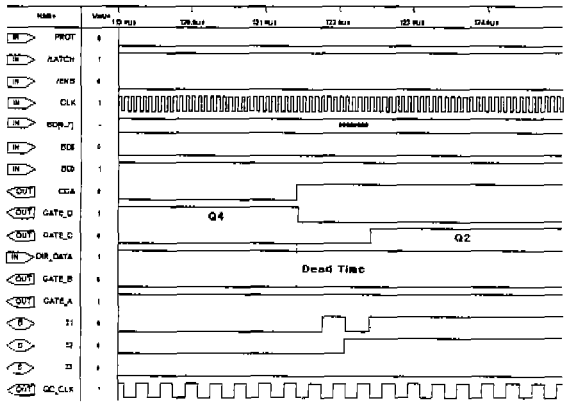


Fig. 3 Digital-to-phase-shift circuit in the DSP controller



(a) Simulation waveforms of the digital-to-phase shift circuit 1



(b) Simulation waveforms of the digital-to-phase shift circuit 1

Fig. 4 (a) Simulation waveforms of the digital-to-phase shift circuit 1 using DSP controller

GN(Gate enable) signal of 8bit counter and 2bit counter is high, and when GN signal of 8bit counter is changed from high to low, 8bit counter starts count down. When QH ~ QA of 8bit counter are all 'L', output signal(COUT) of 8bit counter becomes from 'L' to 'H'. At the next rising edge of a clock, the output signal(COUT) of 8bit counter becomes 'L'. Therefore, output signal(COUT) of 8bit counter has one period pulse width of CLK. When output signal(COUT) of 8bit counter(41) becomes 'H', also input pin(CIN) of 2bit counter(42) which connected COUT pin of 8bit counter(41) becomes 'H' . 2bit counter starts count down at the next rising edge of a clock. If output QB, QA of 2bit counter(42) is 'L', output signal(COUT) of 2bit counter(42) becomes 'H' and becomes 'L' at the next rising edge of a clock. Output signal(COUT) of 2bit counter(42) is transmitted to the input clock signal of D flip-flop(60: figure 3). When output signal(COUT) of 2bit counter(42) become 'H', output Q(CGA) of D flip-flop(60) is generated according to input pulse signal(DIR_DATA) on input pin(D) of D flip-flop. Therefore, the output (CGA) of D flip-flop is phase-shifted as amount of data value latched from 10bit counter(40) compared to the input pulse(DIR_DATE) and is divided into the positive and negative pulse signal. The divided pulse signals are transmitted to the counter3, 4, and the counter3, 4 produce the gate signal of switching devices (GATE_C, GATE_D) which included the dead time. So, gate signal(GATE_C, GATE_D) control two switch(Q_2, Q_4)of the right leg in the full bridge dc/dc converter. Figure 4(a), (b) show simulation waveforms of the input and output signal of digital-to-phase-shift circuit. Sign 2a as shown in Fig. 4(a) is the phase-shifted delay time between GATE_A(Q_1) and GATE_C(Q_2). Sign e is a part of dead time set by QB(X_1) and QC(X_2) of counter 3 and sign d describes the gate control signal(GATE_C) included dead time set by sign e.

2.2 Digital-To-Phase Shift PWM Circuit 2 Using the Low Cost Micro-processor

The use of DSP controller rather than analog controller in the phase-shifted full bridge dc/dc converter has the several benefits such as the inherent advantages of the improved robustness to EMI, the ability to communicate the operating conditions and the ease of adjusting the

control parameters. Also, DSP controller has characteristics of the very fast operating speed and the floating-point computation. But, for a phase-shift control, DSP controller requires the 10bit down counter to transform from digital value calculated by DSP to the phase-shifted signal and extra A/D converter to sense external signal of voltage or current. Therefore, for the reduce of the cost and the ease of utilizing, 80196 micro-processor(or TMS320C24X series processor) included 10bit A/D converter and 8 bit counter internally can be used. PWM output signals of 80196KC generate PWM with two selectable mode - one period per 256 state time(25.6μs at 20MHz) or per 512 state time(51.2μs at 20MHz) which cab be selected by the pre-scale bit of IOC 2.2

PWM-period = 512/system clock frequency
PWM-high=(PWM-control-register*2)/system clock frequency

As mentioned above, switching frequency of the phase-shifted full bridge dc/dc converter can be controlled by using the internal clock(CLK) and PWM-period register of 80196KC. 80196KC has three PWM output pin(PWM 0, PWM 1, PWM 2) and in digital-to-phase shift circuit, we used two PWM pin(PWM 1, PWM 2). All of PWM output in 80196KC use the same counter and rise to 'H' synchronously at the start point. Also, PWM output signal becomes 'H' to the amount of data value determined by the PWM control register, and if the PWM control register value coincide with 8bit counter value, PWM output signal becomes 'L'. PWM1 pin with the constant pulse width controls two switch (Gate_A : Q_1, Gate_B : Q_3) of the left leg and PWM 2 pin with the phase-shifted output signal compared to the PWM 1 output signal controls two switch (Gate_C : Q_2, Gate_D : Q_4) of the right leg in the full bridge dc/dc converter.

As shown in Fig. 5, PWM1 output with the constant duty cycle by writing 8bit value to PWM1-control register is connected in the clock input of D flip-flop and the output Q(DQ_1) of D flip-flop is divided to the half of PWM1 frequency by the rising edge of the PWM1 output signal.

Output(DQ_1) of D flip-flop is divided positive and negative signal and is connected in the input pin A of the shift registers(Shift-REG1, 2) to have dead time. Then, outputs of shift register(shift REG) control two switch(Gate_A : Q_1, Gate_B : Q_3) of the left leg in the full bridge dc/dc converter. Simultaneously, 80196KC senses the output voltage and current of the dc/dc converter by the internal A/D converter and calculate the proper 8bit value to regulate output voltage or current, and then write the calculated 8bit value to PWM2 control register to get the phase-shifted duty cycle output. The output of PWM2 is inverted and is transmitted to the clock input of D flip-flop. Output(DQ_2)of D flip-flop according to D input condition(upper flip-flop output signal : DQ_1) of D flip-flop is divided by the rising edge of the phase shifted signal as duty width as the inverted PWM2.(PWM2 output has 255 resolution and controls output voltage or current due to the phase shifted control) The divided signal in two are divided positive and negative signal pulse and connected in the shift registers(Shift-REG3, 4) to have dead time. Then, outputs of shift register (shift REG) control two switching devices (Gate_C: Q_2, Gate_D: Q_4) of the right leg in the full bridge dc/dc converter.

Figure 6(a), (b) show the simulation waveform of digital-to-phase shift pulse generation circuit.

Sign a of figure 6(a) is phase shifted signal and figure 6(b) describes dead time set by output QC of shift register(shift REG)

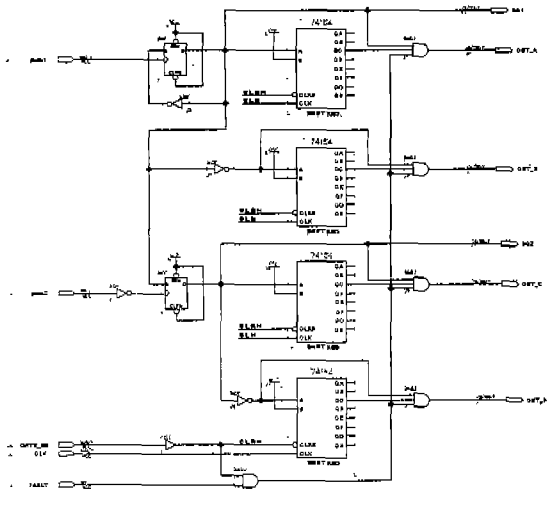
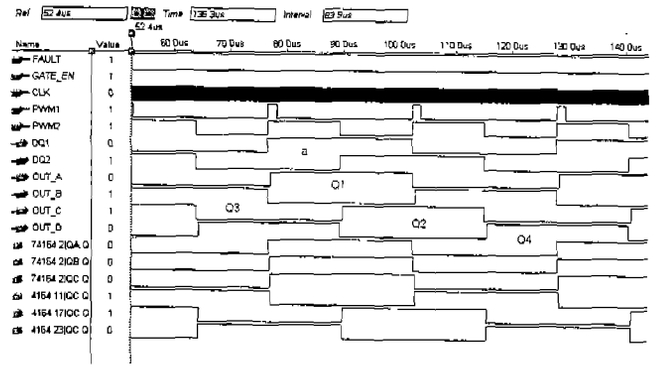
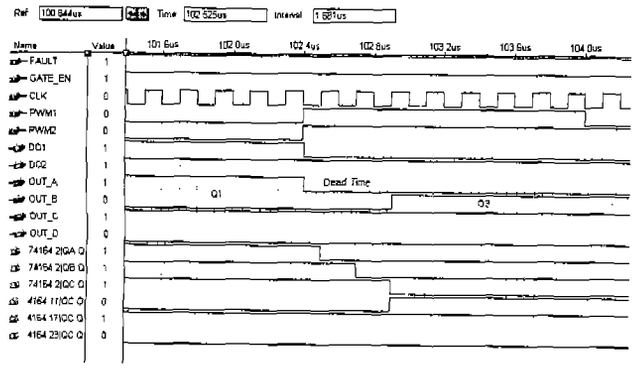


Fig. 5 Digital-to-phase-shift circuit in microprocessor controller



(a) Simulation waveforms of the digital-to-phase shift circuit 2



(b) Simulation waveforms of the digital-to-phase shift circuit 2

Fig. 6 Simulation waveforms of the digital-to-phase shift circuit 2 using microprocessor controller

3. Experimental Result

An experimental prototype of the full bridge dc/dc converter using the digital-to-phase-shift circuit in DSP controller was designed for the following specifications.

* Input voltage: 540VDC,
* Output power: 45kW(15VDC, 3000A)
* Switching frequency: 20kHz
* Switching device: IGBT, 300A, 1200V(IGBT Driver EXB841)
* Output diode: 200V, 580A

Fig. 7 shows the experimental waveforms of the IGBT gate signal using digital-to-phase shift circuit 1 of DSP controller. Dead time of the IGBT gate signal is determined by the output pin(Q_H ~ Q_A) of 8bit counter and dead time set circuit(60) in Fig 3. As shown in Fig. 7, although the dead time in the digital-to-phase shift circuit 1 is set(1.02us), IGBT gate signals are delayed because of the rising/falling time and input capacitance of IGBT.

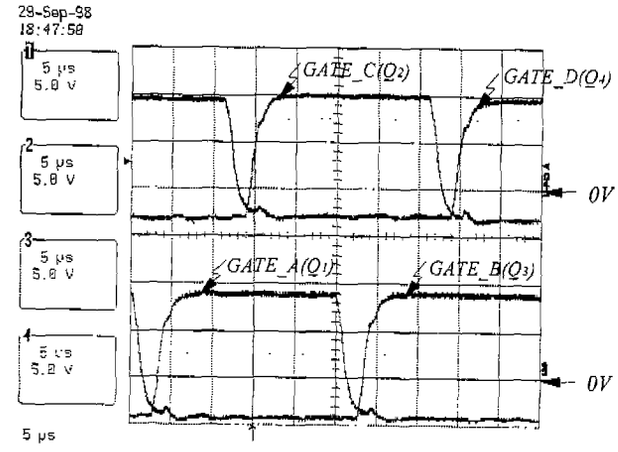


Fig. 7 Experimental waveforms of IGBT driver using digital-to-phase shift circuit 1

4. Conclusion

In this paper, digital-to-phase shift PWM circuits for phase-shift full bridge dc/dc converter in the switching power supply have been suggested, and verified by simulation and experiment.

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