Power Factor Correction of the Single-Stage AC/DC Converter with Low Conduction Loss and High Efficiency

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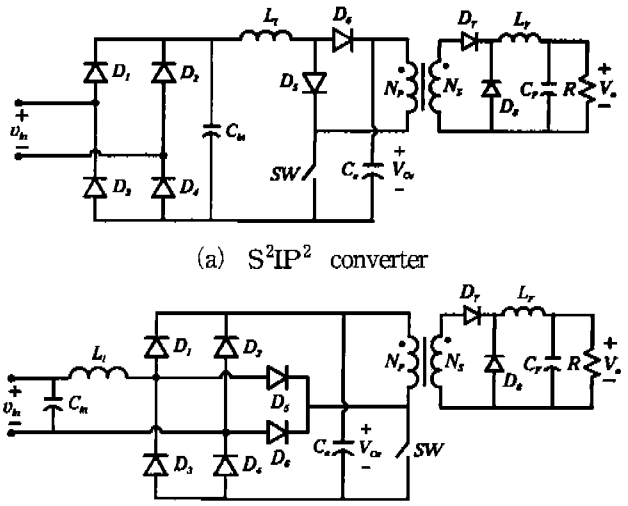
Abstract- This paper proposes a new single-stage, single-switch AC/DC converter based on the boost power factor correction (PFC) cell. The converter offers both high power factor and high efficiency. To reduce the dc voltage on the energy storage capacitor, the dc bus voltage feedback method was used. A 100W (5V/20A) prototype was built and tested to show the validity of the proposed converter.

1. INTRODUCTION

Since several requirements of harmonic standards such as IEC 1000-3-2 and IEEE 519 have been effective, PFC techniques have been attaining an increasing attention. The most common approach to meet power quality requirements is based on a two-stage approach. In the two-stage approach, a non-isolated PFC pre-regulator, which creates an inter- mediate dc bus with a relatively large second-harmonic ripple, is combined with a dc/dc converter that provides an isolation and a high-bandwidth voltage regulation. Although this approach offers both good power factor correction and fast output regulation, it has a poor conversion efficiency due to the two-stage power processing and a high cost due to high component counts and complexity. Accordingly, the two-stage approach is not desirable for low power applications.

Recently, many single-stage approaches were suggested to keep the size and cost within acceptable limits, and designers have attempted to integrate the function of power factor correction and isolated dc/dc conversion into a single power stage[2]-[5]. In the single-stage approach, PFC, isolation, and high-bandwidth control are performed in a single step. Generally, these converters use an internal energy storage capacitor to handle the difference between the varying instantaneous input power and a constant output power.

Figure 1(a) shows the single-stage isolated power factor corrected power supply (S^2IP^2) topology based on the boost PFC cell[3]. Figure 1(b) shows the proposed single-stage isolated power factor corrected power supply. The proposed converter reduces diode conduction loss by minimizing the number of the diodes in the conduction path[2].



(a) S^2IP^2 converter

(b) Proposed converter

Fig. 1 S^2IP^2 converter and proposed converter.

The input inductor, L_i, in the PFC stage of the most converters operates in DCM, so low input-current harmonic distortions are achieved by the inherent property of the DCM boost converter. The output filter inductor, L_F, could operate either in CCM or in DCM. If L_F operates in CCM, the magnitude of the energy storage capacitor voltage, V_{Ce}, strongly depends on the line voltage and output power. For universal line-voltage, ranging from 90 Vac to 265 Vac, V_{Ce} can exceed 1000 Vdc at high line voltage and light load with L_F in CCM[5].

To reduce the energy storage capacitor voltage, a few methods were proposed. First, the variable-frequency control substantially reduces the voltage V_{Ce}[5]. However, since the method needs a wide range of switching frequency, it reduces the efficiency and makes filter designs difficult. Secondly, if L_F is designed to be operated in DCM, V_{Ce} is independent of the load current, and depends only on the ratio of two inductances, L_i / L_F[3]. However, this method is not desirable due to much higher current stresses on semiconductor components compared with the CCM operation. Finally, the dc bus voltage feedback methods with additional windings on the transformer can

further reduce the dc voltage on the energy storage capacitor[6]-[8]. In addition, due to the magnetic coupling of windings, N_1 and N_S or N_2 and N_R, during the on/off time, a part of the input energy is directly transferred to the output. These methods seem particularly attractive since the dc voltage can be reduced effectively, while low input-current harmonic distortions and high efficiency can be achieved.

Figure 2 shows the converter with two additional windings, N_1 and N_2, for the dc bus voltage feedback.

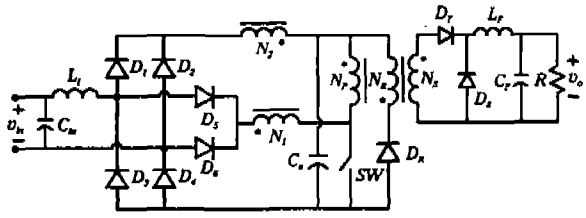


Fig. 2 Proposed converter with dc bus voltage feedback.

2. PRINCIPLES OF OPERATION

A. The proposed converter without dc bus voltage feedback

The operational modes of the proposed topology consist of six modes. The three modes shown in Fig. 3 occur during a switching cycle when the line voltage is positive, and other three modes occur when the line voltage is negative. The operational principles of the latter three modes are identical to those of the former three modes.

Mode 1

When the line voltage is positive and the switch is on, the input inductor is charged by the line voltage through diode D_5 and the energy stored in the capacitor is transferred to the filter inductor of the dc/dc converter through the transformer.

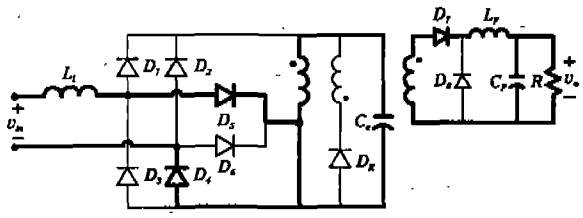
Mode 2

When the line voltage is positive and the switch is off, the energy stored in the input inductor and the reset winding is transferred to the energy storage capacitor through D_1 and D_R, respectively. During this mode, the secondary voltage of the transformer is negative, and the energy stored in the filter inductor is transferred to the output capacitor and load.

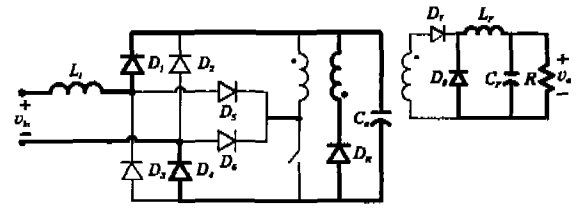
Mode 3

When the energy stored in the input inductor is transferred completely, the input inductor current falls to zero. The filter inductor current continues to flow to the output.

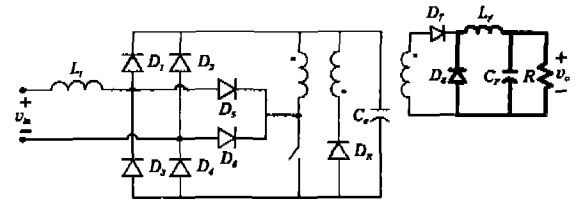
The inductance of the input inductor, L_i, is small so as to operate in DCM, while the inductance of the filter inductor is large enough to operate in CCM. Figure 4 shows the input inductor currrent in DCM for half the



(a) Mode 1. $v_{in} > 0$, SW : on



(b) Mode 2. $v_{in} > 0$, SW : off, $i_{Li} \neq 0$



(c) Mode 3. $v_{in} > 0$, SW : off, $i_{Li} = 0$

Fig. 3 Topological stages of the proposed converter.

period of line cycle. Around the peak of the input voltage, the converter operates at the boundary of the CCM and DCM. In the figure, the on-time, T_{on}, is almost constant over the line period.

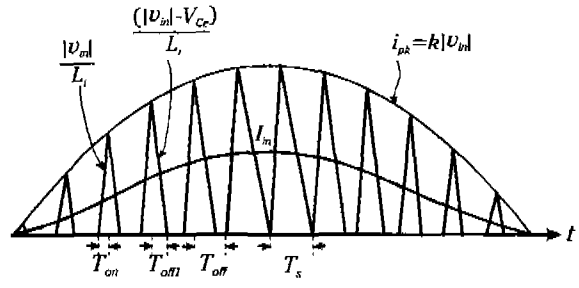


Fig. 4 Input inductor current waveform.

Assuming sinusoidal input voltage $v_{in} = V_m \sin \omega t$, the peak input inductor current, i_{pk}, is determined as:

$$i_{pk} = \frac{|v_{in}| \cdot T_{on}}{L_i} = \frac{V_m \cdot D \cdot T_s}{L_i} |\sin \omega t| \qquad (1)$$

where V_m is the amplitude of the input voltage, T_s is the period of a switching cycle, and the duty cycle, D, is obtained from the flux balance condition of L_F as:

$$D = \frac{N_P}{N_s} \cdot \frac{V_o}{V_{Ce}} \qquad (2)$$

where V_o is the output voltage, N_P is the number of turns of the primary winding, and N_S is that of the

secondary winding.

The discharging time of the input inductor current, T_{off1}, is given by:

$$T_{off1} = \frac{i_{pk}}{(V_{Ce} - |v_{in}|)/L_i} = \frac{|v_{in}| \cdot T_{on}}{V_{Ce} - |v_{in}|} . \quad (3)$$

Due to the presence of the input filter capacitor, C_{in}, an average input inductor current, I_{in}, is given by:

$$I_{in} = I_{on(ave)} + I_{off1(ave)}$$

$$= \frac{|v_{in}| \cdot D^2 \cdot T_s}{2L_i} + \frac{|v_{in}|^2 \cdot D^2 \cdot T_s}{2L_i(V_{Ce} - |v_{in}|)} \quad (4)$$

$$= \frac{D^2 \cdot T_s \cdot V_{Ce}}{2L_i} \cdot \left(\frac{\alpha \cdot \sin\omega t}{1 - \alpha \cdot \sin\omega t}\right)$$

where $\alpha = V_m / V_{Ce}$, I_{in} is the line current, $I_{on(ave)}$ is the average of the input inductor current during on-time, and $I_{off1(ave)}$ is the average of the input inductor current during discharging time.

B. The proposed converter with dc bus voltage feedback

Figure 5 shows the topological stages of the converter during a switching cycle, and Fig. 6 shows its key waveforms.

Mode 1

During the on-time, with winding N_1, the induced voltage across N_1 opposes the rectified input voltage $|v_{in}|$. As a result, to keep the same volt-second product across L_i, a larger duty cycle is necessary. With a larger duty cycle, although the load current reduces, voltage V_{Ce} will not be increased but maintained within an acceptable limit. In addition, through the magnetic coupling of windings N_1 and N_S, the energy stored in N_1 is directly transferred to the output. Other principles of operation are the same as those of the converter without dc bus voltage feedback.

The rising slope of the inductor current, di_{Li}/dt, is given by:

$$\frac{di_{Li}}{dt} = \frac{|v_{in}| - \frac{N_1}{N_P} V_{Ce}}{L_i} \quad (5)$$

where i_{Li} is the inductor current.

The switch current, i_{SW}, is given by:

$$i_{SW} = i_{Li} + i_P + i_M \quad (6)$$

where i_P is the filter inductor current referred to the primary winding and i_M is the magnetizing current.

Mode 2

When the switch SW is turned off, the voltage across L_i, v_{Li}, is given by:

$$v_{Li} = |v_{in}| - (1 + \frac{N_2}{N_R}) V_{Ce} . \quad (7)$$

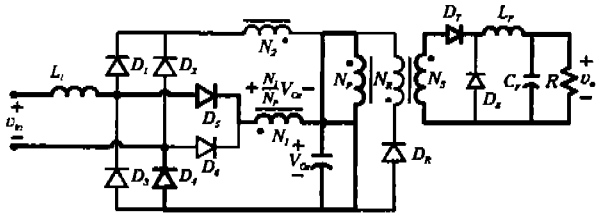
Accordingly, the required reset voltage for L_i can be obtained with a smaller V_{Ce} because of the induced voltage $(N_2/N_R)V_{Ce}$ across winding N_2. When the energy stored in L_i is discharged to C_e, in addition to direct path through diodes, an indirect path through the magnetic coupling of windings N_2 and N_R exists. Other principles of operation are the same as those of the converter without dc bus voltage feedback.

The falling slope of the inductor current, di_{Li}/dt, is given by

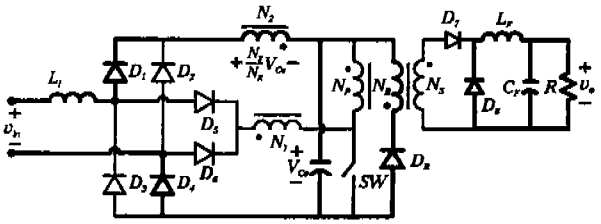
$$\frac{di_{Li}}{dt} = \frac{|v_{in}| - (1 + \frac{N_2}{N_R}) \cdot V_{Ce}}{L_i} . \quad (8)$$

Mode 3

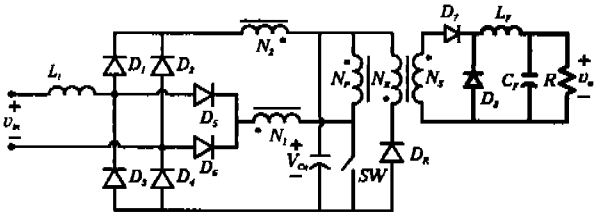
When the energy stored in the transformer is reset completely, the voltage across the transformer falls to zero.



(a) Mode 1. $v_{in} > 0$, SW : on



(b) Mode 2. $v_{in} > 0$, SW : off



(c) Mode 3. $v_{in} > 0$, SW : off

Fig. 5 Topological stages of the proposed converter.

Figure 7 shows the line voltage and current waveforms. As shown in the figure, the input current cannot flow until the line voltage exceeds the induced voltage across N_1, $(N_1 / N_P)V_{Ce}$. Therefore, a larger ratio N_1 / N_P increases input-current harmonic distortions due to a larger dead angle, while it reduces the energy storage capacitor voltage. The dead angle, θ, is given by:

$$\theta = \sin^{-1}\left(\frac{N_1}{N_P} \cdot \frac{V_{Ce}}{V_m}\right) . \quad (9)$$

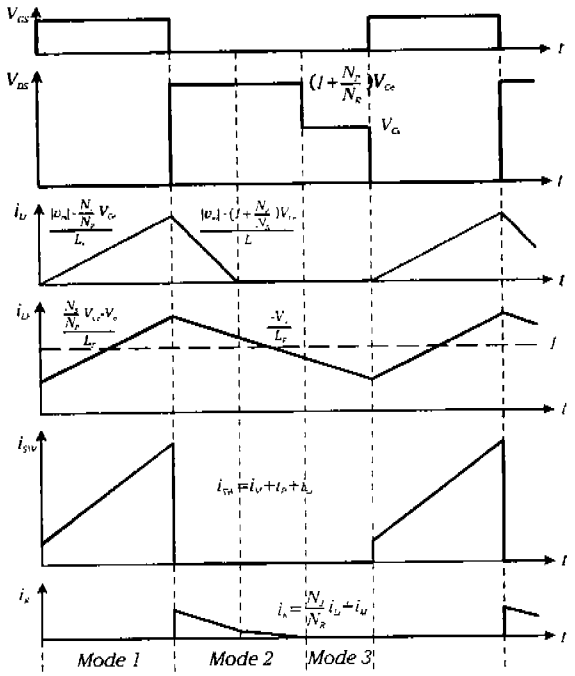


Fig. 6 Key waveforms of the proposed converter.

The average input inductor current, I_{in}, is determined as:

$$I_{in} = \frac{D + D_{off1}}{2} \cdot i_{pk} \tag{10}$$

where the peak inductor current, i_{pk}, is given by:

$$i_{pk} = \frac{|v_{in}| - \frac{N_1}{N_P} V_{Ce}}{L_i} \cdot DT_s \tag{11}$$

and the discharging duty ratio of the input inductor current, D_{off1}, is given by:

$$D_{off1} = \frac{|v_{in}| - \frac{N_1}{N_P} V_{Ce}}{(1 + \frac{N_2}{N_R}) V_{Ce} - |v_{in}|} \cdot D. \tag{12}$$

By combining the flux balance condition of the input inductor with equations (10) and (11), it can be shown:

$$I_{in} = \frac{V_{Ce} D^2 T_s}{2L_i} \frac{(1 - \frac{N_1}{N_P} + \frac{N_2}{N_R})(-\frac{N_1}{N_P} + \frac{|v_{in}|}{V_{Ce}})}{1 + \frac{N_2}{N_R} - \frac{|v_{in}|}{V_{Ce}}} . \tag{13}$$

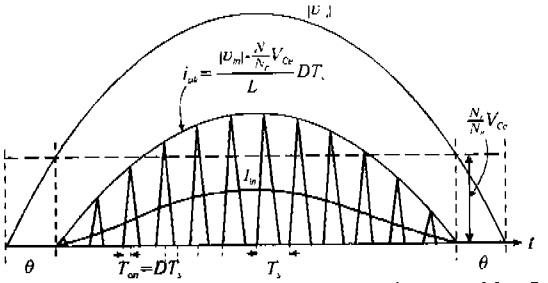


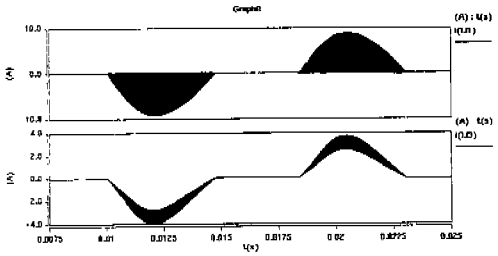
Fig. 7 Line voltage and current waveforms with L_i operating in DCM.

The ripple of the filter inductor current is determined as:

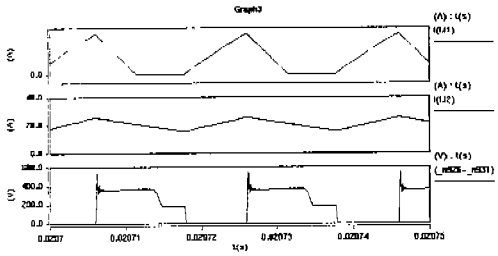
$$\Delta i_{LF} = \frac{V_o \cdot (1-D) T_s}{L_F} . \tag{14}$$

In designing the filter inductor, the inductance value can be designed to place i_{LF} at the boundary of the CCM and DCM when the load current is reduced to low power level. This design can further reduce the voltage on the energy storage capacitor below an acceptable limit even at very low power levels.

3. SIMULATION and EXPERIMENTAL RESULTS

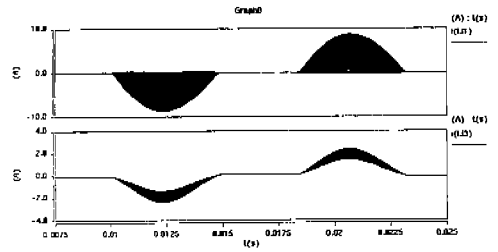


(a) Input inductor current and line current

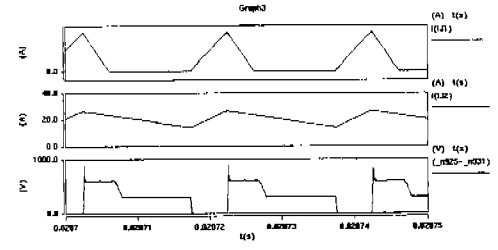


(b) Input inductor current, output filter inductor current, and switch voltage

Fig. 8 Simulation results of the converter (120Vac).



(a) Input inductor current and line current



(b) Input inductor current, output filter inductor current, and switch voltage

Fig. 9 Simulaion results of the converter (200Vac).

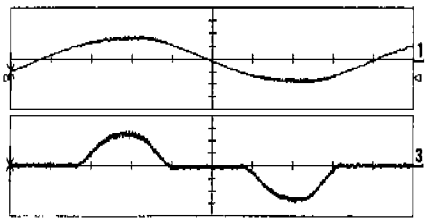
In order to verify the operation and performance of the proposed converter with dc bus voltage feedback, computer simulations were performed. Figures 8 and 9 show the simulation results of the converter at different input voltage levels.

A 100W (5V/20A) prototype with dc bus voltage feedback has been built and tested. The components shown in Table I were used for the implemention of the circuit.

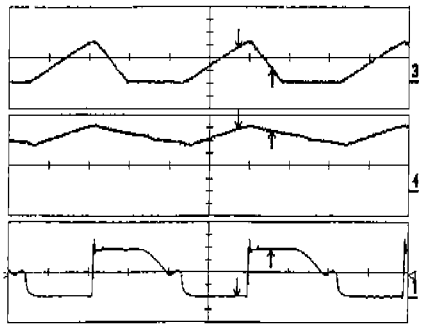
Table I Components for the implementation of the converter

C_{in}	1 μF	L_i	60 μH
D_R	FR305	D_7, D_8	C30PQ60
SW	GT40T101	L_F	8 μH
D_1, D_2, D_5, D_6	HFA30PA60C		
C_e	470 μF/400V×2 (series)		
C_F	2200 μF/50V×3 (parallel)		
TR	PQ50/50 core with N_P=N_R=34 turns, N_1=20 turns, N_2=12 turns, and N_S=3 turns		

Figures 10 and 11 show the waveforms of the converter at different input voltages at full load. Figure 12 shows the waveforms of the converter at one fifth of the full load. As can be seen, the filter inductor current operates at the boundary of the DCM and CCM at this specific power level. Since the filter inductor current operates in DCM at very low power levels, the voltage, V_{Ce}, is kept within an acceptable limit.

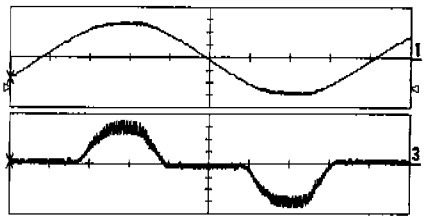


(a) Input line voltage (100V/div.) and current (1A/div.)

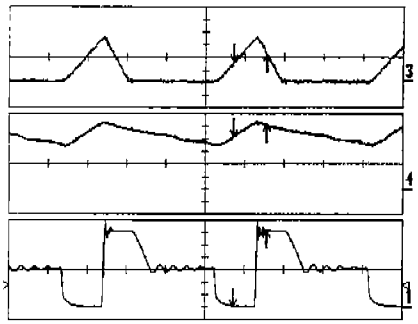


(b) Input inductor current (2A/div.), output filter inductor current (5A/div.), and switch voltage (100V/div.)

Fig. 10 Experimental results of the converter (120Vac, 100W).



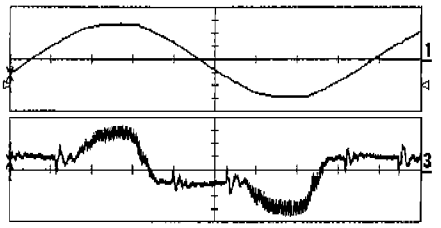
(a) Input line voltage (100V/div.) and current (0.5A/div.)



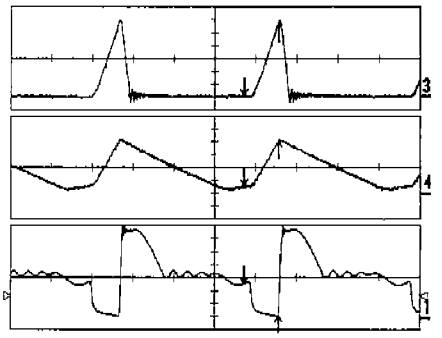
(b) Input inductor current (2A/div.), output filter inductor current (5A/div.), and switch voltage (100V/div.)

Fig. 11 Experimental results of the converter (200Vac, 100W).

In the implementation, general purpose PWM IC controller, UC3825, was used for a fast output-voltage feedback control. The switching frequency was 50 *kHz*.



(a) Input line voltage (100V/div.) and current (0.1A/div.)



(b) Input inductor current (0.5A/div.), output filter inductor current (2A/div.), and switch voltage (100V/div.)

Fig. 12 Experimental results of the converter (200Vac, 20W).

Figures 13 and 14 show the power factor (PF), total harmonic distortions (THD), energy storage capacitor voltage (V_{Ce}), and efficiency(η) measured at each load. Table II summarizes PF, THD, V_{Ce}, and η measured at different input voltages.

As can be seen from the figures and table, even at high input voltage and light load, energy storage capacitor voltage, V_{Ce}, is kept below 450Vdc, while the PF, efficiency, and THD are deteriorated somewhat compared with those of the converter without dc bus voltage feedback. Through measuring the harmonic components of the line current, we could see that the converter with dc bus voltage feedback satisfied the harmonic standard of IEC1000-3-2 class D limit at the input voltage of 240Vac.

Table II Measured results at different input voltages(100W)

$V_{in(rms)}$[V]	PF	THD[%]	V_{Ce}[V]	η[%]
120	0.869	55.1	182	77.8
180	0.867	55.7	274	76.6
240	0.863	55.4	363	74.9

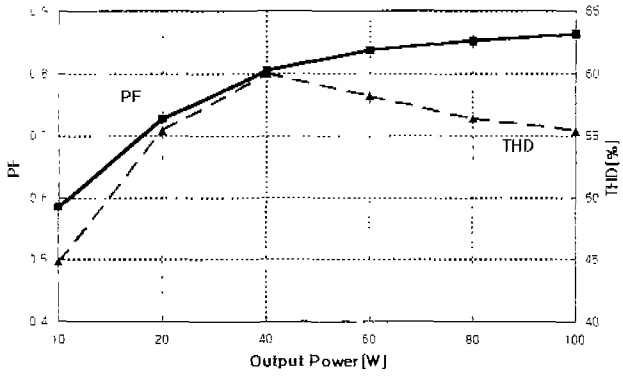


Fig. 13 Power factor (PF) and total harmonic distortions (THD) of the converter at each load (240Vac).

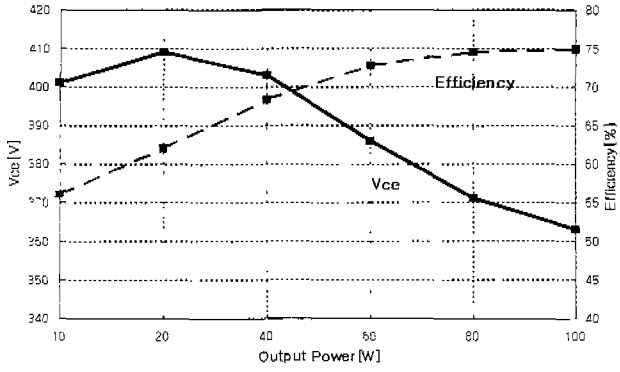


Fig. 14 Energy-storage capacitor voltage (V_{Ce}) and efficiency (η) of the converter at each load (240Vac).

4. CONCLUSIONS

A new single-stage, single-switch AC/DC converter based on the boost PFC cell is proposed. With the dc bus voltage feedback method, the energy storage capacitor voltage was kept below 450Vdc even at very low power (about 10W) with the input voltage of 240Vac. The operational principles of the proposed topology were explained. The simulation was performed with SABER and an experimental 100W prototype has been built and tested in order to verify the operation and performance of the proposed converter. As can be seen from the experimental and simulation results, the proposed converter works well with high PF, low THDs, and high efficiency.

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