An Alternative Zero Voltage Switching Method of Boost Rectifier in Power Factor Correction Rectifier/Regulator System using DC Linked Energy Feedback Circuit

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ABSTRACT - A new single phase power factor correction rectifier/regulator with dc linked energy feedback circuit is proposed, which is capable of achieving the zero voltage switching (ZVS) of a boost rectifier stage without any auxiliary switch. The performance of the proposed rectifier/regulator is demonstrated through a 200 W, 90 kHz prototype. This proposed rectifier/regulator with dc linked energy feedback circuit is particularly suited for distributed power system applications.

I. Introduction

Recently, increasing emphasis on the power quality such as IEC1000-3-2 standards has placed a stronger demand on the performance of ac-dc converters as the front end power processing unit of many electronic systems. The requirements often include the followings:

- unity input displacement factor
- very low total harmonic distortion of the input current
- tight output voltage regulation
- transformer isolation between source and load
- high efficiency and high power density.

These requirements are very crucial to high power applications such as distributed power systems. Several types of single-phase ac-dc converters which satisfy one or more of the above requirements have been proposed. All of them use some form of high-frequency pulse-width-modulation (PWM) controlled switching rectifier in order to minimize the size and weight of reactive filtering components. In this paper, a novel ZVS PWM single-phase ac-dc converter is described. Its performance characteristics are superior to those of the ZVT boost rectifier followed by a ZVS full-bridge dc-dc converter. Moreover, the new converter is capable of implementing a ZVS for the boost rectifier without any auxiliary power switch by using the dc link energy feedback circuit. The presence of a dc link energy feedback circuit has little effects on the steady-state characteristics of the converter. Thus, well known design equations for the boost rectifier and the ZVS half-bridge dc-dc converter [1-2], can be used in designing a single-phase rectifier/regulator system. The basic operational principles of the proposed converter are analyzed and a control strategy is developed. Experimental results are then presented, which illustrate the converter function and verify the operational principles discussed.

II. Principles of operation

Fig.1 shows the circuit diagram of the proposed converter. The converter can be divided into several function blocks. The CCM PWM boost rectifier, composed of an input inductor L_B, an output diode D_B, and a power switch S_B, is used for a power factor correction operation. The unity power factor is obtained by using an average current mode PWM technique[5]. The dc linked energy feedback circuit, composed of a transformer T_r, an inductor L_r, and a diode D_{aux}, is used to allow a ZVS of the switch S_B. With this circuit, a zero current switching (ZCS) of the diode D_B is allowed, which can eliminate the reverse recovery problem of D_B. Two paralleled ZVS half-bridge dc-dc converters are used for the tight output voltage regulation and transformer isolation. The half-bridge converter 1 and 2 are composed of power switches S_{H1}, S_{H2}, S_{H3}, and S_{H4}, center tapped transformers T_{r1} and T_{r2}, output rectifiers D_{H1}, D_{H2}, D_{H3}, and D_{H4}, and output inductors L_{OH1} and L_{OH2}. The output voltage regulation is obtained by using a peak current mode PWM technique. With this technique, two paralleled ZVS half-bridge converters can be operated in parallel while sharing the total load current equally. The dc link capacitors C_{DC1} and C_{DC2} are energy storage capacitors required to store the 120 Hz ripple energy needed in a single-phase power factor correction converter. The output capacitor C_{OH} is a filtering capacitor required to regulate a specific output voltage. The gate to source voltage (V_{gs}) waveforms for all switches in the proposed converter are shown in Fig. 2. As shown in this figure, the gate to source

voltage of S_B is exactly synchronized to that of S_{H3}. On the other hand, the turn-on instant of S_{H1} is slightly ahead of that of S_B with the shifted time of T_D. The gate to source voltages of S_{H2} and S_{H4}, can be obtained using the asymmetrical duty cycle controlled PWM technique[2]. The voltages at node A, V_A and node B, V_B which are the same as the drain to source voltages of S_{H1} and S_{H3}, respectively, are obtained as shown in this figure. Then, the resulting narrow voltage pulses, V_{AB} are used to activate the dc linked energy feedback circuit prior to turning on the boost switch S_B, to allow a ZVS of S_B and a ZCS of D_B. It is noted that the duty cycle of the boost rectifier , D_{TB} and that of the half-bridge converter, D_{THB}, are different since they are obtained from different PWM controllers. This duty cycle variation of the half-bridge converter can cause in different locations for the positive voltage pulses of V_{AB} ($+V_{DC}$), but a same location for the negative voltage pulses of V_{AB} ($-V_{DC}$). It is also noted that the pulse widths of positive pulses and negative pulses of V_{AB} are same since the duty cycles of two paralleled half-bridge converters are same under the current mode control technique. Thus, the transformer T_r does not have any flux imbalance problem.

For the analysis of a circuit operation, the assumptions are made as follows:

- ◆all power semiconductors are ideal with no output capacitance
- ◆circuit operates in a steady state
- ◆ZVS of S_{H1}, S_{H2}, S_{H3}, and S_{H4} are obtained using a asymmetrical duty cycle controlled PWM technique
- ◆turn ratio of T_r, N, is larger than 1
- ◆input inductor L_B is sufficiently large to be approximated by a current source of I_{LB}
- ◆V_{DC} is considered as constant during a switching cycle
- ◆dead times of two half-bridge converters are short enough so that the rise time or fall time of V_{AB} can be neglected.

The last assumption is valid since the dc linked energy feedback circuit is activated only when the negative voltage pulses of V_{AB} reaches $-V_{DC}$ in the proposed converter.

Fig.3 shows the nine topological states and the key waveforms are shown in Fig.4 for the proposed converter in which the duty cycle of a boost rectifier is large enough so that the positive voltage pulses of V_{AB} are created during the on time of S_B. Even when these voltage pulses are created during the off time of SB, the circuit operation is not affected as can be seen in the next. The detailed description of each topological state is given in the following.

Mode 1 (T0 - T1) : Prior to T_0, the switch S_{H2} of the half-bridge converter 1 and the switch S_{H4} of the half-bridge converter 2 are on while the switch S_B of the boost rectifier is off. Therefore, the operation of the boost rectifier is the same as that of the off time mode in a conventional boost converter. Thus, the current flowing through the diode D_B in the boost rectifier is I_{LB} which is the input current of the boost converter . When the switches S_{H1} and S_{H2} of the half-bridge converter 1 are both off, the drain to source voltage of S_{H1}, V_A, rises linearly from zero to V_{DC}, results in a zero voltage across S_{H2}. At T_0, the switch S_{H2} is turned on during the ZVS condition and the primary voltage across T_r in a dc linked energy feedback circuit, V_{AB}, becomes $-V_{DC}$. The current flowing through the magnetizing inductance L_m, i_{mr}, decreases with the slope of $-V_{DC} / L_m$. Since the voltage across the secondary winding in T_r, V_x, is $-NV_{DC}$, the diode D_{aux} is now forward biased. The voltage across L_r is NV_{DC}, so the current flowing through L_r, i_{Lr}, increases linearly from zero with the slope of NV_{DC} / L_r as follows:

$$i_{Lr}(t) = \frac{NV_{DC}}{L_r}(t - T_0). \qquad (1)$$

The current flowing through the primary winding of T_r, i_{pr}, is obtained as

$$i_{pr}(t) = \frac{i_{Lr}}{N} + i_{mr} = I_{mr,pk} - \frac{V_{DC}}{L_m}(t - T_0) - \frac{V_{DC}}{L_r}(t - T_0) \qquad (2)$$

where $I_{mr,pk}$ is the peak value of the magnetizing current i_{mr}. The current flowing through D_B, i_{DB}, decreases as $i_{DB}(t) = I_{LB} - i_{Lr} = I_{LB} - \frac{NV_{DC}}{L_r}(t - T_0)$. (3). At T_1, i_{DB} reaches zero, achieving a ZCS of D_B. The duration of mode 1 can be obtained as $T_{t0-t1} = \frac{L_r I_{LB}}{(NV_{DC})}$. (4).

Mode 2 (T1-T2) : Mode 2 begins when the diode D_B is off during the ZCS condition. Since the switches S_{H1} and S_{H4} are on continuously, V_x remains $-NV_{DC}$ during mode 2. The stored energy in the parasitic capacitance C_r of the switch S_B, is transferred to L_r in a resonant man-

ner. At T_2, the voltage across S_B, v_{SB}, reaches zero, which results in a ZVS condition of the boost rectifier switch S_B. It is noted that, if the turn ratio of T_r, N, is larger than 1, the time required to achieve a ZVS condition of S_B is shorter than one-quarter of the resonant period formed by L_r and C_r, e.g., $\frac{\pi}{2}\sqrt{L_r C_r}$. The duration of mode 2 can be obtained as

Mode 3 (T2-T3) : At T_2, the anti-parallel diode of S_B is on, and the voltage across the secondary winding of T_r, V_x, remains $-NV_{DC}$. Since the voltage across L_r is $(N-1)V_{DC}$, the current flowing through L_r, i_{Lr}, increases linearly. At T_3, when the switches S_{H3} and S_{H4} of the half-bridge converter 2 are both off, the drain to source voltage of S_{H3}, V_B, decreases linearly from V_{DC} to zero. Therefore the switch S_{H3} can be turned on during the ZVS condition. The primary voltage across T_r, V_{AB}, increases from $-V_{DC}$ to zero, and the current flowing through the magnetizing inductance L_m, i_{mr}, decreases to zero at T_3. At the same time, since the gate to source voltage of S_B is exactly synchronized to that of S_{H3}, the boost rectifier switch S_B is turned on during the ZVS condition as is explained in mode 2 operation. To satisfy the ZVS condition of S_B, the following inequality should be satisfied as

$$T_D \geq T_{t0-t1} + T_{t1-t2} = \frac{L_r I_{LB}}{(NV_{DC})} + \frac{\pi}{2}\sqrt{L_r C_r} \qquad (5)$$

where it is assumed that the duration of mode 2, T_{t1-t2}, is one quarter of the resonant period formed by L_r and C_r, which is valid since the actual duration of mode 2 is shorter than $\frac{\pi}{2}\sqrt{L_r C_r}$. As can be seen in inequality (5), the ZVS condition of S_B can be achieved for any load or line voltage condition of the boost rectifier in the proposed converter.

Mode 4 (T3-T4) : Mode 4 begins when the switch S_{H3} of the half-bridge converter 2 and the switch S_B of the boost rectifier are turned on at T_3 during the ZVS condition. Since the voltage across the primary winding of T_r, V_{AB}, is zero, the voltage across the inductor L_r becomes $-V_{DC}$. At T_4, $i_{Lr}(t)$ becomes zero and the diode D_{aux} is off. The current flowing through the switch S_B increases to I_{LB} during mode 4.

Mode 5 (T4 - T5) : Mode 5 begins when the diode D_{aux} is turned off. The switch S_{H1} of the half-bridge converter 1 and the switch S_{H3} of the half-bridge converter 2 are on during mode 5. At the same time, the boost switch S_B is on so that the operation of the boost rectifier becomes the same as that of the on-time mode in a conventional boost converter. The current flowing through the switch S_B in the boost rectifier is I_{LB}. Mode 5 ends when the switch S_{H1} of the half-bridge converter 1 is turned off.

Mode 6 (T5 - T6) : When the switches S_{H1} and S_{H2} of the half-bridge converter 1 are both off, the drain to source voltage of S_{H2}, $V_{DC}-V_A$, decreases from V_{DC} to zero, results in a zero voltage across S_{H2}. At T_5, the switch S_{H2} of the half-bridge converter 1 is turned on during the ZVS condition and the primary voltage across T_r in a dc linked energy feedback circuit, V_{AB}, becomes $+V_{DC}$. The current flowing through the magnetizing inductance L_m, i_{mr}, increases with the slope of V_{DC} / L_m. Since the voltage across the secondary winding in T_r, V_x, is now NV_{DC}, the diode D_{aux} is reverse biased and the current flowing through L_r, i_{Lr}, remains zero. Mode 6 ends when the switch S_{H3} of the half-bridge converter 2 is turned off.

Mode 7 (T6-T7) : When the switches S_{H3} and S_{H4} of the half-bridge converter 2 are both off, the drain to source voltage of S_{H3}, $V_{DC}-V_B$, decreases from V_{DC} to zero, results in a zero voltage across S_{H4}. At T_6, the switch S_{H4} is turned on during the ZVS condition and the primary voltage across T_r in a dc linked energy feedback circuit, V_{AB}, becomes zero. Mode 7 ends when the switch S_B of the boost rectifier is turned off at T_7.

Mode 8 (T7-T8) : Mode 8 begins when the switch S_B is turned off at T_7. The voltage across the switch S_B, v_{SB}, increases from zero as follows:

$$v_{SB}(t) = \frac{I_{LB}}{C_r}(t - T_7). \qquad (6)$$

Since the switches S_{H2} and S_{H4} are both on during mode 8, the primary voltage across T_r, V_{AB}, remains zero. So the current flowing through the magnetizing inductance L_m, i_{mr}, remains $i_{mr,pk}$. At T_8, the voltage across the switch S_B, v_{SB}, reaches V_{DC} and the diode D_B is turned on. The duration of mode 8 can be obtained

as follows: $T_{t7-t8} = \frac{C_r V_{DC}}{I_{LB}}$. (7)

Mode 9 (T8-T9) : At T_8, the diode D_B is turned on. The operation of mode 9 is the same as that of the off-time mode in a conventional boost converter. The switches S_{H2} and S_{H4} of two half-bridge converters remain on state during mode 8. The current flowing through the magnetizing inductance L_m, i_{mr}, remains $i_{mr,pk}$. When the switch S_{H2} of the half-bridge converter 1 is turned off at T_9, another switching cycle starts.

It is noted that the dc linked energy feedback circuit is affected only during mode 1 to mode 3. Hence, the proposed converter is independent of the location of positive pulses $+V_{AB}$, which may vary in accordance with the duty cycle D_H of the half-bridge converters. It is also noted that. in the proposed converter, the leakage inductance of T_r can serve as L_r , so the external inductor can be removed in the dc link feedback circuit.

III. Experimental Results

To experimentally characterize the ZVS technique of the PFC boost rectifier in the proposed rectifier/regulator, a prototype has been constructed using the components listed in Table I as follows:

◆rated output power : 200 W
◆output voltage : $V_o = 50V$
◆input rms line voltage : $\sqrt{2} \times 110V$
◆switching period : $T_s = 11us$.

Fig.7 shows the switch voltage and current waveforms of the boost switch S_B for different duty cycles of the boost rectifier. The turn-on transient waveforms of the switch S_B are shown in Fig.8. It can be seen that the ZVS of the boost switch S_B occurs regardless of the rectified line voltages. Fig.9 shows the current waveforms of D_B for different duty cycles. It is noted that the ZCS of D_B is insured, eliminating the reverse recovery problem of D_B. Fig.10 shows the switch voltage and output inductor current waveforms of the two paralleled half-bridge converters. It is shown that the ZVS of the switch and equal load sharing operation of two paralleled half-bridge converters are satisfied in the proposed converter. Fig.11 shows the synchronized gate signals and the resulting voltage waveforms of V_{AB}, V_A, and V_B. It can bee seen that the required V_{AB} of the proposed converter can be created using the synchronization circuit. Fig.12 shows the primary and secondary current waveforms of the auxiliary transformer T_r. It clearly shows that the waveforms are agreed well with the theoretical analysis. Fig.13 shows the dc link waveforms of a conventional and the proposed boost converter stage for the power factor correction operation. It is noted in this figure that the switching ripples of the inductor current i_{LB} waveforms are small due to the ZVS of S_B. Fig.14 shows the waveforms of the line voltage V_{AC}, line current I_{AC}, output voltage V_o and output current I_o. It can be seen that the unity power factor and tight output voltage regulation are obtained from the proposed converter. Fig.15 shows the overall efficiency as a function of the output load power. It is noted that the efficiency of the proposed converter is 93.7 % at the rated load.

IV. Conclusion

In this paper, a novel power factor correction ZVS rectifier/regulator topology, based on a boost converter and two half-bridge converters, is presented, which offers the following distinctive features:

◆ZVS for all power semiconductor switches
◆ZCS for the output diode of the boost converter stage
◆unity power factor
◆tight output voltage regulation with fast transient response
◆no low frequency harmonics on either input or output
◆transformer isolation.

In the conventional approach based on a ZVT PWM boost converter and a ZVS PWM half-bridge converter, the above discussed features cannot be obtained since there exists an auxiliary switch for the ZVT network in the boost converter, which actually has hard switching characteristics. The design considerations and control strategy for the proposed converter are described. The prototype successfully meets the unity power factor requirements with an efficiency of above 93.7 %. Furthermore, the proposed converter does not need any semiconductor switch for a ZVS operation of the boost converter, which can result in a reduced cost in designing a rectifier/regulator module used in distributed power system applications.

References

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[2]P. Imbertson and N. Mohan,"Asymmetrical duty cycle permits zero switching loss in PWM circuits with no conduction loss penalty", IEEE.Trans.on.IA.,vol.29, no.1, January 1993, pp.121-125.

[3]L. Dixon, "High power factor pre-regulators for off line power supply", Unitrode switching regulated power supply design seminar manual, 1990, pp.12.1-12.16.

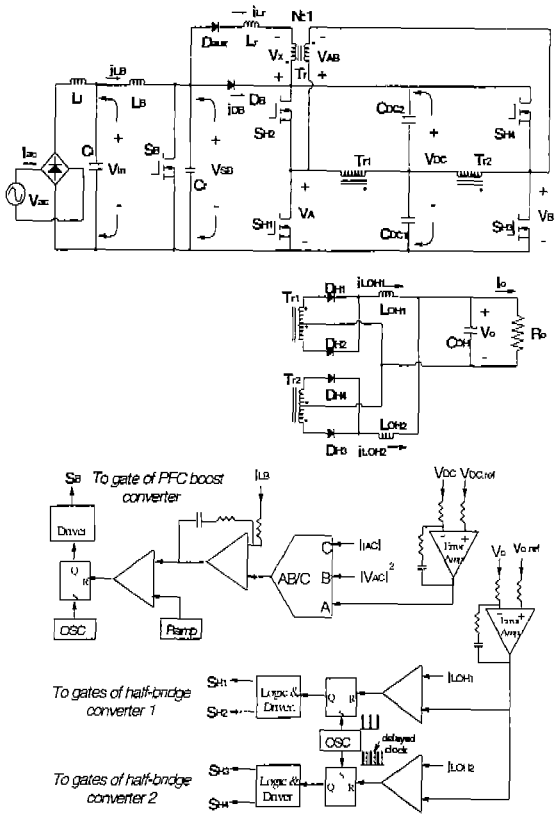


Fig.1. Circuit diagram of the proposed PFC rectifier/regulator

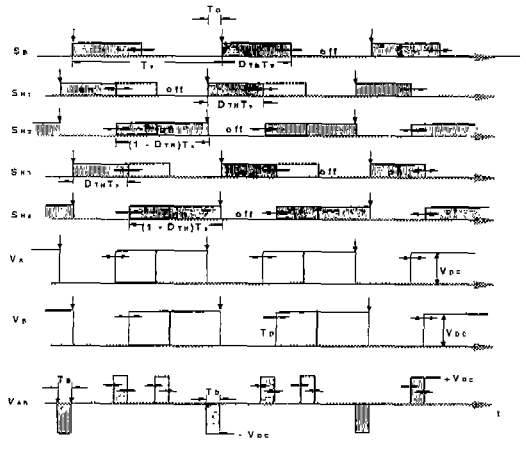


Fig.2. Synchronized gates signals and DC link feedback pulses

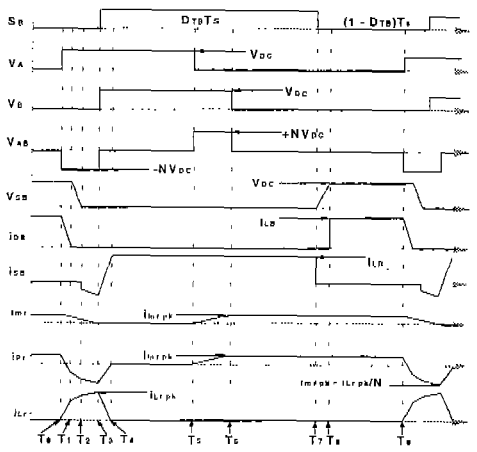
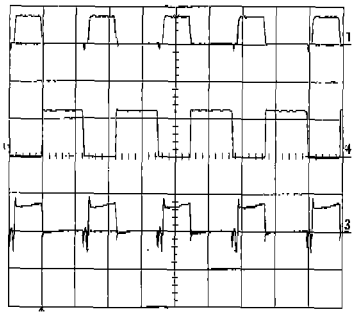


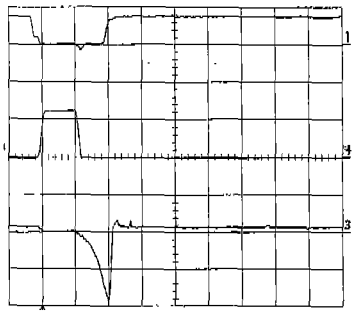
Fig.4. Key waveforms of the proposed rectifier/regulator



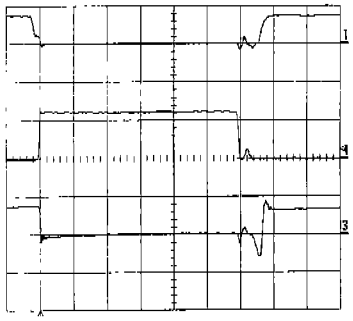
(a) Voltage/current waveforms of the switch S_B in case of small duty cycle D_{TB}:

(b) Voltage/current waveforms of the switch S_B in case of large duty cycle D_{TB}:

Fig.7. The switch voltage and current waveforms in the boost rectifier stage (time : $5us / div$)

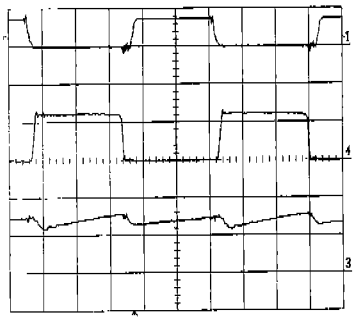


(a) Turn-on transient waveforms in case of large D_{TB}:

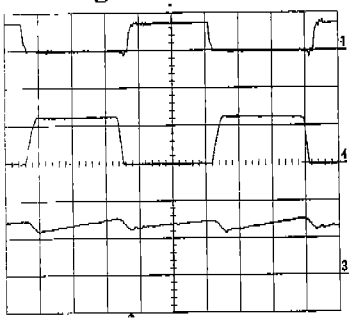


(b) Turn-on transient waveforms in case of small D_{TB}:

Fig.8 Turn-on Transient waveforms of the boost switch S_B (time : $1us / div$)

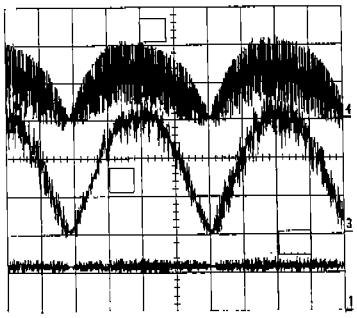


(a) Half-bridge converter 1 waveforms:

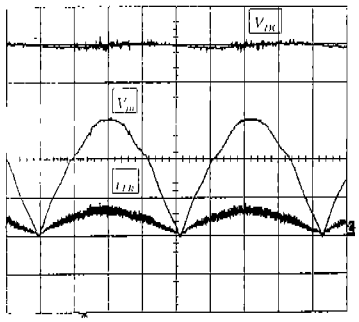


(b) Half-bridge converter 2 waveforms:

Fig.10. The switch voltage waveforms and the output current waveformsof two paralleled half-bridge converters (time : $2us / div$)



(a) Conventional hard switching PFC boost rectifier waveforms



(b) Proposed ZVS PFC boost rectifier waveforms;

Fig.13 Experimental dc link waveforms of PFC operation(time: $2ms / div$)

◆ PFC Boost Rectifier Stage

S_B	IRF450 (VDS=500V,ID=14A.)
L_B	500uH
C_{DC1} 、 C_{DC2}	1000uF
D_B	S30L60 (Io=30A, VR=600V)

◆ Half-Bridge DC-DC Converter Stage

$S_{H1,2,3,4}$	IRF450
$D_{H1,2,3,4}$	S30L60
$L_{OH1,2}$	50uH
C_{OH}	220uF
$T_{r1,2}$	L_m=100uH, L_{lk}=20uH, $N = 6/11$
T_r	L_m=100uH, L_r=20uH, N=1.2
D_{aux}	S30L60

Table. 1. Proposed converter parameters