Two Stage Power Factor Correction (PFC) Converter With A Single PWM Controller

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ABSTRACT – **Two-stage power factor correction (PFC) converter with a single PWM controller for universal input voltage (90-264V) is proposed. It consists of a power factor pre-regulator cascaded by a DC/DC converter as in a conventional two-stage approach. However, a single PWM controller is used as in a single-stage, single-switch PFC approach. The switch in the PFC part is synchronized with the switch in the DC/DC converter with a fixed switching frequency. Employing an adaptive delay scheme the switch in the PFC part is controlled to limit the energy storage capacitor voltage within a designed range for the optimum efficiency, and to reduce input current harmonic distortion. The experimental results obtained on a 200W (5V/40A) prototype PFC converter are given to verify the effectiveness of the proposed control method.**

I. Introduction

Recently international regulations governing the amount of harmonic currents (e.g. IEC-1000-3-2) were imposed to the lower power level applications. great deal of effort has been made for the last several years to develop efficient and cost effective power factor correction (PFC) schemes,. A number of single-stage scheme were proposed in order to improve efficiency and to reduce cost and size from the conventional two-stage schemes, which usually employ power factor pre-regulator cascaded by a DC/DC converter [1-3].

In general, the single-stage PFC converters operate in discontinuous conduction mode (DCM), and offer inherent power factor correction capability. Since this type of converters use a single switch controlled by a conventional PWM controller, an additional control circuitry for PFC can be eliminated. Indeed the single-stage approach has many advantages over two-stage approach when the power level is low and the load range is not wide. However, one of the main drawbacks of single-stage PFC converter is that the voltage on the energy storage capacitor increases as the line voltage increases and/or output current decreases and this forces to use high voltage rating switching devices. To reduce the capacitor voltage, frequency modulation technique can be employed [3]. In this approach, the switching frequency varies over a wide range, and the efficiency is deteriorated. This makes this type of converter impractical for the universal input applications having a wide range of line input voltage (90-264V) and load current specification. Moreover, the switch of the single-stage converter has a large current stress because it carries both the boost current and the DC/DC converter current. In fact, a trade off study shows that a single-stage, single-switch approach is not a good candidate for 200-300W power level.

Another drawback of single-stage approach is that the voltage of the energy storage capacitor should be kept relatively high in order to achieve high power factor. To achieve high power factor keeping relatively low capacitor voltage, some control methods have been proposed [6-7]. However, these approaches are not suitable for universal input application.

In order to overcome the above mentioned problems, of singe-stage approach, a two-stage PFC converter with a single PWM controller for universal line input voltage was proposed [4]. In that approach, a single PWM controller with a simple delay scheme drives the switches of the PFC part and the DC/DC converter part respectively, to keep the capacitor voltage within the optimal range. However, since it employs constant duty DCM boost, there always exist some input current harmonic distortion. In this paper, in order to improve the input current harmonic distortion an adaptive delay control scheme is proposed, where the line input voltage variation is used as an input of the delay control. With the proposed control method, the capacitor voltage is regulated within the optimal range keeping high power factor (greater than 98%) and low input current harmonics over the universal input voltage range.

II. Proposed control scheme

Fig.1 shows the circuit diagram of Boost Integrated with Buck Rectifier/Energy storage/Dc-dc converter (BIBRED) as an example of single-stage PFC converter [2]. It can be understood as an integrated connection of boost converter with an isolated DC/DC converter (Buck) as identified by the dotted-line boxes. As can be seen in Fig.1, when the switch Q1 is turned on both the boost current I_1 and the primary current of the DC/DC converter I_{c1} flow through the switch. This increases the current stress on the switch, which forces to use two or more

switches in parallel for above 100W power level.

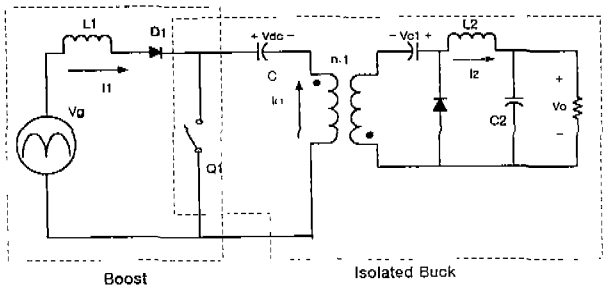


Fig.1 Circuit diagram of single-stage PFC converter (BIBRED)

In the proposed approach the boost converter and the isolated DC/DC converter are cascaded as in a conventional two-stage approach. However, in the proposed approach additional PWM controller for the boost part is not necessary since single PWM controller with an adaptive delay scheme drives the switches of the boost PFC part and the DC/DC converter part respectively with a different duty ratio [4]. The circuit diagram of the proposed PFC converter employing the delay control is shown in Fig.2. The converter has a boost PFC switch, Q1 synchronized with the switch, Q2 of the cascaded DC/DC converter. Q2 is controlled to regulate the DC output voltage by PWM controller. And Q1 is controlled by the adaptive delay scheme to keep the capacitor voltage within a desired range and to reduce input current harmonic distortion depending on the operating condition.

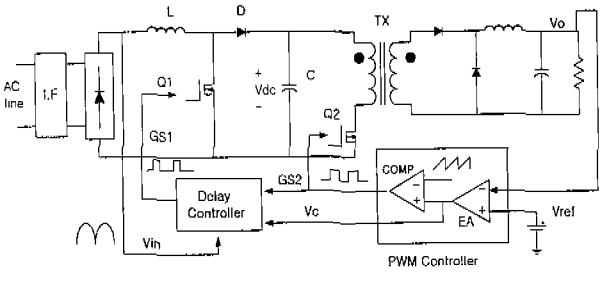


Fig.2 Circuit diagram of the proposed PFC converter

As can be seen in Fig.2 the inputs of the delay controller are the gate drive signal for Q2 (GS2), the error amplifier output voltage (Vc) and the rectified input voltage (Vin). The delay controller adds turn-on delay (Dx) and turn-off delay (Dy) to the gate drive signal of forward switch Q2 (GS2) as can be seen in Fig.3 and the duty ratio of boost switch Q1 is given by

$$D_B = D_F - D_X + D_Y \tag{1}$$

where D_F is the duty ratio of forward switch Q2. In the proposed control scheme, the duty ratio of the boost switch is controlled by modulating the turn-on delay (Dx) and turn-off delay (Dy). Moreover, Since the gate signals of the Q1 and Q2 are synchronized, the switch Q1 is protected automatically when the DC/DC converter is protected by alarm signals such as over current and over voltage.

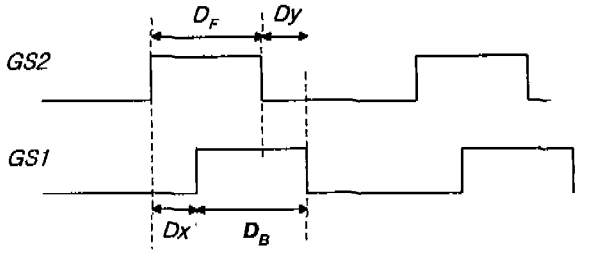


Fig.3 Gate signals for Q1 and Q2

2.1. Turn on delay Dx

Since the boost PFC part operates in DCM for an inherent PFC capability, if the two switches, Q1 and Q2 operate with the same duty ratio, the energy storage capacitor voltage will increase as the load current decreases and/or line voltage increases as in a single-stage PFC converter. For efficiency and optimum design of the transformer such a large variation of the capacitor voltage is undesirable. To keep the capacitor voltage within a desired range, the boost switch duty ratio D_B should be modulated according to the capacitor voltage. By introducing turn-on delay proportional to the capacitor voltage to the gate drive signal of S2, it is possible to control D_B without using another PWM controller.

In the proposed control method, the error amplifier output voltage of the PWM controller (Vc) is used as an input of the delay controller instead of the capacitor voltage since the capacitor voltage is given by

$$Vdc = \frac{n \cdot V_o}{D_F} = \frac{n \cdot V_o \cdot V_P}{Vc} \tag{2}$$

$$\cong nV_oV_P\left(\frac{1}{V_{CO}} - \frac{(V_C - V_{CO})}{V_{CO}^2} + \frac{2(V_C - V_{CO})^2}{V_{CO}^3} - \cdots\right) \cong V_{dO} - K_1 V_C \tag{3}$$

where n is the turn ratio of the transformer, Vo is the output voltage, V_P is the amplitude of ramp of PWM controller, V_{CO} is the value of error amplifier output voltage where the Taylor series expansion is done, and V_{dO} and K_1 are constants. From (1) - (3) the boost switch duty ratio is given by

$$D_B = \frac{V_C}{V_P} - K_d(V_{dO} - K_1 \cdot V_C) + D_y \approx K_{dx} \cdot V_C + B + D_y \tag{4}$$

where K_d is a constant, B is the offset and K_{dx} is the gain of the turn-off delay control.

2.2. Turn off delay D_y

For the DCM boost converter, the boost gain (the ratio of the energy storage capacitor voltage to the peak of the line input voltage) should be kept relatively high in order to draw an almost sinusoidal current from the mains. This imposes high voltage stress on the energy storage capacitor for high power factor and the boost gain should be greater than 1.29 to achieve power factor greater than 0.95 [5]. In that case the capacitor voltage could be higher than 480V for universal line input voltage.

So far, some techniques to reduce input current harmonic distortion using variable frequency control or variable duty-ratio control have been proposed [6-7]. However, the variable frequency control method requires wide range of frequency variation and the variable duty-ratio control method needs another PWM controller and complex control circuit.

The line input current of the PFC part is expressed as

$$i_{in} = V_{in} \frac{D_B^2}{2L \cdot fs} \cdot \frac{V_{dc}}{V_{dc} - V_{in}} \tag{5}$$

where L is the boost inductor, V_{in} is the rectified line voltage, and fs is the switching frequency. In order to make the line input current of (5) sinusoid, D_B should be modulated periodically with a frequency twice of the line frequency as follows ;

$$D_B = D_{BM} \cdot \sqrt{1 - \frac{V_{in}}{V_{dc}}} \tag{6}$$

where D_{BM} is a constant. The exact implementation of (6) requires complex control circuit because it involves the division of V_{in} by V_{dc} and the square-root function. However, in the proposed control scheme the energy storage capacitor voltage V_{dc} is kept around the peak of the maximum line input voltage (about 400V), and V_{dc} in (6) can be considered as almost constant. Then, D_B of (6) can be approximated as ;

$$D_B = D_{BM} - \frac{K_2}{V_{dc}} \cdot V_{in} = D_{BM} - K_{dy} \cdot V_{in} \tag{7}$$

where K_{dy} is the gain of the turn-off delay control. Fig. 4 shows D_B of (6) and (7) as a function of rectified line voltage. As can be seen the plot generated using (6) can be approximated with the linear equation of (7) and the control law of (7) can be simply implemented by introducing the turn-off delay proportional to the line voltage. Since it represents a continuous adjustment of the duty ratio according to the variation of V_{in} , it can be thought as a kind of feedforward control. With (4) and (7), the overall control law of D_B can be expressed as

$$D_B = K_{dx} \cdot Vc - K_{dy} \cdot V_{in} + D_o \tag{8}$$

where K_{dx}, K_{dy} are the turn-on and turn-off delay gain respectively and Do is the offset.

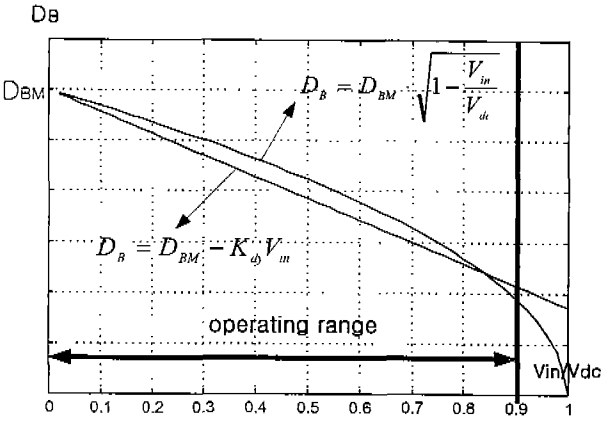


Fig.4 D_B as a function of line voltage

2.3. Procedure to determine the delay control gains

Fig.5 shows boost switch duty ratio D_B and Forward switch duty ratio D_F as a function of error amplifier output voltage Vc using (8). Since D_B is changed periodically according to the rectified line voltage, it is indicated with a gray area. The maximum duty ratio D_{Bmax} and D_{Fmax} occur at the minimum line voltage with maximum load, and the minimum duty ratio D_{Bmin} and D_{Fmin} occur at the maximum line voltage with minimum load.

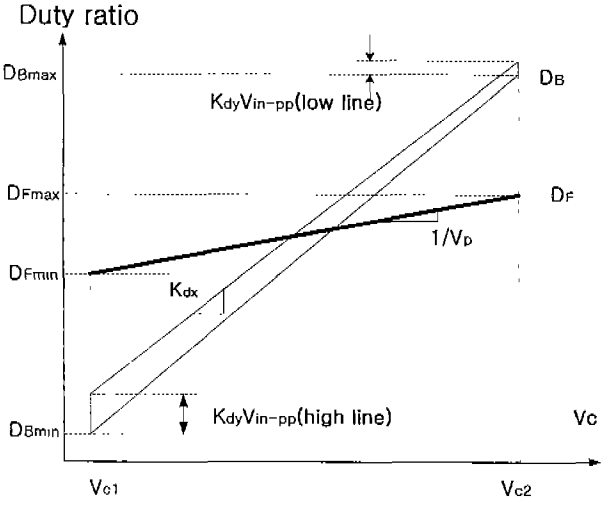


Fig.5 D_B and D_F as a function of Vc

From (2) and Fig.5 the range of the energy storage capacitor voltage is determined with D_{Fmax} and D_{Fmin} as follows ;

$$\frac{n \cdot V_O}{D_{F\max}} \le V_{dc} \le \frac{n \cdot V_O}{D_{F\min}} \tag{9}$$

If the line input current is a perfect sinusoid, from (5) and (8) the rms of the line input current is given by

$$i_{in}^{rms} = V_{in}^{rms} \frac{(K_{dx}V_c - K_{dy}V_{in}^{peak} + D_o)^2}{2L \cdot fs} \cdot \frac{V_{dc}}{V_{dc} - V_{in}^{peak}} \quad (10)$$

Using (10), D_{Bmax} and D_{Bmin} can be calculated at minimum line voltage with full load and at the maximum line voltage with the minimum load respectively using the input-output power balance equations ;

$$P_O^{max} = \frac{V_{in-low}^{rms\ 2} \cdot D_{Bmax}^{\ 2}}{2L \cdot fs} \cdot \frac{V_{dc}^{min}}{V_{dc}^{min} - V_{in-low}^{peak}} \cdot \eta_1 \quad (11)$$

$$P_O^{min} = \frac{V_{in-high}^{rms\ 2} \cdot D_{Bmin}^{\ 2}}{2L \cdot fs} \cdot \frac{V_{dc}^{max}}{V_{dc}^{max} - V_{in-high}^{peak}} \cdot \eta_2 \quad (12)$$

where P_o is the output power ,$V_{in\text{-}high}$ and $V_{in\text{-}low}$ are the maximum and minimum line voltage respectively, and η_1 and η_2 are the estimated efficiencies under full load and minimum load condition respectively.

From (6) and (7), the turn-off delay gain K_{dy} is given by

$$K_{dy} = \frac{3D_{Bmin}}{V_{in-high}^{peak}} \left(\sqrt{\frac{V_{dc}^{max}}{V_{dc}^{max} - V_{in-high}^{peak}}} - 1 \right) \quad (13)$$

where $3D_{Bmin}$ is used instead of D_{Bmin} to optimized K_{dy} for the full load condition.

From (11) – (13) the turn-on delay gain K_{dx} is given by

$$K_{dx} = \frac{D_{Bmax} - D_{Bmin} - K_{dy}(V_{in-high}^{peak} - V_{in-low}^{peak})}{V_{c2} - V_{c1}} \quad (14)$$

III. Simulation and experimental results.

To verify the effectiveness of the proposed control method, experimental 200W PFC converter with the following specifications was designed:

V_{in}^{rms} = 85-265 V (universal input) Vo=5 V

Io= 4-40 A (20-200W) fs= 50 kHz

The circuit diagram of the power stage is shown in Fig.1. It was built with the following components. Q1 : IRFP450, Q2 : IRFPG50, D : MUR860, C : 450V/220Uf, L : 105uH(PQ3220), and TX : EER35 (primary :70 T, +5V secondary: 4T, +12V secondary: 9T). The delay control is implemented using one CMOS IC 4011, two transistors and one OP-AMP as shown in Fig.5. T1, R1 and T2, R2 act as a voltage controlled current source that makes the variable turn-on delay, Dx and turn off delay, D_Y respectively.

Fig.6 shows the simulated and measured capacitor voltages respectively. The parameters of (8) used in the simulation are as follows; K_{dx} =0.412, K_{dy} =5.25 $\times 10^{-4}$, D_o = -1.45. As can be seen from Fig.6 the capacitor voltage is kept within 310-410V range from the minimum load to full load over the universal line input voltage range.

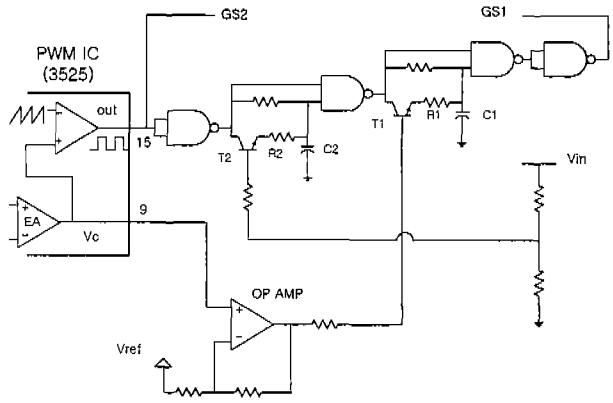


Fig 5. Circuit implementation of the proposed delay scheme

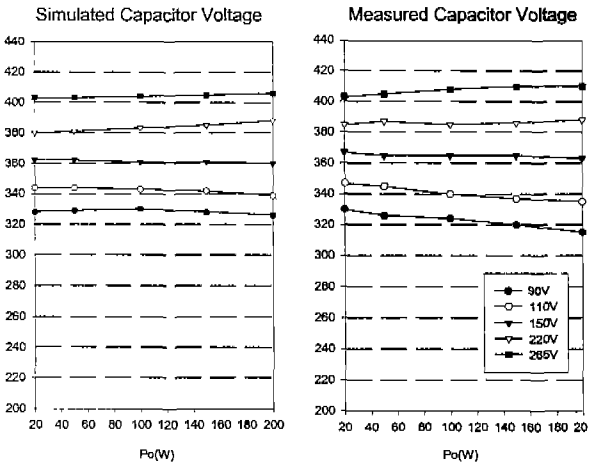
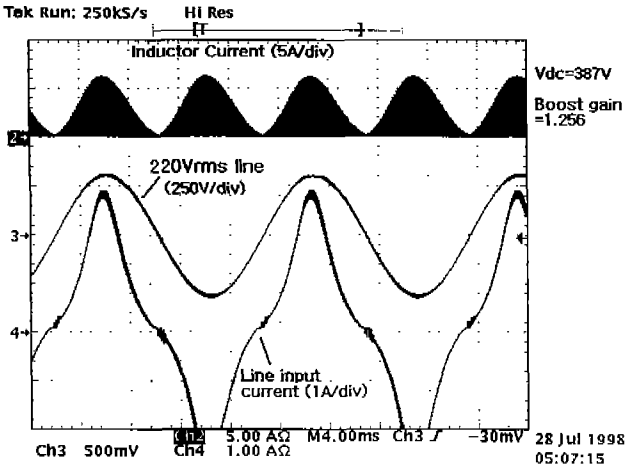


Fig.6 Simulated and measured capacitor voltage as a function of load

Fig.7 and 8 show the input current waveforms of the DCM boost PFC converter and the proposed control method respectively to show the effectiveness of the proposed control method in reducing input current harmonic distortion. The line voltage is 220Vrms and 265Vrms at full load and the capacitor voltage is kept at the same value for each case. As can be seen, the line input current waveforms remain almost sinusoidal while the input current distortion of DCM boost increases as the boost gain decreases. Fig.9 compares the harmonic components of the line input currents of Fig.7 and 8, and shows that the input current harmonics of the proposed method are much reduced compared to the DCM boost PFC converter.



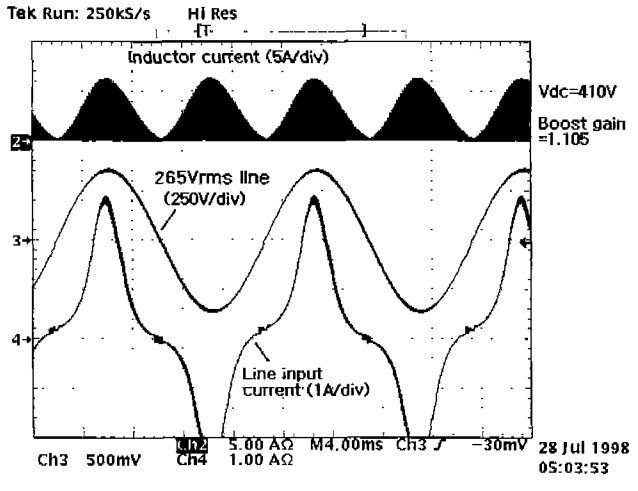
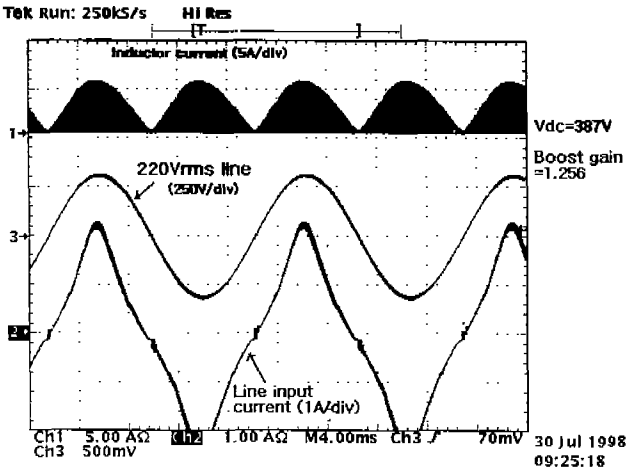


Fig.7 Input current waveform of DCM boost PFC



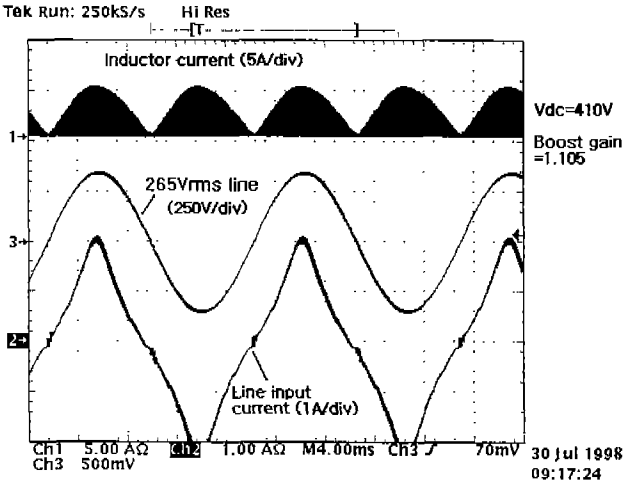
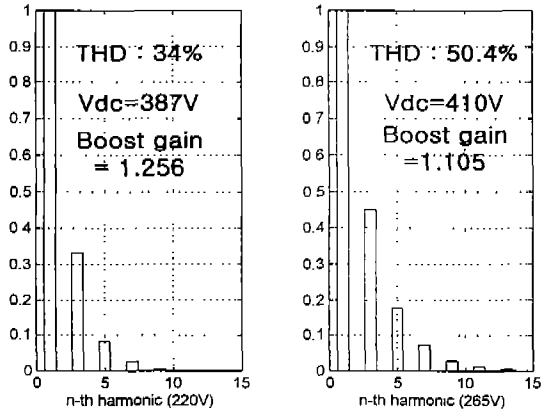
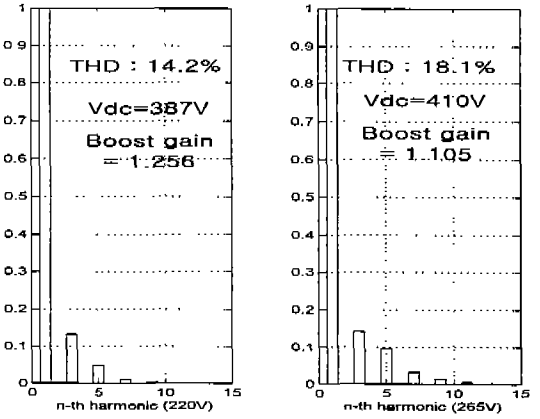


Fig .8 Input current waveform of the proposed control method



DCM boost PFC converter



When the proposed control method is used

Fig.9 Normalized FFT of the line input currents of Fig.7 and Fig.8

Fig.10 and 11 compare the THD and the power factor of the proposed control method with those of DCM boost PFC converter when the boost gain is kept at the same value for each case. As can be seen, when the proposed control method is applied the THD is kept lower than 20% and the power factor is kept greater than 98% over the universal input voltage range.

Fig.12 shows the measured equivalent line input current harmonic components for different line voltages on full load condition. All line current harmonics are below the IEC-1000-3-2 class D requirement over the universal line input voltage range.

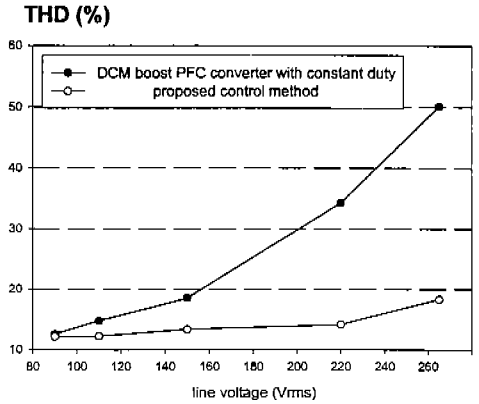


Fig.10 THD for different line voltages

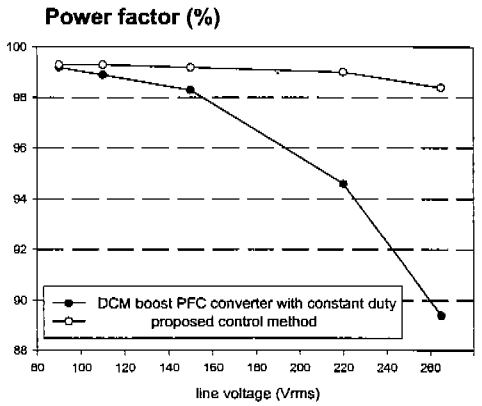


Fig:11 Power factor for different line voltages

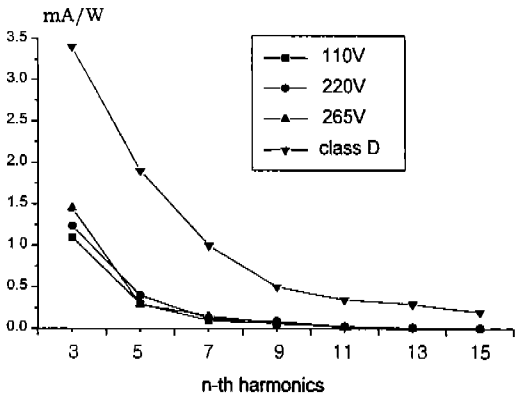


Fig.12 Measured equivalent line input current harmonics

IV. Conclusion

Due to the high current and voltage stress, single-stage PFC converter is not suitable for universal input applications with 200-300W power level in respect of efficiency and cost. In the proposed approach, the two-stage PFC converter with a single PWM controller employing a adaptive delay scheme is used. With the proposed control method, the energy storage capacitor voltage is regulated within the optimal range keeping high power factor and low input current harmonic distortion over the universal input voltage range.

V. Reference

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