OPTIMIZATION TECHNIQUE FOR HIGH QUALITY RECTIFIERS

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ABSTRACT - A procedure for the optimal design of high quality rectifiers is introduced in this paper. The procedure is capable of producing different optimal designs for the same rectifier based on the objective performance required from that rectifier. A FORTRAN-based computer system designed to solve large-scale optimization problems was used in this work to obtain the optimal designs. The optimization program uses Wolfe algorithm in conjunction with a quasi-Newton algorithm as well as a projected augmented Lagrangian algorithm to solve the highly nonlinear optimization problem. The paper also introduces a detailed analysis and an application of the procedure on a boost-type zero-current switch (ZCS) single-switch three-phase rectifier introduced recently in the literature. The obtained results are compared with popular simulation packages (i. e. PSPICE and SIMCAD) to support the validity of the proposed concept.

1. INTRODUCTION

The concern regarding power system harmonic currents and power quality has grown in recent years due to the wide-spread of electronics loads. The power industry realizes significant benefits from demand-side power factor correction. Only a portion of the total costs attributed to low power factor is recovered through power factor penalties or kVA-based demand charges. Eliminating unnecessary demand for electric current means fuel savings, reduced transmission and transformer losses, improved voltage regulation, and an increase in available capacity throughout the power company's system without additional investment in generation or distribution. Reducing peak current demand can allow the utility to postpone the construction of new generating capacity. The utilities recognize that demand-side power factor correction is a very effective way to improve service and reduce costs and, best of all, improve the utility's competitiveness in a deregulated environment. For these reasons and more, the modern power quality standards [1-2] demand the benefit of acting as a high-power-factor (HPF) load. Designers normally try to meet these standards at the lowest cost.

Many low cost HPF rectifiers (single-phase and three-phase) have become a focus of attention in the recent literature's [3-19]. However, the optimal choice of parameters of the different rectifiers in order to obtain optimal performance indices is a subject which has not been tackled thoroughly in the literature. Studies introduced in [10-12] which allow the informed optimization of the power stage design are important for the designers.

The work presented herein introduces a procedure capable of providing the optimal selection of any rectifier parameters based on the performance index or indices the user of the rectifier may require. Due to the large number of performance indices and control parameters of any rectifier, as well as the highly non-linear relationships between the control parameters in the performance indices, the optimal parameter choice becomes a complicated problem. Because of such high non-linearity, a FORTRAN-based computer system designed to solve large-scale optimization problems [20] was used in this paper. In addition, and in order to simplify the complicated design problem and to obtain results with high degree of acceptance, the suggested procedure starts with analyzing the different rectifier performance indices in terms of each of the rectifier design parameters while the other design parameters are kept constant. The analysis step is then followed by deriving empirical formula for each rectifier index in terms of each of the rectifier design parameters. Finally, the optimization problem is formulated as an objective function containing the performance index or indices with equal or unequal weighting factors based on the importance of each of the performance indices to the user. The objective function is then optimized (minimized or maximized) subject to the constraints imposed by the relationships between the different design parameters as well as any bounds may required to be imposed on some or all the performance indices not included in the objective function. Limits on the values of the rectifier design (control) parameters can also be added to the optimization formulation in order to obtain the optimal solution at practical values for such parameters.

2. OPTIMIZATION PROBLEM FORMULATION

The performance of any rectifier system is always measured by different indices such as total harmonic distortion in the input current, dc output power, total stresses on the switches, etc. Such rectifier performance indices vary widely between the different rectifier topologies and can be controlled by the proper choice of different components such as switching frequency, inductors, capacitors, etc., within the same topology. Such components are usually called the design or control parameters.

Let us refer to the rectifier control parameters by the variables $X_1, X_2, ..., X_N$; where N is the number of the control parameters in a certain rectifier topology. As for the rectifier performance indices, let us refer to them by the functions $f_1(X_1, X_2, ..., X_N)$, $f_2(X_1, X_2, ..., X_N)$, ..., $f_M(X_1, X_2, ..., X_N)$, where M is the number of the rectifier performance indices under consideration.

Now, let us assume that we want to obtain the practical values of the rectifier components which optimize the value of the i[th] index while the other performance indices are bounded by some upper and/or lower bounds. This problem can be formulated mathematically in the form,

$$\text{Optimize} \quad f_i(X_1, X_2, ..., X_N) \tag{1}$$

w.r.t. $X_1, X_2, ..., X_N$, subject to

$$LF_m \le f_m(X_1, X_2, \cdots, X_N) \le UF_m; \quad m = 1,2,\cdots,M; m \ne i \tag{2}$$

$$LZ_k \le Z_k(X_1, X_2, \cdots, X_N) \le UZ_k; \quad k = 1,2,\cdots,K \tag{3}$$

$$LX_n \le X_n \le UX_n; \quad n = 1,2,\cdots,N \tag{4}$$

where LF_m and UF_m are the lower and upper limits on the performance index m. Function $Z_k (X_1, X_2, ..., X_N)$ presents the k^{th} relation in a set of K relationships between the rectifier control parameters. Such set of relationships may be in the form of equality constraints (=) or in the form of upper (UZ) and/or lower (LZ) bounds. LX_n and UX_n are the lower and upper practical limits, respectively, on the control parameter n. Optimizing the performance index (f_i) may take the form of minimization or maximization.

The optimal solution of the above formulated problem (Eqs. (1) - (4)) gives the values of the rectifier parameters which produce the optimal (minimum or maximum) value of the i^{th} rectifier performance index, while the other rectifier performance indices lie within the imposed required limits.

The suggested optimization procedure is very powerful in a way that it can not only optimize one performance index but also can optimize more than one index at the same time while imposing limits on the other indices. For example, it can minimize both performance indices (f_i) and (f_j) while imposing limits on the values of the remaining (M-2) indices. The performance indices involved in the objective function may also be of different importance to the user and therefore, such indices may take different weighting factors in the problem formulation. In such case, the formulation presented in (1)-(4), will be modified as follows

$$\text{Minimize} \quad w_i * f_i(X_1, X_2, ..., X_N) + w_j * f_j(X_1, X_2, ..., X_N) \qquad (5)$$

w.r.t. $X_1, X_2, ..., X_N$, *subject to*

$$LF_m \le f_m(X_1, X_2, \cdots, X_N) \le UF_m; \quad m = 1,2,\cdots,M; \ m \ne i \& j \qquad (6)$$

$$LZ_k \le Z_k(X_1, X_2, \cdots, X_N) \le UZ_k; \quad k = 1,2,\cdots,K \qquad (7)$$

$$LX_n \le X_n \le UX_n; \quad n = 1,2,\cdots,N \qquad (8)$$

where w_i and w_j are the weighting factors associated with performance indices i and j, respectively. One can also minimize a performance index (e.g. f_i) and maximize another (e.g. f_j) at the same time, and in this case (5) will take the form

$$\text{Minimize} \quad w_i * f_i(X_1, X_2, ..., X_N) + w_j / f_j(X_1, X_2, ..., X_N) \qquad (9)$$

It should also be mentioned here that the rectifier performance indices have values of different order of magnitudes, and accordingly, the performance indices should be used in per-unit system especially if the objective function is associated with more than one performance index.

3. APPLICATION

In order to check the validity, applicability, and successfulness of the suggested optimization procedure, it was applied to a low-distortion three-phase multi-resonant zero-current switch (ZCS) boost rectifier published earlier [19], and shown here in Fig. 1. This rectifier is selected as a case study because of its advantages, which includes:

- Use of a single controlled switch operating at ZCS, with good switch utilization.
- High power factor, low harmonic rectification is performed naturally.
- Constant semiconductor stresses at full and minimum load.
- Simple control circuit. The switch turn-on time is essentially constant for complete output load range. Thus, only the control of the switch turn-off time is required for frequency control..
- Small reactive components sized to filter the switching-frequency-, rather than line-frequency-, harmonics.

The rectifier ideal switching waveforms for the first 30° interval along with the switching sequence are shown in Fig. 2. The detailed circuit performance is presented in [19]. Referring to Fig. 1, the rectifier has three line inductors L_i, along with the output tank inductor L_r plus the tank capacitor C_r. These three components L_i, L_r, and C_r of the rectifier were considered as the control (design) parameters in the optimization problem, along with the rectifier output voltage V_o and the switching frequency F_s of the power switch Q. The rectifier performance was studied in terms of total percentage input current harmonics ($\%THDI$), output dc power of the rectifier (P_{out}), total stresses on both power switch Q (Q_{stress}) and dc-side diode D (D_{stress}), and the power switch silicon utilization factor (SUF). These performance indices are defined below in (10)-(14). Based on the above, this system has five control parameters (N = 5) and five performance indices (M = 5).

$$\%THDI = \frac{\sqrt{\sum_{i=2}^{NH} \left(I^{(i)}\right)^2}}{I^{(1)}} * 100 \qquad (10)$$

$$P_{out} = V_o * I_o \qquad (11)$$

$$Q_{stress} = V_{Q\text{-}peak} * I_{Q\text{-}peak} \qquad (12)$$

$$D_{stress} = V_{D\text{-}peak} * I_{D\text{-}peak} \qquad (13)$$

$$SUF = \frac{P_{out}}{Q_{stress}} \qquad (14)$$

where $I^{(i)}$ is the rms input harmonic current of order (i), $I^{(1)}$ the rms fundamental input current, NH the highest order of harmonics to be considered, I_o the output dc current, $V_{Q\text{-}peak}$ and $I_{Q\text{-}peak}$ the peak voltage and current of the power switch Q, respectively, $V_{D\text{-}peak}$ and $I_{D\text{-}peak}$ the peak voltage and current of the dc-side diode D, respectively. The total percentage input current harmonics were calculated for the system up to the first 25 order.

3.1 Performance Analysis

At first, the system performance was studied at an ac input line voltage of 208V, 60-Hz line frequency and the different system performance indices were obtained at a base case shown in Table 1. Then, each performance index was studied in terms of each of the control parameters by changing these control variables one at a time keeping the other variables constant.

Changes in the rectifier performance indices, in terms of the different design parameters, are shown in Figures 3-7. Fig. 3 shows that $\%THDI$ decreases with the increase in the output voltage. This can be explained by deep insight look to the behavior of the different quantities of the rectifier during its operation. Referring to Fig. 2, increasing V_o, while keeping the input line voltage constant, requires an increase in the input line currents i_a, i_b, and i_c. Such increase in line currents and output voltage causes larger areas under the line currents curves in each switching interval with sharper slopes of such curves after time t_3. Such changes in line currents waveforms lead to less total input current harmonics ($\%THDI$).

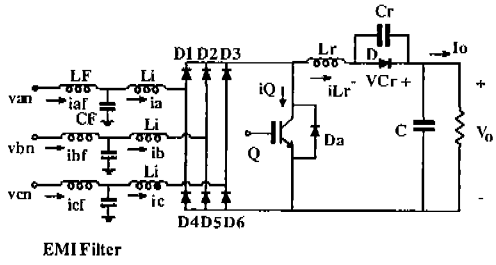

Fig. 1. Three-phase multi-resonant zero current switch boost rectifier [19].

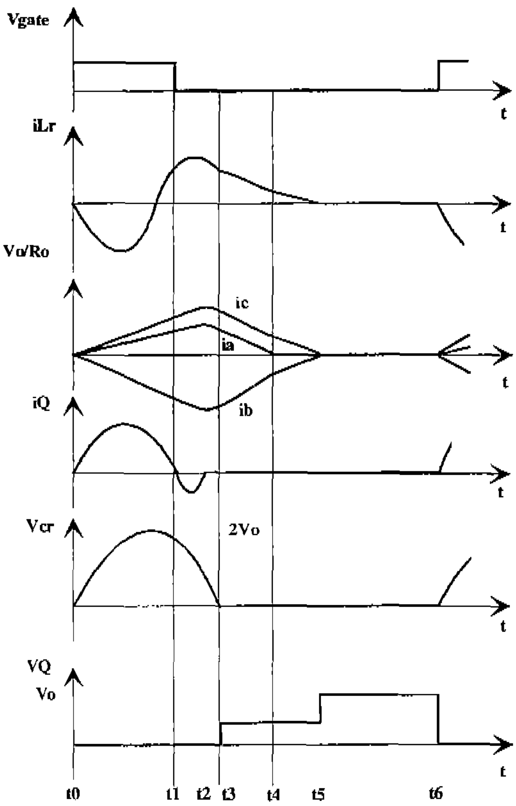

Fig. 2. Ideal switching waveforms for the rectifier of Fig. 1.

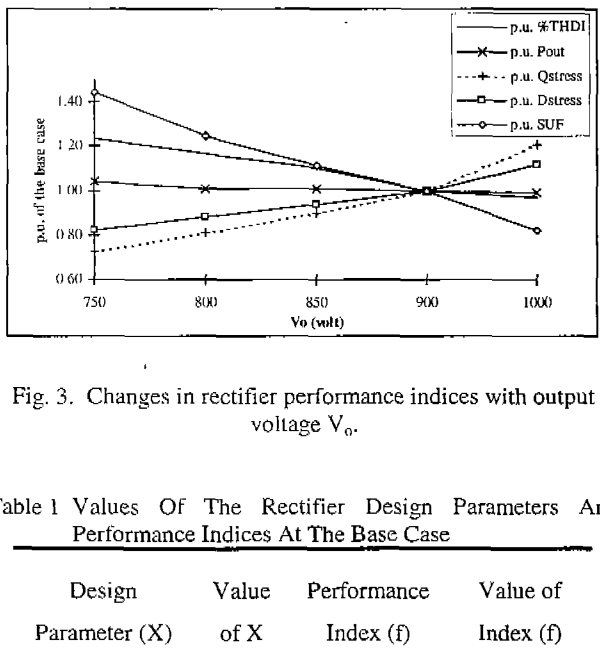

Fig. 3. Changes in rectifier performance indices with output voltage V_o.

Table 1 Values Of The Rectifier Design Parameters And Performance Indices At The Base Case

Design Parameter (X)	Value of X	Performance Index (f)	Value of Index (f)
V_o, volt	900	%THDI	5.73
F_s, kHz	60	P_{out}, kW	13.05
C_r, μF	0.25	Q_{stress}, kVA	159.8
L_r, μH	10	D_{stress}, kVA	181.9
L_i, μH	12.5	SUF	0.0817

The increase in V_o also causes an increase in the maximum capacitor voltage v_{cr} ($v_{cr,pk}=2V_o$) which then takes more time to discharge thus, the time interval from the beginning of the switching interval up to a complete discharge of C_r increases. Accordingly, the remaining interval time ($t_{3\text{-}5}$), over which the output current is calculated, would be slightly smaller leading to less output current. Therefore, the output dc power of the rectifier reduces with increasing V_o as shown in Fig. 3. On the other hand, the increase in input currents and output voltage causes an increase in i_{Lr}. From the above analysis for the behavior of the different rectifier waveforms, we can conclude that since input currents and i_{Lr} current values increase with the increase in V_o, the values of the power switch current i_Q also increases since $i_Q = -i_b - i_{Lr}$ [19]. Accordingly, both the power-switch peak current and the dc-side diode peak current also increase with V_o leading to higher Q_{stress} and D_{stress}, respectively. Finally, since P_{out} decreases with an increase in V_o while Q_{stress} increases, the silicon utilization factor (*SUF*) of the power switch deeply decreases as V_o increases.

The effects of both the tank inductor L_r and the tank capacitor C_r on the rectifier performance indices are shown in Figs. 4 and 5, respectively. Both L_r and C_r have great effect on the rectifier performance indices through two very effective factors defined in [19], which are

$$\text{The base impedance} = R_o = \sqrt{\frac{L_r}{C_r}} \tag{15}$$

$$\text{The base angular frequency} = \omega_r = \frac{1}{\sqrt{L_r C_r}} \tag{16}$$

Increasing L_r leads to an increase in R_o and a decrease in ω_r. Since the peak of i_{Lr} is inversely proportional with R_o while it oscillates with ω_r thus, increasing L_r causes i_{Lr} peak value to decrease and its wave length in the first interval in each switching period to increase, Fig. 2. Such changes in peak value and wavelength causes reduction in the peak value of i_Q producing less Q_{stress} with higher L_r. The above changes also cause t_{01}, t_{12}, and t_{23} to increase with L_r. Thus higher line currents are obtained at t_2. In the following time intervals in each switching period, the functions of i_a, i_b, i_c, and i_{Lr} contain terms directly proportional with $\sqrt{K_o}$, others inversely proportional with $\left(1-\frac{\omega^2}{\omega_r^2 K_o}\right)$, and sinusoidal terms with angular frequency $\omega_r\sqrt{K_o}$ where K_o was defined as [19],

$$K_o = \frac{3L_i}{2L_r} \tag{17}$$

Such complicated effects of L_r through K_o and ω_r in the current waveforms during time interval $t_{2\text{-}5}$ leads to an oscillation in the slope of the current curves after t_2 while the areas under the curves of these currents always increase due to the prime increase in the currents during the first two time intervals. The net effect of all such changes is shown in Fig. 4 as an oscillating increase in *%THDI* with L_r. Since the value of i_{Lr} at t_3, which is also the peak of the dc-side diode current, increases with L_r, thus, D_{stress} increases with L_r. On the other hand, since the area under i_{Lr} curve during the period $t_{3\text{-}5}$ increases with L_r, the average dc output current also increases leading to an increase in the output dc power. Due to the decrease in Q_{stress} and increase in P_{out} with L_r, *SUF* of the power switch *Q* highly increases with the increase in L_r. Similar analysis can be derived for the effects of C_r except that increasing C_r causes a reduction rather than an increase in R_o.

Increasing L_i leads to reduction in the line currents during the period $t_{0\text{-}2}$. The amplitude of the power switch current i_Q is also inversely proportional with L_i during the first two time intervals according to (18).

$$i_Q = \frac{-V_m}{\omega L_i}\left[\cos(\omega t_0 - 120^\circ) - \cos(\omega t - 120^\circ)\right] + \frac{V_o}{R_o}\sin(\omega_r(t-t_o)) \quad (18)$$

Accordingly, increasing L_i reduces $i_{Q\text{-}peak}$ leading to less Q_{stress}. On the other hand, L_i has a similar effect on *%THDI* as L_r through K_o with two differences. First, K_o increases with L_i instead of being reduce with L_r. Secondly, the areas under the input currents during the first two time intervals in each switching period are reduced with the increase in L_i rather than being increased with L_r. Accordingly, as it is shown in Fig. 6, an oscillating decay in *%THDI* with the increase in L_i was obtained. In addition, the resultant reduction in i_{Lr} current through the time interval $t_{3\text{-}5}$ with the increase in L_i leads to lower average dc-side diode current producing less output dc power, and also less peak current through the dc-side diode which results in less D_{stress}. The reduction in P_{out} with the increase in L_i is higher than the reduction in Q_{stress} and thus *SUF* of the power switch *Q* also reduces with the increase in L_i.

Finally, the effects of the switching frequency F_s on the rectifier performance indices are shown in Fig. 7. Such effects are mainly because increasing F_s means more switching periods under each power frequency cycle. This causes the input line currents to cover more area and take shapes closer to the sine wave leading to less harmonics. The average dc output current increases with increasing F_s so does P_{out}. Both power switch and dc-side diode peak currents approximately do not change with F_s and accordingly, both Q_{stress} and D_{stress} remain almost the same, while *SUF* of *Q* increases. These results are consistent with the results obtained in [19].

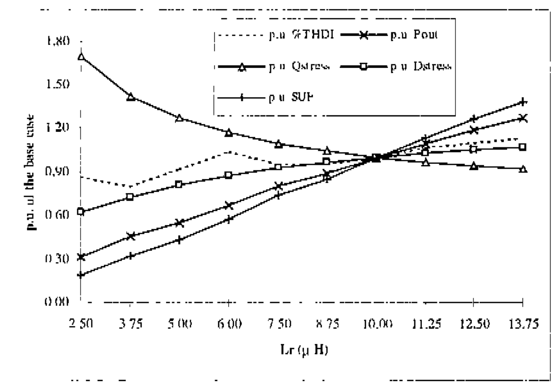

Fig. 4. Changes in rectifier performance indices with tank inductor L_r.

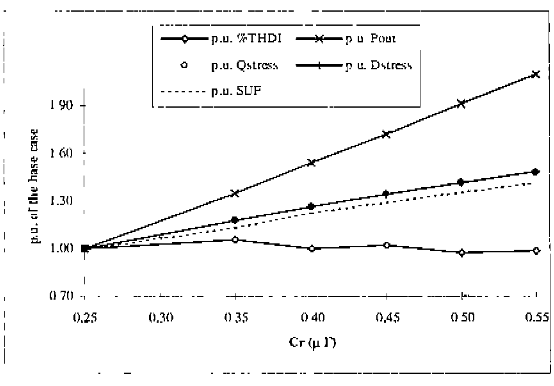

Fig. 5. Changes in rectifier performance indices with C_r.

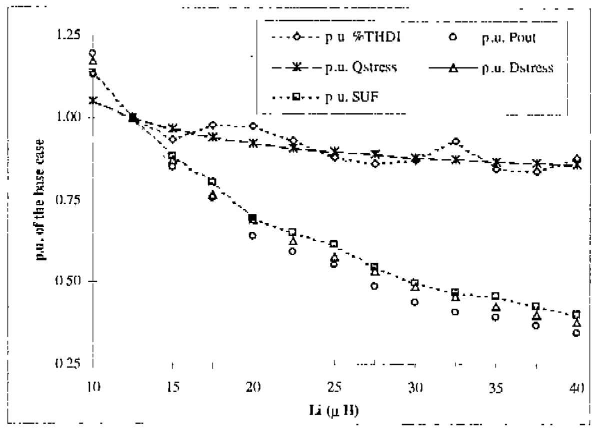

Fig. 6. Changes in rectifier performance indices with input inductor L_i.

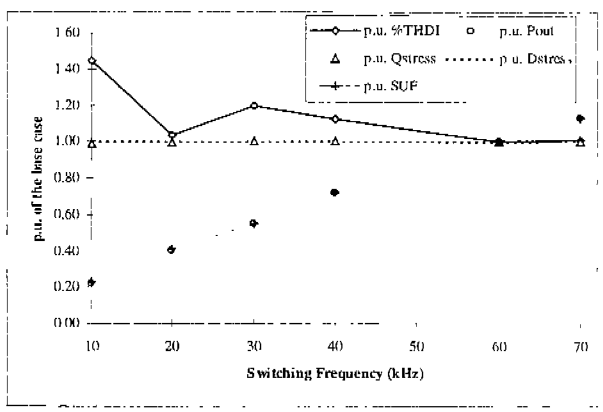

Fig. 7. Changes in rectifier performance indices with switching frequency F_s.

3.2. *Optimal Designs*

After the detailed analysis of the rectifier system under consideration, this section introduces the application of the optimization procedure to that system to obtain different optimal designs for different requirements.

Best fitting equations have been obtained for each of the performance indices as functions of the control variables. The optimization problem was then formulated using the best fitting equations and the optimal solution was obtained. For the rectifier described above, six optimal designs have been obtained to satisfy six different criteria, which are:

Case 1: The optimal solution required to obtain minimum total stresses on the power switch under some lower and upper limits imposed upon the other five performance indices.

Case 2: The optimal design required to obtain the minimum of the total stresses on both the power switch and the dc-side diode with the same upper and lower limits imposed upon the remaining four performance indices as in case 1.

Case 3: With the same limits on the performance indices, the optimal design required to obtain maximum output dc power from the rectifier was obtained.

Case 4: Cases 2 and 3 were joined together to give the optimal design needed to minimize total stresses on both power switch and dc-side diode and maximize the rectifier output dc power at the same time.

Case 5: Due to the importance of the harmonic specifications in any rectifier standards, the optimal design for minimum *%THDI* was obtained in this case with the same imposed limits as in the other cases.

Case 6: With the same limits, the optimal design for minimum Q_{stress} and *%THDI* with weighting factor of 2 for *%THDI* was finally obtained in this case.

Table 2 (in the Appendix) displays the values of the design parameters obtained in each of the above six cases, along with the value of each of the performance indices of the rectifier.

From Table 2, it is quite clear that stress on the power switch (Q_{stress}) in case 1 has the lowest value in the six studied cases as expected. When it was required to minimize the sum of the total stresses on both power switch (Q_{stress}) and dc-side diode (D_{stress}), as in case 2, or to minimize Q_{stress} with *%THDI*, as in case 6, a compromise has been done and Q_{stress} value was increased a little while D_{stress} in case 2 had a lower value than that in case 1, and the value of *%THDI* was increased than that of case 5. On the other hand, when the total stresses ($Q_{stress}+D_{stress}$) were to be minimized along with maximizing the output dc power (P_{out}), another compromise was done which led to a decrease in Q_{stress} in this case than that in case 2 but still higher than that value in case 1. The diode stress (D_{stress}) value was on the other hand, increased to a value higher than those of the other cases except that of case 3. This gives an indication that D_{stress} should have a weighting factor higher than 1.0 in the objective function of case 4 if we were interested in reducing it more. Also, in case 4, since Q_{stress} was minimized while P_{out} was maximized, the resultant *SUF* of the power switch *Q* was in this case the highest in all studied cases. The output power P_{out} in case 3 had a value higher than its value in all other cases but again less than its value in case 3 where it was required to maximize the output dc power P_{out} only. *%THDI* also had the lowest value in case 5 when it was minimized by itself.

The results of Table 2 are compared with several popular simulation packages such as PSPICE and SIMCAD to prove the validity of the proposed approach. The results came out in a good agreement. Fig. 8 shows a PSPICE simulation result for the rectifier of Fig. 1 using case 5 in Table 2. The input voltage is set to $208V_{L-L}$, the switch on-time is set to 7µsec, and the load resistance is set to 131.3Ω. The *THDI* in the line current is about 5.33%, which is very close to the predicted result (*THDI*=5.52%) in Table 2.

Although, the input current harmonics were considered in this application as the percentage total distortion defined by (10), it should be clear that the optimization procedure is capable of considering any individual harmonic(s) whether in the objective or as constraints.

4. CONCLUSION

A powerful optimization procedure has been introduced to provide the optimal design of three-phase single-switch rectifiers. The procedure can be generalized to any other type of rectifiers. The procedure is capable of providing the practical values of any rectifier design parameters which allow the rectifier to optimize its performance index which the user might be interested in and satisfy any limits he may wish to bound the other rectifier performance indices with. The procedure is also capable of handling more than one-performance indices as an objective function at the same time. The optimization program used in the procedure was very powerful in dealing with the highly nonlinear formulation characterizing the rectifier performance. The high non-linearity was also simplified using variable separation and best fitting technique.

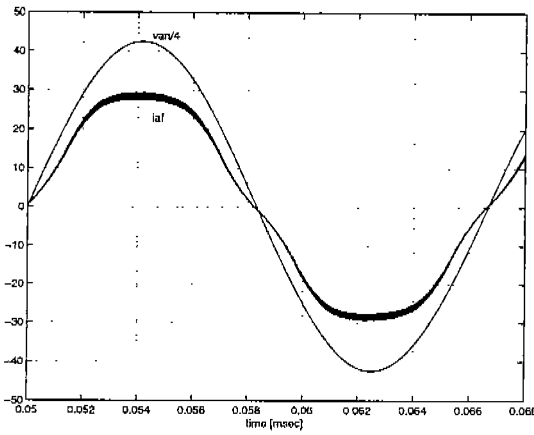

Fig. 8 Simulated input line current with its ac-phase voltage, for the rectifier of Fig. 1 with THDI 5.33%.

The procedure has been successfully tested on a low-distortion three-phase multi-resonant boost rectifier introduced recently in the literature.

The deep analysis of such rectifier showed contradiction between the effect of the different rectifier control parameters on the performance indices. Some of the parameters have positive impact on some of the rectifier performance and negative impact on some other indices. Some other parameters have opposite impact on the rectifier performance. Accordingly, the proper parameter choice of any rectifier system is essential and varies according to the objective required from the system and the standards. The suggested optimization procedure is very effective in making such choices for any considered rectifier topology.

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APPENDIX

Table 2 Summary Of The Optimal Solution Obtained For The Rectifier System [19] In Six Different Cases

Case No.	Design Parameter (X)	Value of X	Rectifier Performance Index (f)	Value of Index (f)	Objective
1	V_o [volt]	878.7	*%THDI*	7.0	minimize Q_{stress}
	F_s [kHz]	39.14	P_{out}, *kW*	9.7	Result:
	C_r [μF]	0.25	D_{stress}, *kVA*	168.1	Q_{stress} = 134.8 kVA
	L_r, L_i [μH]	13.75, 14.9	*SUF*	0.07	
2	V_o [volt]	878.7			minimize $Q_{stress}+D_{stress}$
	F_s [kHz]	45.43	*%THDI*	5.67	Results:
	C_r [μF]	0.25	P_{out}, *kW*	8.96	Q_{stress} = 145.5 kVA
	L_r, L_i [μH]	10.5, 14.9	*SUF*	0.062	D_{stress} = 157.7 kVA
3	V_o [volt]	878.7	*%THDI*	6.13	maximize P_{out}
	F_s [kHz]	55.44	Q_{stress}, *kVA*	173.3	Result:
	C_r [μF]	0.3	D_{stress}, *kVA*	211.5	P_{out} = 16.05 kW
	L_r, L_i [μH]	9.88, 11.14	*SUF*	0.092	
4	V_o [volt]	878.7			minimize $Q_{stress}+D_{stress}$ &
	F_s [kHz]	55.44	*%THDI*	6.3	maximize P_{out}
	C_r [μF]	0.25	*SUF*	0.11	Results: Q_{stress}=138.9kVA,
	L_r, L_i [μH]	13.75, 13.27			D_{stress}=181 8kVA, P_{out}=14.98 kW
5	V_o [volt]	968.9	P_{out} *kW*	7.15	minimize *%THDI*
	F_s [kHz]	39.14	Q_{stress} *kVA*	193.4	Result:
	C_r [μF]	0.274	D_{stress} *kVA*	175.7	*%THDI* = 5.52
	L_r, L_i [μH]	8.834, 14.75	*SUF*	0.037	
6	V_o [volt]	884.0			minimize Q_{stress}+2(%THDI)
	F_s [kHz]	39.14	P_{out} *kW*	10.43	Results:
	C_r [μF]	0.271	D_{stress} *kVA*	175.5	Q_{stress} = 141.7 kVA
	L_r, L_i [μH]	13.75, 15.0	*SUF*	0.074	*%THDI* = 6.44