A Current Sharing Circuit for the Parallel Inverter

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Abstract - The parallel inverter is popularly used because of its fault-tolerance capability, high-current outputs at constant voltages and system modularity. The conventional parallel inverter usually employs active and reactive power control or frequency and voltage droop control. However, these approaches have the disadvantages that the response time of parallel inverter control is slow against load and system parameter variation to calculate active, reactive power, frequency and voltage. This paper describes a novel control scheme for power equalization in parallel-connected inverter. The proposed scheme has a fast power balance control response, a simplicity of implementation, and inherent peak current limiting capability since it employees an instantaneous current/voltage control with output voltage and current balance and output voltage regulation. A design procedure for the proposed parallel inverter controller is presented. Furthermore, the proposed control scheme is verified through the experiment in various cases such as the system parameter variation, the control parameter variation and the nonlinear load condition.

Ⅰ. INTRODUCTION

The parallel operation of the modularized small power UPS (inverter) has advantages in the cost and maintenance effective views compared with the single unit operation of a high power inverter.[1] However, the circulation current excusing in the parallel inverter modules results in damage of power semiconductors in the parallel inverter.[2, 3] Furthermore, the output current of the parallel inverter is internally dissipated between parallel-connected inverters, and the output voltage regulation causes the inverter switching interference and the output voltage oscillation.[4, 5, 6]

In this paper, the instantaneous voltage/current control for parallel inverter is proposed to eliminate these problems. The proposed parallel inverter controller employs the current share bus, the instantaneous current controller and the instantaneous voltage controller. The current share bus extracts the highest output current Imax among the parallel inverter output currents after feeding the output currents of the modules. Furthermore, the highest output current Imax of the current share bus is subtracted from the output currents of each parallel inverter module and the subtraction result provides the current deviation I expressing the circulation current. The proposed instantaneous voltage/current controller of the parallel inverter quickly eliminates the current deviation I and provides the function of the power balance between parallel inverter modules. At the same time, the digital PLL(Phase Locked Loop) is utilized to achieve synchronization between the outputs of each parallel inverter module. As a result, the digital PLL eliminates the circulation current caused by the phase difference of output voltages in the parallel inverter. The operation principle and simulation results are described in the Chapter Ⅱ and the Chapter Ⅲ. The all instantaneous current and voltage controller and the digital PLL are implemented by ADSP21061 DSP(Digital Signal Processor). Finally, the external view of the proposed parallel inverter module and experimental results are shown in chapter Ⅳ. The experimental results are presented to confirm the proposed current share bus control and instantaneous voltage/current control scheme.

Ⅱ. Current Control for Parallel U.P.S Output Power Equalization

The operation of the current-controlled parallel UPS with balanced power distribution can be studied by considering the equivalent circuit as shown in Fig.1. The autonomous current controlled parallel UPS ensures power balance operation. In this scheme, the power balance control has two current control loop and one voltage control loops in order to grantee the power balance between parallel UPS.

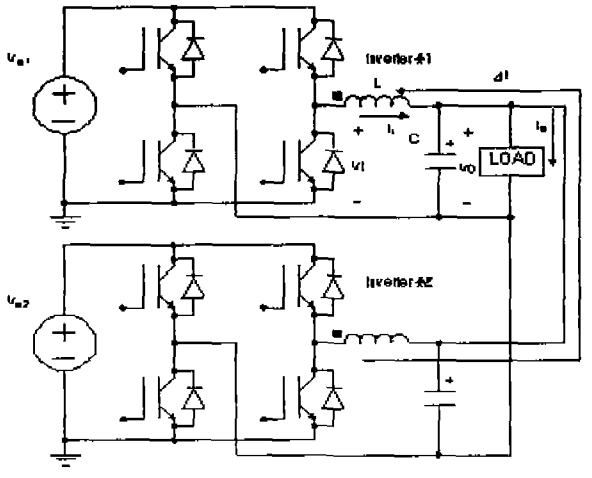

Fig. 1 Block Diagram of the Parallel Inverter Module

1. Parallel Inverter Module Modeling

The inverter switching frequency does not heavily affect on the inverter dynamics of the fundamental frequency since the switching frequency is even hundred times more than the fundamental frequency. Therefore, the parallel connected inverter module can be simplified as shown in the Fig. 2. In the Fig. 2, Z describes all kinds of loads including linear and nonlinear load and the circulation current directly affects the load current, the inductor current and the IGBTs. To eliminate the circulation current, the current share bus and the instantaneous voltage/current controller are proposed in the next section.

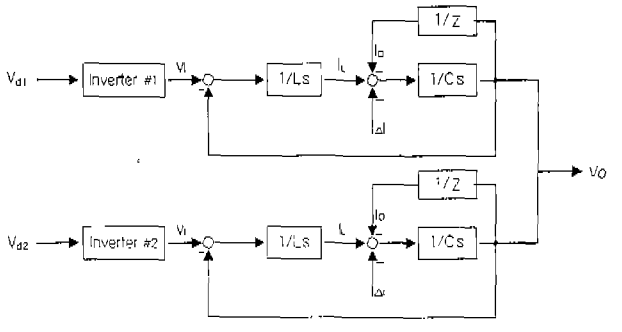

Fig. 2 Parallel Inverter Block Diagram

2. Circulation Current Dynamic Characteristics

First, the time and frequency domain analysis of the parallel inverter modules is carried out to analyze the circulation current characteristics. The transfer functions for the output voltage and the circulation current can be expressed as;

$$\frac{Vo(s)}{Vi(s)} = \frac{1}{LCs^2 + (L/R)\,s + 1} \quad , \tag{1}$$

$$\frac{Vo(s)}{\Delta i(s)} = \frac{s}{LCs^2 + (L/R)\,s + 1} \quad , \tag{2}$$

Where L is filter inductance, C is filter capacitor, and R is load. If L=5(mH), C=10(F) and R=100(Ω) are chosen, the z-transform of (1) and (2) can be expressed as;

$$\frac{Vo(z)}{Vi(z)} = \frac{0.15z + 0.01}{z^2 - 1.9\,z + 0.96} \quad , \tag{3}$$

$$\frac{Vo(z)}{\Delta i(z)} = \frac{3.9z - 3.9}{z^2 - 1.9z + 0.96} \quad , \tag{4}$$

Note that the denominator of the voltage transfer function is coincided with the denominator of the current deviation transfer function. From this relationship, it is obvious that the compensating voltage for the circulation current is essentially added to the reference voltage Vi* of the voltage controller in order to eliminate the influence of the circulation current on the inverter output voltage as shown in Fig. 4. In Fig.3, the bode plot of the (4) is shown. This figure illustrates the circulation current heavily affects the output voltage on the fundamental frequency 60(Hz) and the switching frequency range.

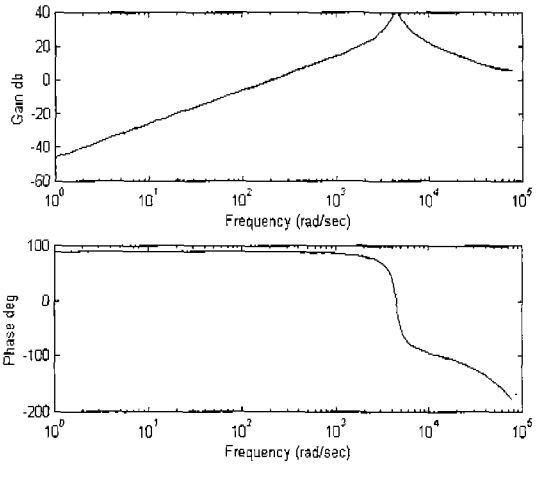

Fig. 3 Circulation Current Bode Plot

3. Parallel Inverter Controller Design

In this section, the instantaneous current, voltage and

parallel control scheme are proposed to implement the parallel inverter system with fast elimination ability for the circulation current. The overall parallel control loop is composed of three different control loops; the first one is internal current control loop, the second is external voltage control loop, and the third is parallel control loop to eliminate the circulation current. The operation principle of the proposed scheme is as follows. First, the capacitor current is controlled to maintain the capacitor voltage be sinusoidal shape under the varying load condition since the capacitor voltage has a linear relationship with the capacitor current.

Therefore, as the first step, the current control loop is designed. Secondly, the voltage controller is considered to improve the overall system dynamics. Finally, the parallel operation control is implemented with the current share bus in order to eliminate the circulation current and to guarantee the stable operation.

3.1. Current Control Loop

The load of the parallel inverter module can be considered as linear and nonlinear loads. The output voltage V_0, the output current I0 and the current deviation I described in Fig. 4.

Here, I_L* is produced from the output voltage controller as shown in Fig 7. (* means the reference value)

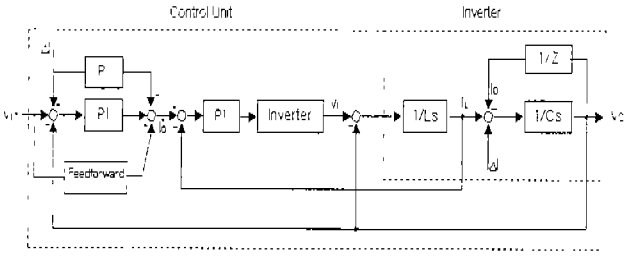

Fig. 4 Proposed Control System Block Diagram

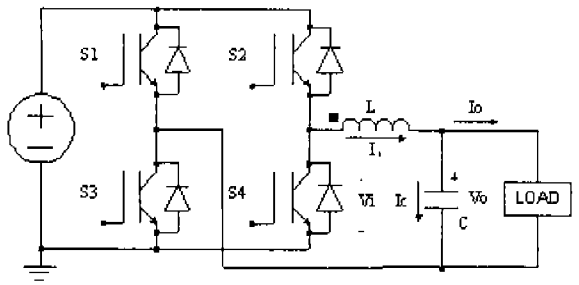

Fig. 5 Single Phase Inverter System

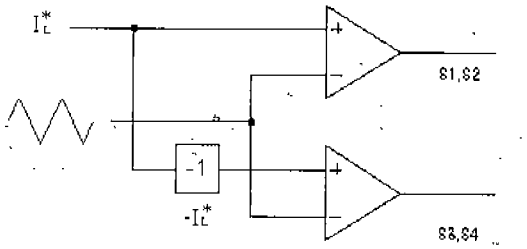

Fig. 6 Current Controller Block Diagram

Fig. 6 shows the current controller block diagram with the unipolar voltage switching strategy. The IGBT s1, s2 and s3, s4 are controlled separately by comparing Vtri with I_L^* and I_L* respectively. If the current reference I_L^* is bigger than Vtri, IGBT s1 be on-state and IGBT s2 be off-state. On the opposite condition IGBT s1 be off state and IGBT s2 be on state. IGBT s3 and s4 can be operated on the same condition with the reference $-I_L$*

3.2. Voltage Controller

The voltage controller of the parallel inverter module is shown in Fig. 7. Here, the reference voltage of the parallel inverter output can be expressed as;

$$V_i^* = V^* \cdot \sin(\omega t) \quad , \tag{5}$$

Where V* is the peak value and is the angular frequency. The reference voltage Vi* is subtracted from the sensed voltage and circulation current I obtained from the voltage sensor and the current share bus respectively, and the subtracted result is fed to PI controller as shown in Fig. 7. The PI controller could decouple the common denominator component embedded in the (3) and (4). The differentiation of the capacitor voltage is equal to the current through the capacitor such as

$$I_c^* = \frac{dV_o^*}{dt} = (\omega C) \cdot \sqrt{2} \cdot V \cdot \cos(\omega t) \quad , \tag{6}$$

Here, the current deviation I is added with Ic* and Io as shown in Fig. 7. Finally, the reference current Io* is created by the summation of the Isum (Isum = I+Ic*-Io) and the PI voltage controller output IF.

3.3. Parallel Inverter Controller

The disagreement in the control parameters and system parameters between parallel inverter modules produce the large circulation current and unbalanced power flow

between parallel connected inverters. Furthermore, the output voltage regulation of the parallel inverter causes the inverter switching interference and the output voltage oscillation. The proposed parallel inverter controller employs the current share bus, the instantaneous current controller and the voltage controller to solve these problems. The current share bus is designed to be blunted against the noise and the current share bus output is fed to the current controller and the voltage controller as shown in Fig. 6 and Fig. 7. The current share bus as shown in Fig. 9 extracts the highest output current Imax among the output currents of the parallel inverter. According to the Conduction State of diodes, the Imax is shown up the output node c in Fig. 9. The conduction state of + conduction diode (d1, d3) is decided by the current peak values of the Io1 and Io2. After competing between the Io1 and Io2 , the bigger current is coming up the node a. At the same story, the negative bigger current is coming up the node b depending on the conduction state of the-conduction diode (d2, d4). The outputs of node a and node b are added on the output terminal (node c) of the current share bus. Furthermore, the highest output current Imax is subtracted from the output currents (Io1, Io2) of each parallel inverter module as shown in Fig. 8. The subtraction results, the current deviation I, is fed to the current controller, the voltage controller, and the parallel inverter controller as shown in Fig. 6 and Fig. 7 and Fig. 8. The circulation current could be nullified by the current controller and the voltage controller as described in the previous section.

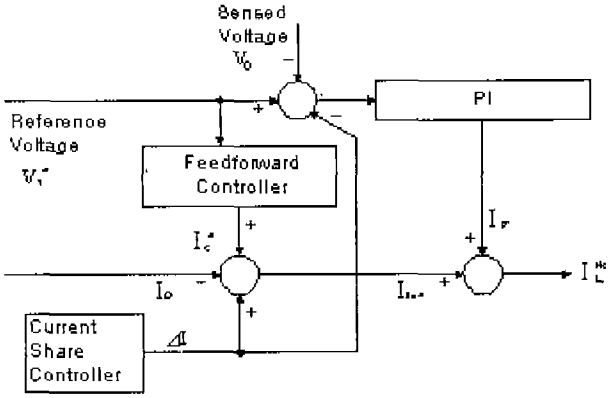

Fig. 7 Voltage Controller Block Diagram

IV. SYSTEM CONFIGURATION AND EXPERIMENTAL RESULTS

1. System Configuration

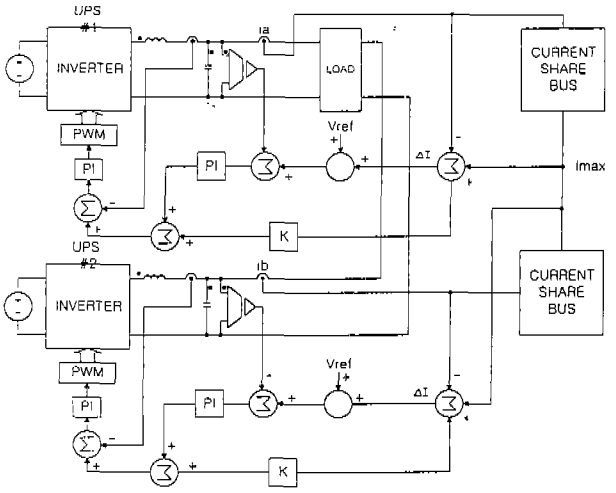

Fig. 8 Parallel Inverter controller

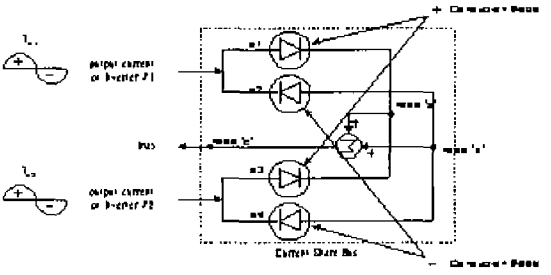

Fig. 9 Connection Diagram of Current Share Bus

Fig. 10 and Fig. 11 shows the system block diagram and the external view of the manufactured 1(kW) parallel inverted system. The parallel inverter is composed of power unit, sensor unit, controller and protection unit as shown in Fig.10.

2. Experimental Results

The experiment has been carried out to investigate the performance of the proposed scheme. The experimental conditions are classified as following two different modes to address the circulation characteristics.

- Parallel Mode Operation without the Current Share Bus Control
- Parallel Mode Operation with the Current Share Bus Control

2.1 Parallel Mode Operation without the Current Share Bus Control

In this section, the experiment without the current share bus has been carried out under various load conditions. Fig.12(a) shows the output current transient

response without current share bus control. The load is increased from 30(W) to 1,000(W) after 20(msec). Fig. 12(b) shows the output current waveforms under the steady state with 700(W) load. It can be seen that each inverter output current has different shape even if the peak values of each output current are same.

To check the output current deviation between two inverters, the circulation current is measured as shown in Fig.12(c). Each inverter output current measured under the nonlinear load condition (100W) is depicted As shown in Fig. 13(a), a difference between two currents are drastically increased compared with linear load as shown in Fig. 12(b). Fig. 13(b) shows that the 100(W) nonlinear load draws the circulation current as same as the 1(kW) linear load.

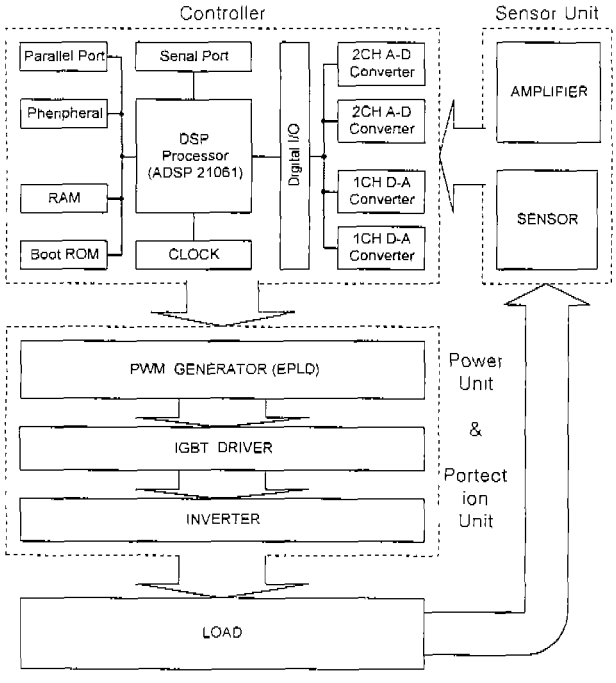

Fig. 10 Parallel Inverter System Block Diagram

2. Parallel Mode Operation with Current Share Bus Control.

In this section, the experiment with the current share bus has been carried out under various load conditions. Fig.14(a) shows the output current transient response with current share bus control. The load is increased from 30(W) to 1,000(W) after 14(msec). It shows that the output current reaches the steady state within a half period from the load change instant. Fig. 14(b) shows the output current waveforms under the steady state with 700(W) load. It can be seen that each inverter output current has exactly same shape even if there is the load variation at 14(msec). The circulation current is measured as shown in Fig.14(c). Here, the circulation current is drastically decreased compared with the circulation current as shown in Fig. 12(c).

Each inverter output current measured under the nonlinear load condition (100W) is depicted as shown in Fig. 15(a). Furthermore, the circulation current under the condition is shown in Fig. 15(b). It shows that the 100(W) nonlinear load draws the negligible circulation current.

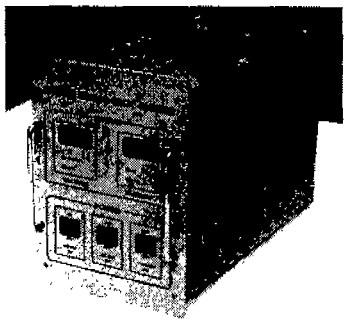

Fig. 11 External View of the Manufactured 1(kW) Parallel Inverter System

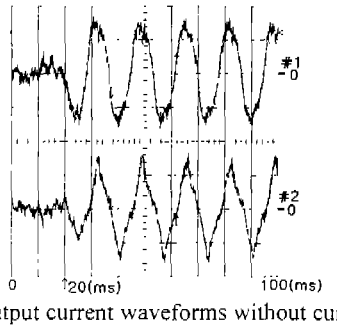

Fig. 12(a) Output current waveforms without current share bus control
(6A/div 10ms/sec)

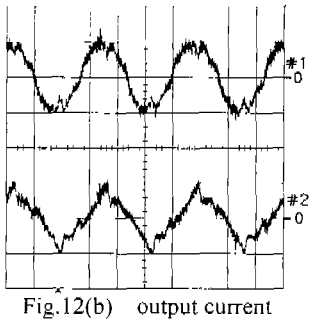

Fig.12(b) output current waveforms under 700(W) linear load
(6A/div 5ms/sec)

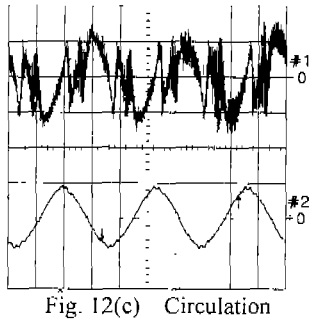

Fig. 12(c) Circulation current(#1) and output voltage(#2) under 700(W) linear load
(0.5A/div 300V/div 5ms/sec)

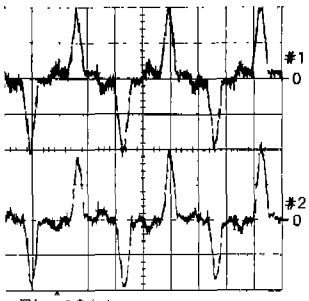

Fig. 13(a) output current waveforms under 100(W) nonlinear load (6A/div 5ms/sec)

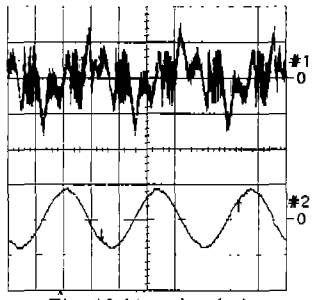

Fig. 13(b) circulation current(#1) and output voltage(#2) under 100(W) nonlinear load. (0.5A/div 300V/div 5ms/sec)

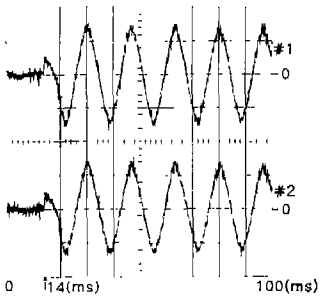

Fig.14(a) output current waveforms with current share bus control (6A/div 10ms/sec)

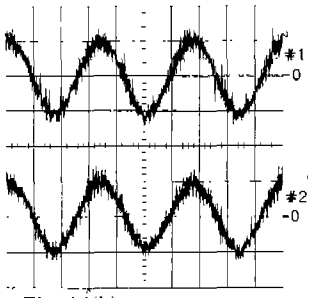

Fig. 14(b) output current wave forms under 700(W) linear load. (6A/div 5ms/sec)

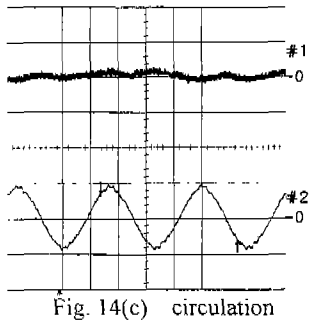

Fig. 14(c) circulation current(#1) and output voltage(#2) under 700(W) linear load (0.5A/div 300V/div 5ms/sec)

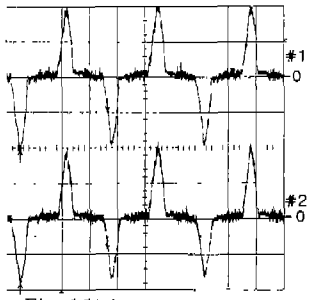

Fig. 15(a) output current waveforms under 100(W) nonlinear load (6A/div 5ms/sec)

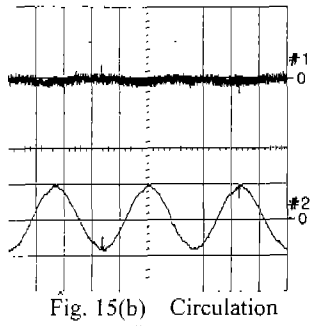

Fig. 15(b) Circulation current(#1) and output voltage(#2) under 100(W) nonlinear load (0.5A/div 300V/div 5ms/sec)

V. CONCLUSION

In this paper, a novel parallel inverter module scheme eliminating the circulation current is proposed. By employing the proposed current share bus and the instantaneous voltage/current control, the circulating current can be quickly nullified under the various nonlinear and linear loads. The primary advantage of the proposed scheme is that the instantaneous current sharing controller forces the output current deviations of each inverter to be zero in every switching period. Furthermore, the output reference of the voltage controller is instantaneously to eliminate the unbalanced power. This results in superior power balance performance for parallel operation.

The proposed scheme has been verified through out various experiments. The experimental results show that the T.H.D of the output voltage is less than 2.37(%) even under the worst load condition.

VI. REFERENCES

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