COMMON-MODE VOLTAGE PULSE CANCELLATION METHOD BASED ON SPACE-VECTOR PWM IN CONVERTER-INVERTER SYSTEM

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Abstract - **This paper proposes the advanced PWM method that can reduce common-mode voltage in three-phase PWM converter-inverter system. By the proper distribution of the zero-voltage vector of inverter, it is possible to cancel out a common-mode voltage pulse in a sampling period. Since the proposed PWM method maintains the effective-voltage vector, it does not affect the control performance of converter-inverter system. Without any extra hardware, overall common-mode voltage can be decreased by one-third compared with conventional PWM scheme.**

I. INTRODUCTION

Numerous problems accompanied by common-mode voltage due to high-speed pulse width modulation have been reported in many AC machine drive applications; leakage current flowing through the stray capacitance between motor winding and frame[1,2], radiated and conducted EMI(Electromagnetic Interference) problem [3,4], bearing current and shaft voltage[5,6], breakdown of motor insulation and so on. Thus, concerns about these problems have been increased and many studies for reducing the common-mode voltage have been progressed all over the world. Some works focused on the design of common-mode choke/transformer[1,2] or the fourth leg in conventional converter[7,8]. Since these methods require additional hardware, the drawbacks of increase in inverter weight and volume or complexity in its control are unavoidable. And the filter or transformer parameters should be redesigned according to various applications. In recent, researches for reduction of the common-mode voltage using PWM scheme came to the front[9,10]. However, in these methods, large ripples in motor currents have to be encountered due to the absence of zero-voltage vector, and there exists a limitation of modulation index because of synthesis of zero-voltage vector using effective voltage vectors.

This paper proposes a PWM method that can reduce common-mode voltage in three-phase PWM converter/inverter system. By shifting the effective-voltage vector of inverter in a sampling period, it is possible to eliminate a common-mode voltage pulse. Hence, overall common-mode voltage can be reduced to two-third compared with three-phase symmetric PWM scheme case. The proposed PWM method maintains the effective-voltage vector and just manipulates the zero-voltage vector, so that it does not aggravate the control performance of converter/inverter system. And it can be easily implemented in software without any extra hardware.

II. RELATIONSHIP BETWEEN COMMON-MODE VOLTAGE AND SWITCHING FUNCTION

Fig. 1 shows three-phase PWM boost converter and inverter system widely used in ac machine drives. The voltage-current equations for converter-inverter system can be given by (1) for source side and (2) for load side.

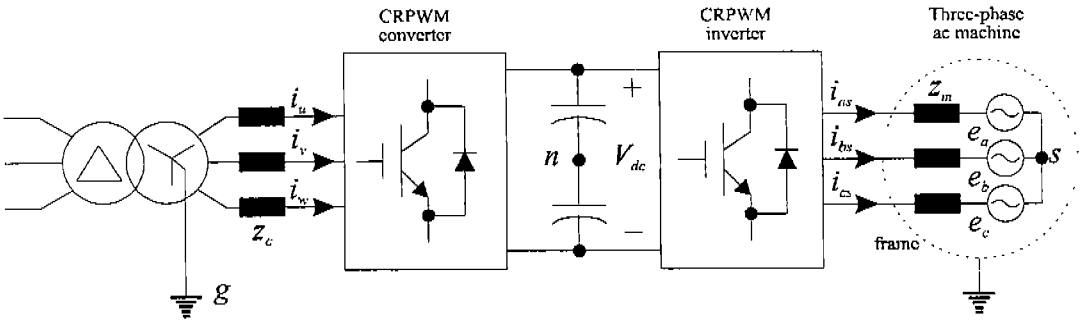

Fig. 1. Three-phase PWM converter-inverter system for ac machine drive(*g*:grounding point, *s*:stator neutral).

$$\begin{cases} v_{ug} = -z_c i_u + e_u \\ v_{vg} = -z_c i_v + e_v \\ v_{wg} = -z_c i_w + e_w \end{cases} \quad \textit{for source side} \qquad (1)$$

$$\begin{cases} v_{as} = z_m i_{as} + e_a \\ v_{bs} = z_m i_{bs} + e_b \\ v_{cs} = z_m i_{cs} + e_c \end{cases} \quad \textit{for load side} \qquad (2)$$

Assuming the balanced three-phase source and load, and taking the virtual mid-point of dc bus, 'n', the voltage difference between ground, 'g' and 'n', v_{gn} can be described as (3). In the same way, the voltage difference between 'n' and stator neutral, 's' can be described as (4).

$$v_{gn} = \frac{v_{ug} + v_{vg} + v_{wg}}{3} \qquad (3)$$

$$v_{sn} = \frac{v_{as} + v_{bs} + v_{cs}}{3} \qquad (4)$$

Since, generally, the neutral point of the star-connected three-phase source is connected to the ground('g' in Fig. 1), and the motor frame is also connected to the same ground, the common-mode voltage in this system corresponds to the voltage difference between the ground and the stator neutral('s' in Fig. 1). From (3) and (4), the common-mode voltage, v_{sg}, can be determined as (5)

$$\begin{aligned} v_{sg} &= v_{sn} - v_{gn} \\ &= \frac{(v_{as} + v_{bs} + v_{cs}) - (v_{ug} + v_{vg} + v_{wg})}{3} \end{aligned} \qquad (5)$$

Using the switching functions of converter and inverter, s_i, ($i = a,b,c,u,v,w$), v_{sg} can be therefore determined as (6), consequently

$$v_{sg} = \frac{V_{dc}}{3}\left[(s_a + s_b + s_c) - (s_u + s_v + s_w)\right] \qquad (6)$$

From (6), it can be known that the both the switching states of the converter-inverter and dc-bus voltage, V_{dc} decide the common mode voltage, regardless of the motor impedance.

Even if there are eight states available for the output voltage vector according to eight switching functions of both the converter and the inverter as illustrated in Fig. 2, possible v_{sg} has seven states(0, $\pm V_{dc}/3$, $\pm 2V_{dc}/3$, $\pm V_{dc}$), which are summarized in Table 1. From Table 1,

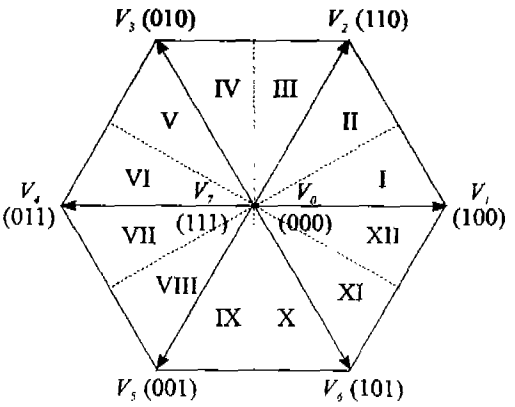

Fig. 2. Voltage vectors according to switching states of converter and inverter in space vector plane, and sectors(I~XII).

TABLE 1. COMMON MODE VOLTAGE ACCORDING TO OUTPUT VOLTAGE VECTORS OF CONVERTER AND INVERTER

		Output voltage vector of Inv.			
		V_1, V_3, V_5	V_2, V_4, V_6	V_0	V_7
Output voltage vector of Conv.	V_1, V_3, V_5	0	$V_{dc}/3$	$-V_{dc}/3$	$2V_{dc}/3$
	V_2, V_4, V_6	$-V_{dc}/3$	0	$-2V_{dc}/3$	$V_{dc}/3$
	V_0	$V_{dc}/3$	$2V_{dc}/3$	0	V_{dc}
	V_7	$-2V_{dc}/3$	$-V_{dc}/3$	$-V_{dc}$	0

it can be seen that v_{sg} changes by $V_{dc}/3$ every switching of converter and inverter, and has V_{dc} peak when the different two zero voltage vectors are applied. Dc-bus voltage of v_{sg} can be avoided if the synchronism between starting point of switching for both converter and inverter with same switching frequency is guaranteed.

III. PWM STRATEGY ELIMINATING A COMMON-MODE VOLTAGE PULSE

Fig. 3 shows the relationship between the switching functions of converter-inverter and the common-mode voltage when using conventional three-phase symmetric PWM method. It can be known that the disagreement between the switching points of converter and inverter brings out the common-mode voltage pulses. Six switching actions of converter and inverter occur in a sampling period, T_Z, as shown in Fig. 3. Thus, three common-mode voltage pulses are generated, of which magnitude is equal to $V_{dc}/3$. Since the synchronism of the converter and inverter control is confirmed, there exists no common-mode voltage pulse of $\pm V_{dc}$. When the magnitude of the active space vector of the inverter is

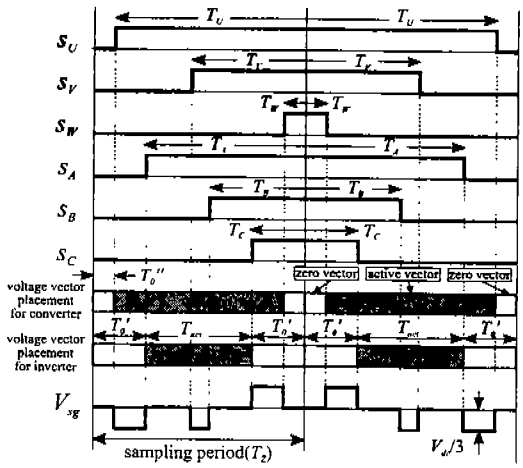

Fig. 3. Switching functions of converter and inverter, and common-mode voltage using conventional symmetric SVPWM.

very small, there can exist the common-mode voltage of $2V_{dc}/3$.

This paper proposes the PWM method that can eliminate one common-mode voltage pulse in a sampling period. Since the common-mode voltage pulse results from the disagreement between the switching points of the converter and the inverter, it is possible to eliminate one common-mode voltage pulse in a sampling period by shifting an inverter switching point and aligning this to one of the converter switching points.

There can exist two kind of the switching alignment method:

- Shifting the inverter switching point of the largest pole voltage reference and aligning this to the converter switching point of the largest pole voltage reference (*Method I*).
- Shifting the inverter switching point of the smallest pole voltage reference and aligning this to the converter switching point of the smallest pole voltage reference (Method II).

In method I, the active space vector of inverter is shifted left by ΔT. As shown in ON-sequence of Fig. 4, the starting points of the active space vectors for both converter and inverter are aligned, making the zero space vector time for inverter $T_0 (= T_0' - \Delta T)$ be equal to the zero space vector time for converter T_0''. Then the first one of common-mode voltage pulse train is eliminated compared to v_{sg} in Fig. 3. In method B, the active space vector for inverter is shifted right by ΔT, and the end points of the active space vectors are aligned, making $T_0 (= T_0' + \Delta T)$ be equal to T_0'', as shown in Fig. 5. Then the last one of common-mode voltage pulse train is eliminated.

ΔT can be computed as (7). Since the modulation index of the converter is generally larger than that of the inverter in variable ac machine drives, ΔT is positive. If ΔT is negative, the proposed reduction method can be realized by shifting the active space vector of the converter rather than the active space vector of the inverter.

$$\Delta T = T_0'' - T_0' = T_0'' - (T_Z - T_{act})/2 \qquad (7)$$

In Figs. 4 and 5, note that the number of generated common-mode voltage pulses is reduced to **two**, although six switching actions of converter-inverter occur in T_Z. Compare this with **three** of the conventional symmetric SVPWM. Hence, using the proposed reduction method, the leakage current produced by high dv/dt common-mode voltage pulses can be reduced to two third of the conventional method.

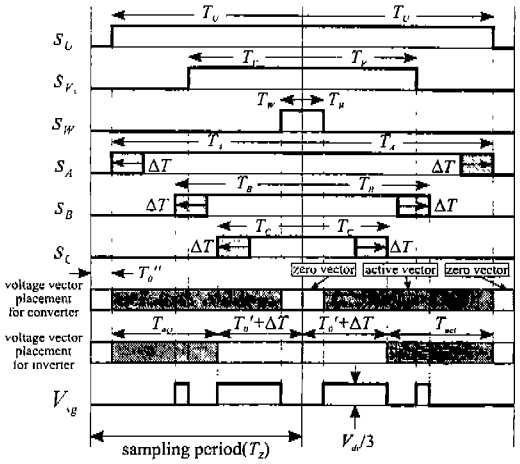

Fig. 4. Switching functions of converter and inverter, and common-mode voltage using proposed reduction method I.

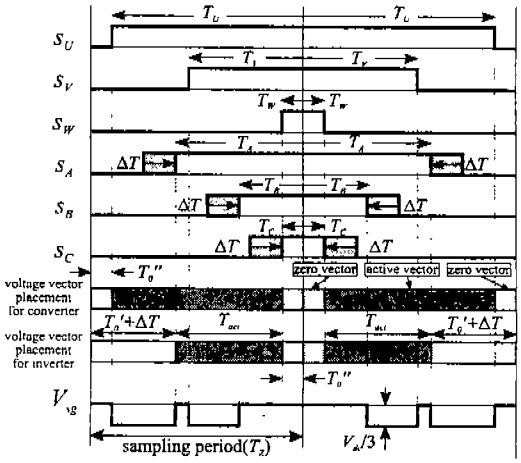

Fig. 5. Switching functions of converter and inverter, and common-mode voltage using proposed reduction method II.

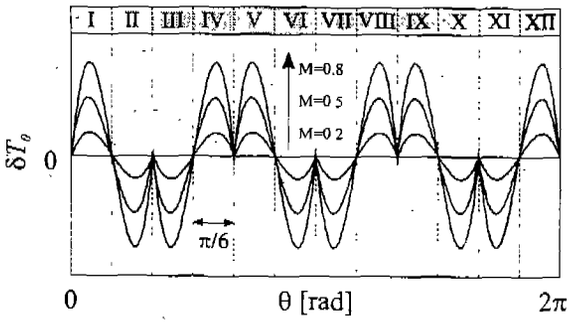

Fig. 6. Dependency of δT_0 on modulation index and angle.

IV. Shifting Active Space Vector and Rms Ripple Current of Three-Phase Load

The square rms of ripple current, I_{ripple}^2 depends on the placement of the zero space vector in a sampling period[11,12]. Thus, in the proposed method, I_{ripple}^2 can be increased compared to that of the symmetrical SVPWM. Since I_{ripple}^2 is given by a polynomial dependent to T_0, the optimal zero space vector time that provides minimum I_{ripple}^2 can be computed and defined as T_{0_opt}. The difference between the zero space vector time in conventional symmetric SVPWM, T_0' $(=(T_Z - T_{act})/2)$ and T_{0_opt} is defined as δT_0, and can be computed as (8).

$$T_0' - T_{0\_opt} = \frac{T_Z}{V_{dc}} \cdot \frac{(V_\alpha^* + V_\gamma^*)(2V_\alpha^* + V_\gamma^*)(V_\alpha^* + 2V_\gamma^*)}{4(V_\alpha^{*2} + V_\alpha^* V_\gamma^* + V_\gamma^{*2})} \equiv \delta T_0 \tag{8}$$

where, V_α^* and V_γ^* are the largest and the smallest one among voltage references of the inverter, respectively.

The dependence of δT_0 on modulation index, M, and inverter voltage angle, θ, is depicted in Fig. 6. If $\delta T_0 > 0$, it can be concluded that method A is more effective than method B. If $\delta T_0 < 0$, method B is preferred to method A, in that the increase in I_{ripple}^2 due to the shift of the active space vector placement is minimized. From Fig. 6, the choice of the aligning method can be confirmed only by sector in which the reference voltage lies, regardless of the modulation index, and is presented in Table 2.

V. Experimental Results

In the experiments, the PWM boost converter controls dc bus voltage, V_{dc} as 370V, and 22kW induction machine is operated with constant V/f ratio. The sampling periods for both converter and inverter are 200μs, and are synchronized each other.

In Fig. 7, v_{gn}, v_{sn} and v_{sg} during T_Z are presented when using the conventional symmetric SVPWM. v_{gn} and v_{sn} denote the voltage difference between virtual ground, n and source ground and stator neutral, respectively. The virtual ground, n that can be realized by accessing the mid-point of the dc bus capacitor. v_{gn} and v_{sn} are $\pm V_{dc}/2$ when zero space vectors are applied, and $\pm V_{dc}/6$ for active space vectors. It can be easily found that there exist **three** common-mode voltage pulses according to converter and inverter switching states. In Fig. 8, it can be shown that the starting points of the active space vectors of the converter and inverter are aligned. Thus first common-mode voltage pulse is eliminated, and the number of generated common-mode voltage pulses is reduced to **two**, using the proposed reduction method.

IV. Conclusions

In this paper, the common-mode voltage in three-phase PWM converter-inverter system is defined according to the switching functions and analyzed. Based on the conventional SVPWM, the proposed method eliminates one common-mode voltage pulse in one sampling period by shifting the inverter active space vector and aligning this to that of the converter. Possible two methods are presented and the choice between two methods is confirmed according to the inverter output angle, minimizing the increase of rms ripple current.

With the help of the proposed reduction scheme, the number of generated common-mode voltage pulses can be reduced to **two**, compared with **three** of the conventional symmetric SVPWM method, so that overall

Table 2. Choice between method A or B minimizing the increase in I_{ripple}^2.

Sector	I	II	III	IV	V	VI	VII	VIII	IX	X	XI	XII
Method	A	B	B	A	A	B	B	A	A	B	B	A

dv/dt current can be decreased by one third. Since the proposed reduction method maintains the active space vector and redistributes the zero space vector, it does not aggravate the control performance of converter-inverter system. In addition, the proposed method can be easily implemented in software without any extra hardware.

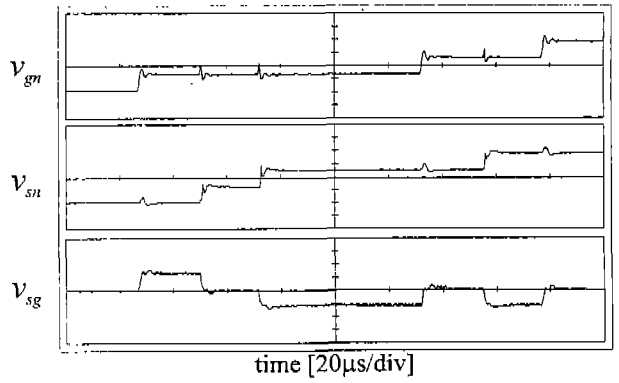

Fig. 7. Experimental results when using conventional Symmetric SVPWM(v_{gn} , v_{sn} , v_{sg} :100[V/div]).

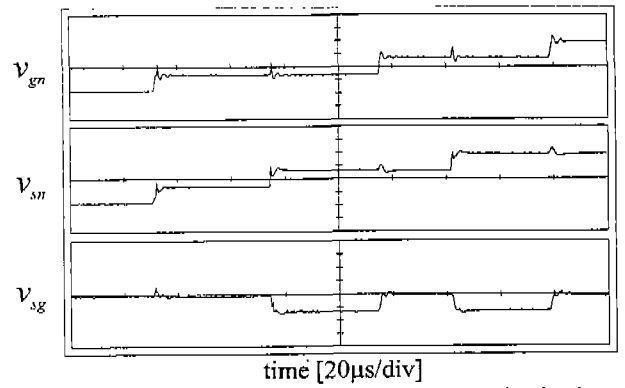

Fig. 8. Experimental results when using proposed reduction method(v_{gn} , v_{sn} , v_{sg} :100[V/div]).

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