A Novel SVPWM Strategy Considering DC-link Balancing for a Multi-level Voltage Source Inverter

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ABSTRACT - This paper proposes a SVPWM (space vector pulse width modulation) strategy for a multi-level voltage source inverter. This strategy is easily implemented as SPWM (sinusoidal pulse width modulation) and has the same DC-link voltage utilization as general SVPWM. The method to keep the voltage balancing of DC-link also is proposed by the analysis model of DC-link voltage fluctuation. The usefulness of the proposed SVPWM is verified through the simulation.

I. INTRODUCTION

To realize high power high efficiency DC-AC conversion, numerous multi-level inverter topologies such as diode clamped configuration, flying capacitor configuration and H-bridge configuration inverter have been proposed together with suitable control scheme [1]-[3]. The main advantages offered by these inverters can be summarized as:

- Achieving higher voltage rating by synthesizing a lot of lower partial dc voltage source.
- Solving voltage-sharing problem of series connected power devices.
- Reducing THD (total harmonic distortion) in output voltage waveform.
- Reducing electromagnetic interface problems by decreasing switching dv/dt stress.

Especially, in the field of high power variable speed application like traction and steel mill system, DCICs (diode clamped inverter configurations) have been widely used. The DCICs were derived from Neutral Point Clamped inverter given by Nabae et al [1]. After that time, DCMLIs (diode clamped multi-level inverter configurations) were developed [4],[5].

As the technique to control the inverter, Pulse Width Modulation is established a standard of nowadays. A large variety of the PWM strategies has been researched and proposed. In these PWMs, the space vector PWM has excellent dc-link voltage utilization and low current ripple. The sine-triangle PWM is widely employed in an application because of easy implementation[6]. Many papers using SVPWM in diode clamped three-level inverter has been published. However, it is very difficult that SVPWM is employed in DCMLICs because of complex implementation algorithm with 3 or 4 stages[7]. Moreover, DC-link voltage balancing, which certainly is under consideration with realization of DCMLIs, adds an extra weight on difficulty in using SVPWM.

We proposed the SVPWM strategy for DCMLIs in this paper. It is easily implemented by introducing a new approach that space vector PWM is equal to sinusoidal PWM adding proper voltage offset. And, the analysis method of the link potential fluctuation by the reference voltage and phase current in the inverter is described. The DC-link voltage fluctuation can be controlled by this analysis method. The usefulness of the proposed SVPWM is verified through the simulation.

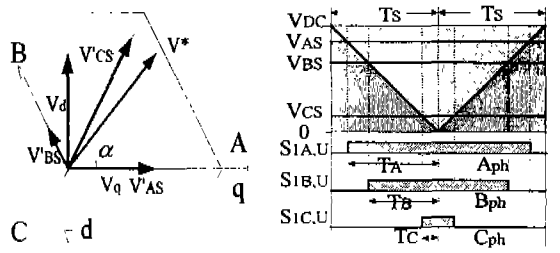
II. PRINCIPLE OF PROPOSED SVPWM

A. Problems of conventional SVPWM

In the SVPWM, generally, the reference voltage vector is realized on average basis by using nearest three vectors in order to minimize the harmonic components of the output line-to-line voltage. The durations of each voltage vector can be calculated by vector calculation[8]. It means that the change of reference voltage vector results in a different vector calculation and the location of the reference voltage vector has to be identified. In DCMLICs, the number of vector calculation equation, generally, is $3(N-1)^2$. And, these vector calculation equations have the terms of sin or cos function, which is not suitable for digital controller such as DSP, MCU etc. Additionally, the durations of each voltage vector is not real on-off time of power device. So, the durations of each voltage vector have to be converted into the real on-off time of power device[7].

B. Realization of novel SVPWM in two-level inverter

If a reference voltage vector V* is placed on any region of space voltage presentation, each phase voltages V_{AS}', V_{BS}' and V_{CS}' (defined as "imaginary



(a) (b)

Fig. 1. Definition of imaginary phase voltages (a) and proposed space vector PWM (b) in two-level inverter.

phase voltage") are derived from reference voltage vector Vd, Vq of the stationary reference frame d-q axis as shown Fig. 1 (a). The imaginary phase voltages are obtained by (1).

$$\begin{bmatrix} V'_{AS} \\ V'_{BS} \\ V'_{CS} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -1/2 & +\sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} |V^*| cos\alpha (= V_q) \\ |V^*| sin\alpha (= V_d) \end{bmatrix} \quad (1)$$

The imaginary phase voltages have the information of line-to-line voltages being seen by the machine. The addition of a dc offset voltage (denoted as "V_{OFFSET}") to each imaginary phase voltage does not change this information. So, we can obtain the same reference voltage vector in the space voltage presentation though a dc offset voltage is added to each imaginary phase voltages[9]. Additionally, If all imaginary phase voltages with addition of a dc offset voltage are located from 0 to DC-link voltage, the instant, when these all imaginary phase voltages change from 0 to DC-link voltage or the contrary, is the same as that of real on-off time of switching devices. If each imaginary phase voltages with addition of a dc offset voltage are defined as effective phase voltage (denoted as "V_{AS}, V_{BS} and V_{CS}"), it can be written:

$$\begin{aligned} V_{AS} &= V'_{AS} + V_{OFFSET} \\ V_{BS} &= V'_{BS} + V_{OFFSET} \\ V_{CS} &= V'_{CS} + V_{OFFSET} \end{aligned} \quad (2)$$

The changing instants of effective phase voltage (denoted as "T_A, T_B and T_C") and dc offset voltage are also expressed as (3) and (4).

$$\begin{aligned} T_A &= \frac{V_{AS}}{V_{DC}} \cdot T_S \\ T_B &= \frac{V_{BS}}{V_{DC}} \cdot T_S \\ T_C &= \frac{V_{CS}}{V_{DC}} \cdot T_S \end{aligned} \quad (3)$$

$$V_{OFFSET} = \frac{1}{2} \cdot (V_{DC} - V_{MAX} - V_{MIN}) \quad (4)$$

Where V_{DC} is dc link voltage; V_{MAX}, V_{MIN} is a maximum, minimum voltage of imaginary phase voltages;

The addition of dc voltage offset makes imaginary phase voltages to have central value from 0 to V_{DC} as shown Fig. 1 (b). It means that this PWM method generates symmetrical switching pulse pattern and

Table 1. Switching States in three-level inverter (X=A,B,C)

Switching State	$S_{2X,U}$	$S_{1X,U}$	$S_{2X,L}$	$S_{1X,L}$	V_X
2	ON	ON	OFF	OFF	V_{DC}
1	OFF	ON	ON	OFF	$V_{DC}/2$
0	OFF	OFF	ON	ON	0

minimizes the ripple of phase currents. Practically, T_A, T_B and T_C can be easily obtained to compare all effective phase voltages with the triangle waveform which has two times of sampling time Ts period as shown Fig. 1 (b). This method is very close to sine-triangle PWM. In three-phase voltage source inverter, when each effective phase voltage is greater than the triangle waveform, the upper power device control signal of each arm becomes high, causing the upper switching devices to turn on. The relation of upper power device and lower power device is complement. Therefore, lower switching device is off. Otherwise, the upper switching device is off and lower is on.

C. Realization of novel SVPWM in DCMLIs

In two-level inverter, the method to realize the voltage Vxs is that V_{DC} generates during $V_{XS}/V_{DC} \cdot T_S$ of sampling time T_S and 0 generates during the rest of sampling time T_S. However, in DCMLIs, the number of inverter phase voltage to generate is N. Therefore, we can utilize many inverter phase voltages.

To explain extension of proposed SVPWM for DCMLIs, three-level inverter is taken an example. Fig. 2 shows a schematic diagram of a three-level inverter. Each phase of this inverter consists of two clamping diodes, four main power devices and four freewheeling diodes. Table 1 shows the switching states of three-level inverter. Fig. 3 (a) shows the presentation of the space voltage vector. This space voltage vector consists of six regions. Each region can be divided into four smaller regions 1,2,3 and 4. Fig 3 (b) shows the space vector diagram of all switching states.

If a reference voltage vector is placed on the any region, all of the imaginary phase voltages, dc offset voltage and effective phase voltages are obtained by (1), (2) and (4) repectivly. To utilize three switching states, the region of dc link voltage is divide into two portions. It is realized that two triangle waveforms of $V_{DC}/2$ magnitude is introduced as shown Fig. 4.

Fig. 4 shows that the phase voltage V_{XS}, which realized by introducing two triangle waveforms

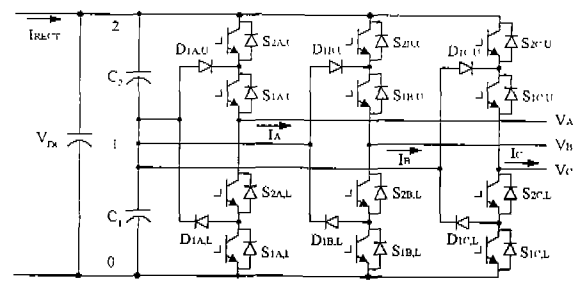
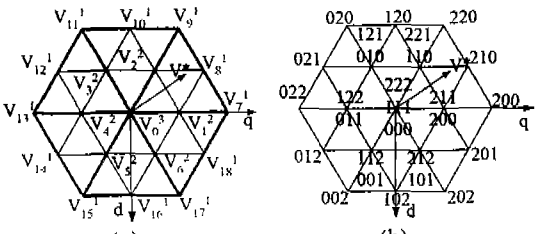
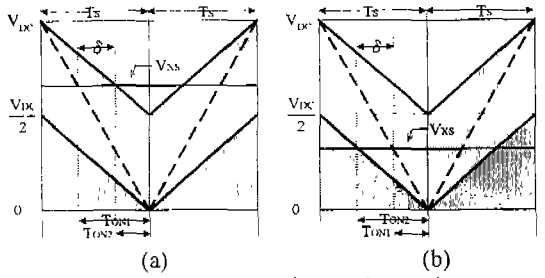


Fig. 2. Schematic diagram of a three-level inverter.



(a) (b)

Fig. 3. Voltage vectors (a) and switching states (b) in space vector presentation of three-level inverter.



(a) (b)

Fig. 4. Realization of phase voltage when $V_{XS}>V_{DC}/2$ (a) and $V_{XS}<V_{DC}/2$ in three-level inverter.

(indicated as solid-line), is equal to that realized by using only one triangle waveform (indicated as dashed-line). Fig. 4 (a) is that V_{XS} is greater than one half of dc link voltage ($V_{DC}/2$). Fig. 4 (b) is on the contrary. The symbols presented in Fig. 4 are as following

- T_{ON1} : on-time duration when one triangle waveform is used.
- T_{ON2} : on-time duration when two triangle waveforms are used.
- δ : time difference between T_{ON1} and T_{ON2}.

In Fig. 4 (a), T_S-T_{ON1} is equal to δ. The phase voltage V_{XS} is realized by the method that one half of dc link voltage ($V_{DC}/2$) generates during the ($2\cdot\delta$) of sampling time T_S and dc link voltage (V_{DC}) generates during the rest time of sampling time (T_S-$2\cdot\delta$). On the contrary, in Fig 4 (b), T_{ON1} is equal to δ. Therefore, the phase voltage V_{XS} is realized that zero voltage is generated during (T_S-$2\cdot T_{ON1}$) of sampling time and ($V_{DC}/2$) generated during the rest of sampling time ($2\cdot T_{ON1}$). The realization of the phase voltage V_{XS} can be represented as:

$$V_{XS} \geq \frac{V_{DC}}{2} \;:\; V_{DC}\cdot\left(\frac{T_{ON}-\delta}{T_S}\right)+\frac{V_{DC}}{2}\cdot\frac{2\cdot\delta}{T_S}$$
$$V_{XS} \leq \frac{V_{DC}}{2} \;:\; \frac{V_{DC}}{2}\cdot\frac{2\cdot T_{ON}}{T_S} \qquad (5)$$

The method to obtain real on-off time of power device also is similar to sine-triangle PWM for three-level inverter. The upper triangle waveform determine the real on-off instant of $S_{2X,U}$(X=A,B,C) power device and lower triangle waveform determine the real on-off instant of $S_{1X,U}$ power device. The relation of $S_{2X,U}$($S_{1X,U}$) and $S_{2X,L}$($S_{1X,L}$) is complement.

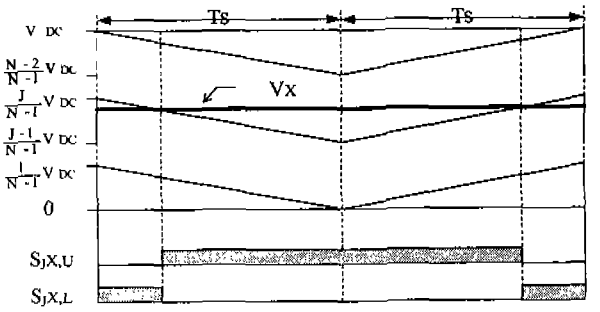


Fig. 5. Proposed space vector PWM in DCMLIs(X=A,B,C).

Fig. 5 shows the disposition of effective phase voltage and triangle waveforms in DCMLIs. The number of triangle waveform is N-1. The J-th triangle waveform determine the real on-off instant of $S_{JX,U}$ and $S_{JX,L}$ switching devices. Therefore, the output phase voltage changes from $(J-1)\cdot V_{DC}/(N-1)$ to $J\cdot V_{DC}/(N-1)$ or the contrary. The change direction is obtained from the rising or falling sloop of the J-th triangle waveform[9].

III. DC-LINK VOLTAGE CONTROL METHOD

A. Approach of DC-link voltage balancing

In DCMLIs, the DC-link voltage is divided by (N-1) capacitors and each capacitor is composed of series connection construction. If voltage unbalancing occurs between each capacitors, the power devices used on DCMLIs are not guarantee safe operation and the line-to-line output voltage waveform has many harmonic components. Therefore, the balancing of DC-link voltage is important function, which determine the safety and efficiency of DCMLIs.

This unbalancing of DC-link voltage originate from the different charging or discharging time and path of each series-connected capacitor in according to switching state and load condition. If a reference voltage vector is placed on any region of space voltage presentation. the switching state and durations of itself corresponding to magnitude and direction of the reference voltage vector. This switching state makes a specific capacitor charge or discharge according to load condition. Therefore, the voltage of the specific capacitor increases or decreases.

In the standpoint of dc link voltage balancing, the addition of dc offset voltage with a equal magnitude to each effective phase voltage obtained by (2) change charging or discharging path and duration on capacitor. Therefore, in the proposed SVPWM, the fluctuation of DC-link voltage can be controlled by addition another dc offset voltage (denoted as "V_{BAL}") to effective phase voltage.

$$V_A = V_{AS} + V_{BAL} = V'_{AS} + V_{OFFSET} + V_{BAL}$$
$$V_B = V_{BS} + V_{BAL} = V'_{BS} + V_{OFFSET} + V_{BAL} \qquad (6)$$
$$V_C = V_{CS} + V_{BAL} = V'_{CS} + V_{OFFSET} + V_{BAL}$$

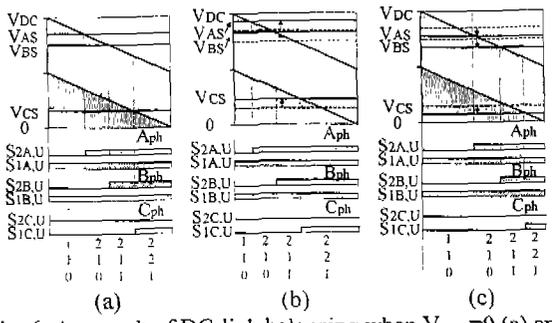


Fig. 6. Approach of DC-link balancing when V_{BAL}=0 (a) and V_{BAL}>0 (b) and V_{BAL}<0 (c) in three-level inverter.

Fig. 6 shows that correlation between dc offset voltage and charging or discharging duration of capacitor in three-level inverter. In Fig. 6 (a), when dc offset voltage is zero, the switching state 110 results in the charging or discharging path through lower capacitor C_1. The switching state 211 and 221 results in the charging or discharging path through upper capacitor C_2. When dc offset voltage is positive, duration T_{110} of switching state 110 decreases and duration T_{211}, T_{221} of switching state 221, 221 increases as shown Fig. 6 (b). It means that the charging or discharging time of upper capacitor C_2 is longer than that of lower capacitor C_1. In Fig. 6 (c), on the contrary, when offset voltage is negative, the charging or discharging duration of lower capacitor C_1 is longer than that of upper capacitor.

Therefore, if each capacitor voltage and load condition is recognized, DC-link voltage can be balanced by adding or subtracting appreciate dc offset voltage. In this paper, dc offset can be obtained by analysis model that is suitable proposed SVPWM as following paragraph. This approach can be extended to DCMLIs.

B. Analysis of link potential fluctuation

To control link potential fluctuation, new analysis method that is suitable for proposed SVPWM is devised. Firstly, in the following analysis, it is assumed that sampling frequency of reference voltage is enough high as compared with fundamental output frequency. Therefore, the phase (arm) currents of the three-level inverter can be considered as constant during sampling time. This assumption becomes more reasonable due to large inductive load of inverter.

Conceptually, the magnitude of effective phase voltages obtained (2) determines the time to flow the corresponding phase current of three-level inverter from or into each partial dc capacitors. For example, it is assumed that effective A phase voltage (denoted as V_A) is one half of overall dc link voltage (V_{DC}/2) and A phase current, that is I_A magnitude, flows from neutral points as shown Fig. 2. The time to flow A phase current I_A from capacitor C_1 and capacitor C_2 is one half of sampling time (T_S/2) and zero, respectively. Therefore, the flowing time of each capacitor (denoted as "$T_{C1,VA}$, $T_{C2,VA}$") can be written in terms of eta function (η (x)) as:

$$T_{C1C2,V_A} = T_S \; H_{C1C2,V_A} \tag{7}$$

Where, $T_{C1C2,V_A} = \left[T_{C1,V_A} \quad T_{C2,V_A}\right]^T$;

$$H_{C1C2,V_A} = \left[\eta(t_A) \quad \eta(t_A - 1)\right]^T;$$

$$t_A = \frac{2 \cdot V_A}{V_{DC}}; \quad \eta(x) = \frac{1}{2}\left(|x| - |x-1| + 1\right);$$

If all the capacitance of each partial dc capacitors is C, the fluctuation of DC-link voltage caused by the current flowing from each partial dc capacitor during sampling time can be obtained as:

$$\Delta I_{C1C2,V_A} = I_A \; T_{C1C2,V_A} \tag{8}$$

Where, $\Delta I_{C1C2,V_A} = \left[\Delta I_{C1,V_A} \quad \Delta I_{C2,V_A}\right]^T$;

$$\Delta V_{C1C2,V_A} = \left(\frac{T_S}{C}\right) \Delta I_{C1C2,V_A};$$

Generally, it is assumed that each three effective phase voltages obtained by (2) (denoted as "Va, Vb and Vc") and three phase currents corresponding to effective phase voltages, which have Ia, Ib and Ic magnitude, flows from partial dc capacitor to motor load as shown Fig. 2 . It is also assumed that the load is balanced. The fluctuation of DC-link voltage on the each partial dc capacitors during sampling time can be written by superposition principle as following:

$$\Delta V_{link,C1C2} = \left(\frac{T_S}{C}\right) H_{C1C2} \; I_{ABC} \tag{9}$$

Where, $\Delta V_{link,C1C2} = \left[\Delta V_{link,C1} \quad \Delta V_{link,C1}\right]^T$;

$$H_{C1C2} = \begin{bmatrix} \eta(t_A) & \eta(t_B) & \eta(t_C) \\ \eta(t_A - 1) & \eta(t_B - 1) & \eta(t_C - 1) \end{bmatrix};$$

$$I_{ABC} = \left[I_A \quad I_B \quad I_C\right]^T; \; T_{A,B,C} = \frac{2 \cdot V_{A,B,C}}{V_{DC}};$$

The current of passive rectifier flows commonly into all partial dc capacitors to make the overall fluctuation of DC-link voltage zero. Therefore, rectifier current results in the fluctuation of DC-link voltage with the same magnitude on each partial dc capacitor as following:

$$\Delta V_{rect,C1C2} = -\frac{1}{2} L \; \Delta V_{linkC1C2} \tag{10}$$

Where, $\Delta V_{rect,C1C2} = \left[V_{rect,C1} \quad V_{rect,C2}\right]^T$; $L = \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix}$;

The overall fluctuation of DC-link voltage can be obtained by adding (9) and (10).

$$\Delta V_{C1C2} = \Delta V_{link,C1C2} + \Delta V_{rect,C1C2} \tag{11}$$

Where, $\Delta V_{C1C2} = \left[\Delta V_{C1} \quad \Delta V_{C2}\right]^T$;

$$\therefore \begin{bmatrix} \Delta V_{C1} \\ \Delta V_{C2} \end{bmatrix} = \left(\frac{T_S^2}{C}\right) \begin{bmatrix} 1/2 & 1 \\ 1 & 1/2 \end{bmatrix} \begin{bmatrix} \eta(t_A) & \eta(t_B) & \eta(t_B) \\ \eta(t_A - 1) & \eta(t_B - 1) & \eta(t_B - 1) \end{bmatrix} \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix}$$

Knowing three phase currents I_A, I_B and I_C and

effective phase voltages V_A, V_B and V_C, the overall fluctuation of DC-link voltage can be estimated by (11).

C. Realization of DC-link voltage control method

Earlier mentioned, in proposed space vector PWM, the addition of optimal voltage offset with a equal magnitude to each effective phase voltages obtained by (2) changes the path and duration to flow the phase current from or into each partial dc capacitors. The best optimal voltage offset is the value to make the overall fluctuation of DC-link voltage estimated by (11) zero during sampling time of reference voltage vector. However, it needs difficult and complex process that mathematical optimal voltage offset is obtained through algebraically solving (11) due to eta function. Though mathematical optimal voltage offset is obtained, it doesn't always valid. For example, sometimes, the summation value of voltage offset and effective phase voltages is not located from 0 to overall dc link voltage. Therefore, this approach is not suitable for real implementation.

As alternative approach, the method that optimal voltage offset for only one of the two partial dc capacitors is chosen among prefixed voltage offset is devised. In this paper, only three prefixed voltage offsets, which are 0, $-(V_{DC}-V_{MAX})$ and $(V_{DC}-V_{MAX})$, are used for simplicity of calculation. Where, V_{dc} is overall dc link voltage; V_{max} is a maximum voltage of three phase reference voltages; Because each of these prefixed voltage offsets makes fully different path and time to flow the phase current from or into each partial dc capacitors respectively, they have enough influence to control DC-link voltage and they are always valid to summation with effective phase voltages. The partial dc capacitor voltage to choose optimal voltage offset is maximum capacitor voltage among two partial dc capacitor voltages. it seems to be desirable to guarantee the safe operating of power devices.

Fig. 7 shows the schematic diagram of proposed DC-link voltage control method. The maximum effective phase voltage and maximum partial capacitor voltage are identified in maximum identification block. The maximum effective phase voltage is used to make prefixed voltage offsets and the maximum partial capacitor voltage is used to choose optimal voltage offset. The fluctuations of DC-link voltage according to each of prefixed voltage offsets can be estimated by (11) in the potential fluctuation estimation block. If the

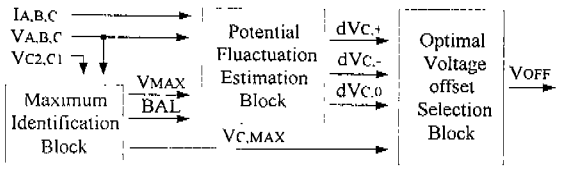


Fig. 7. Schematic diagram of proposed DC-link voltage control.

Table 2. Simulation condition.

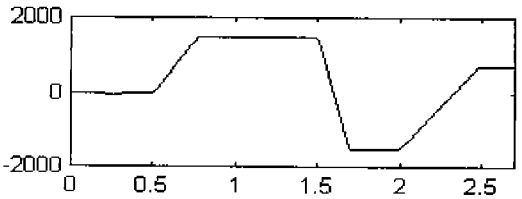
Inverter	Ts	500[us]	C_{DC}	4000uF
Motor	Lr	0.0547[H]	Rr	0.2[Ω]
	Ls	0.0547[H]	Rs	1.26[Ω]
	Lm	0.05[H]	Jm	0.017 [kg·m²]
	Power	3.7[kW]		
Computer System	CPU	P-166	Running time	15[min]
	RAM	64MB		
Reference Speed [S]	0.0-0.5	0[rpm]	0.5-1.5	1500[rpm]
	1.5-2.0	-1500[rpm]	2.0-2.7	750[rpm]

differences between each of the two capacitor voltage and $V_{DC}/2$ are all less than a prefixed value, BAL signal is false. Then, optimal voltage offset becomes zero. Otherwise, optimal voltage offset, that make the maximum fluctuation of partial dc capacitor suppress, is selected in the optimal voltage offset selection block.

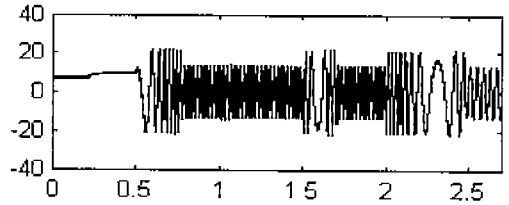
IV. SIMULATION RESULTS

To verify the validity of the proposed SVPWM and control method of DC-link voltage, some simulations is archived by Matlab/Simulink. Table 2 shows simulation condition. To certify the proposed method to keep the balancing of dc link voltage, unbalancing of dc link voltage is made by charging lower capacitor C_1 with 4000A current at 1 second.

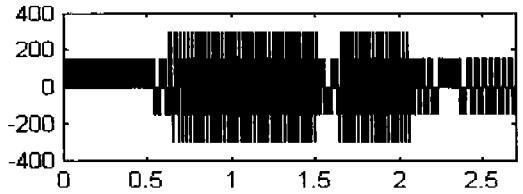
Fig. 8 and Fig. 9 show simulation results of the proposed SVPWM. Fig. 8 (a), (b), (c) and (d) present the steady-state waveforms of motor speed, phase current, line-to-line voltage and DC-link capacitor bank voltage in the three-level inverter respectively. By using the proposed method to keep the balancing of dc link voltage, dc link voltage keeps the balancing when motor speed is accelerated or decelerated. Moreover, in spite of charging lower capacitor C_1 with 4000A current, voltage balancing is well adjusted. Fig. 9 (a) and (b) show the extended line-to-line voltage waveforms of two-level and three-level.



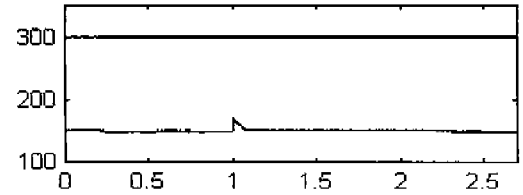
(a) Motor speed.



(b) Phase current.

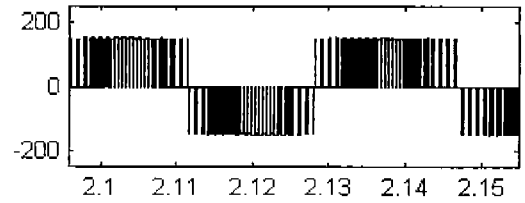


(c) Line-to-line voltage.

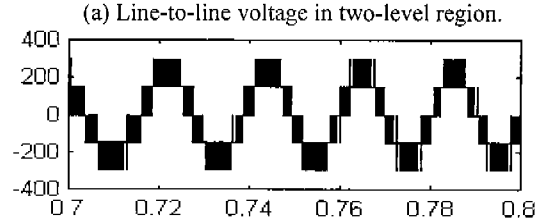


(d) DC-link capacitor bank voltage.

Fig. 8. Simulated waveforms in three-level inverter.



(a) Line-to-line voltage in two-level region.



(b) Line-to-line voltage in three-level region.

Fig. 9. Extended line-to-line voltage in three-level inverter.

V. CONCLUSION

We proposed a novel SVPWM strategy considering DC-link voltage balancing for a diode clamped multi-level inverters in this paper. Because of using only absolute function, min-max sorting algorithm without sinusoidal function, they are easily implemented for Digital Controller such as DSP, MPU. It is similar to SPWM and has the same DC-link voltage utilization as conventional SVPWM. In proposed PWM, the influence of the reference voltage and phase current about the fluctuation of DC-link voltage is analyzed. By this analysis, the method to keep the voltage balancing of series-connected dc partial capacitor is proposed.

The usefulness of the proposed SVPWM and DC-link voltage balancing method is verified through the simulation. They are suitable for a large capacity diode clamped multi-level inverter applied to variable speed drive of induction motor.

Theoretically, the proposed SVPWM and DC-link balancing method can be extended to DCMLIs. However, DCMLIs with more than four-level has another inherent problem of DC-link voltage balancing. When a modulation index is high, the voltage fluctuation of inner capacitors can not be controlled. Therefore, the method to solve it will have to be devised. In DCMLIs, if the modulation index is limited to low depth, the proposed PWM strategy and DC-link voltage balancing method will be able to be available.

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