Design Criteria of the Auxiliary Resonant Snubber Inverter Using a Load-Side Circuit for Electric Propulsion Drives

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ABASTRACT - The design criteria of the auxiliary resonant snubber inverter (ARSI) using a load-side circuit are discussed in relation to electric propulsion drives. In this regard, this paper attempts to develop a set of design criteria for the ARSI. First, the switching characteristics of IGBTs under soft-switching mainly in terms of dv/dt, di/dt and switching losses are discussed and utilized for optimizing the selection of the resonant components in the system. After that, the proper control strategies of ARSIs are analyzed and simulated based on voltage space vector modulations. Later, the design, control and implementation of the auxiliary resonant circuit suitable for industrial products are analyzed and presented. And finally, other factors including power stage layout, packaging and the choice of current sensors are included.

The detailed simulation and experimental results will be included based on a laboratory prototype. The proposed design criteria of the ARSI would help the implementation of an electric propulsion drive system.

I. INTRODUCTION

Conventional high power variable-voltage-variable-frequency (VVVF) drive systems for electric propulsion (EP) applications are limited by the switching frequency of the voltage source pulse-width-modulation (PWM) inverters. This is because power devices are subjected to switching losses and switching stresses of the system that increase linearly with switching modulation frequencies. The use of low switching frequency in high power motor drives results in low efficiency due to higher current / torque ripples. But high frequency switching has the significant merits of reducing the current and torque ripples. In particular, acoustic noise can be eliminated by use of the switching frequencies of 20 kHz and above. Since EP systems are very sensitive to high dv/dt and switching noises related to the switching modulation frequency, they are of limited use in drive applications.

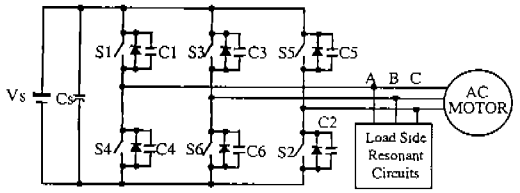
Recently, Soft Switching Inverter (SSI) technologies have been developed for EP drives [1]-[7]. Even though a number of soft-switching circuits have been developed to achieve soft-switching potentials, there still exist several problems in applying the SSI to practical motor drives. The major obstacles in the SSI are the improper main circuit topologies that were proposed in the early development stage. Early SSI technology has mainly been carried out to develop the new circuit topology with a zero-voltage and zero-current concept to reduce the switching losses, dv/dt and electromagnetic interference (EMI). Of them, EMI is a major concern for EP drives. This is because the conducted and radiated EMI noises may cause malfunction of other electronic equipment of the electric vehicle [8]. In investigations of the use of soft-switching inverters, there has been a tendency for the emphasis to be placed upon the control and realization of soft-switching inverter.

This paper endeavors to develop a set of fundamental design criteria for ARSIs that are suitable for high power EP drives. The design aspects considered are for the switching losses and dv/dt, control strategy based on space vector modulation, auxiliary circuit design and its control, and inverter lay-out and packaging. First, the switching characteristics of the IGBTs under the ARSI operations, mainly in terms of dv/dt, di/dt and switching losses for optimizing the selection of the resonant components in the system are discussed. After that, the proper control strategies of ARSIs for EP drives are analyzed and simulated based on voltage space vector modulation (SVM). Later, the design, control and implementation of the auxiliary resonant circuit are included. And finally, other factors including power stage lay-out and packaging are included. To verify the proposed design criteria, the paper includes various results evaluated with theoretical and experimental approaches between hard- and soft-switching inverters.

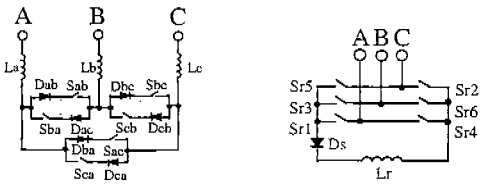
II. ARSI TOPOLOGIES

As ARSI topologies satisfy the zero-voltage switching condition for the main power devices and complete zero-current switching operation for the auxiliary resonant switches during switching, these topologies have the benefit of easy implementation with high efficiency and thus have the potential to be a new family in motor drive applications. In particular, the ARSI topologies with a load-side resonant circuit are a desirable choice due to lower voltage rating of the auxiliary switch.

Figure 1 shows a typical circuit configuration of the ARSI topology that does zero-voltage switching at the load-side. Basically, the ARSIs consist of a traditional six-step inverter with additional resonant circuits which are delta-connected on the output terminals of the inverter.



(a) Basic configuration



(b) Three inductors version (c) One-inductor version

Figure 1. Typical ARSI configuration with a load-side circuit

This structure consists of six power switches, S1-S6, and their anti-parallel diodes, D1-D6. Optionally, capacitors, C1-C6, can be externally added to the inverter. Each auxiliary branch needs at least two auxiliary switching devices for controlling bi-directional operation, which form the four quadrant operations for motor applications. A number of the components in the resonant branch relate with respect to structures [1], [7].

The principle of operation of the ZVT inverter is that the resonant branch circuits operate to provide a zero-voltage condition to the IGBTs during turn-on. The collector-emitter voltage of the IGBT should be kept zero by the parallel capacitors across the main device, like the snubber capacitor in the conventional PWM inverter. Since the resonant capacitor gets fully charged while the IGBT is conducting, the stored energy in the capacitors provides the zero-voltage condition to the IGBT as soon as the IGBT is turned off.

The control of the ARSI with delta connection is obtained by controlling each phase leg, depending on the load current. When the amplitude of the resonant current is larger than the load current to the motor, the auxiliary switch should be turned-on and then the zero-voltage transition will appear in the main switch device. This is achieved by conducting one diode and the auxiliary switch device, while the other remains a diode block.

III. SWITCHING DEVICE AND ITS CHARACTERIZATION UNDER SOFT-SWITCHING CONDITIONS

A. Device selection and its switching characterization

Today, the majority of commercially available used in power inverter/converter applications are Insulated Gate Bipolar Transistors (IGBTs). Most of the IGBTs are punch-through (PT) device, especially for application below 1,000 V. With recent improvements for achieving the forward and reverse blocking capability, non-punch-through (NPT) IGBTs are widely being used beyond 1,200 V application. Since these devices were designed with a high dv/dt, the fundamental switching dynamic behavior clearly is different from that of the original device when it is applied to soft-switching applications with lower dv/dt.

Therefore, the device selection and its switching behavior should be evaluated for the soft-switching operation. The parameter sensitivities of temperature, dv/dt, load current variation and the snubber capacitor and their influence on the working of the device should be analyzed with explain achieving lower switching losses.

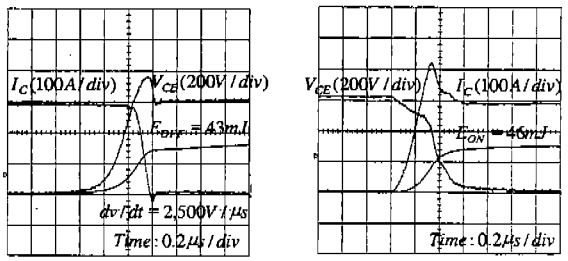
B. Hard-switching characteristics

In a conventional PWM inverter with an inductive load, the turn-on losses cause a reverse recovery in the freewheeling diode and a large current spike. The charges stored in the base of the IGBT cause a current tail at turn-off. This tail increases turn-off losses and also increases a dead-time between the conduction of two devices in the inverter leg. The following experimental waveforms indicate the total losses of the IGBT and diode during switching.

Figure 2 shows the voltage, current and switching energy waveforms of IGBT during turn-on and turn-off under hard switching. During turn-off, dv/dt of 2,500 $[V/\mu s]$ and switching energy of 43 [mJ] were obtained at a load current 300 A. Under turn-on, di/dt of 1,100 $[A/\mu s]$ and switching energy of 46.0 [mJ] at 300 [A] were obtained. Here, considering the current tailing under a hard-switching scheme, turn-off switching loses constitute a very small portion due to the faster turn-off of the device.

C. Turn-off soft-switching characteristics

The turn-off switching behaviors of the IGBT with an ARSI topology are very important with regard to the



(a) Turn-off (b) Turn-on

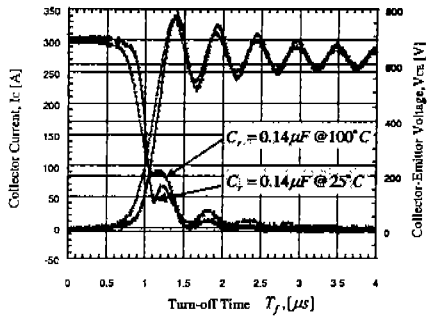
Figure 2. Switching characteristics of the IGBT under hard switching at 300 A

switching losses in the device. In general, the resonant capacitor across the main device significantly reduces the turn-off switching energy due to the lower slope of the voltage rise dv/dt. During turn-off, the parameters of temperature, dv/dt, load current variations and the snubber capacitor are very sensitive to the switching losses. This is very much related to tradeoffs between dv/dt and switching loss in ARSI based on the test conducted. This tradeoff arises because of the relationship between dv/dt and tail current under soft-switching. As the snubbing capacitance increases, switching losses can be significantly reduced at low temperatures, but not at high temperature due to the lifetime of the device.

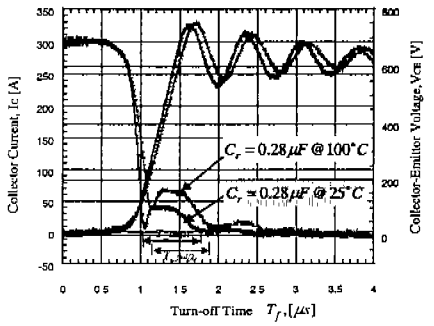
Figure 3 shows experimental turn-off current and voltage waveforms of the IGBT in the ARSI under different temperatures and snubbing capacitors. Figure 3(a) and (b) show the experimental current and voltage waveforms of the IGBT with $C_r = 0.14\mu F$ and $C_r = 0.28\mu F$ at $25^\circ C$ and $100^\circ C$, respectively. Based on the test results, it is inferred that the temperature of the device increases, its dv/dt decreases and the switching losses eventually increase due to the long current tailing. The dv/dt rate of $580V/\mu s$ under $C_r = 0.28\mu F$ in Figure 3(b) is much less than the $2.5KV/\mu s$ that was obtained in the hard-switching condition. The turn-off loss under soft-switching was reduced by four times as compared to the hard-switching condition.

Figure 4 shows turn-off switching energy comparison of the IGBT between hard and soft-switching schemes under different snubbing capacitors. From experimental results, it is obvious that the turn-off switching loss can be reduced by a larger snubbing capacitor at $25^\circ C$, but not at high temperatures, like high as $100^\circ C$, because of the large dumped current.

Besides, one of deign parameters to reduce switching losses is in the gate drive circuit. Since the gate resistor directly relates to the gate capacitance during switching, the total switching energy due to charging and discharging

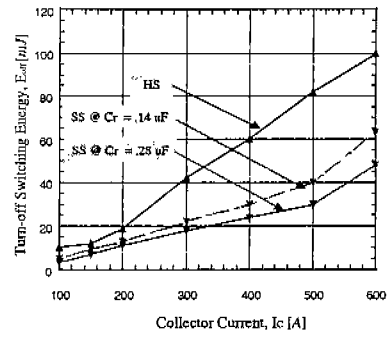


(a) $C_r = 0.14[\mu F]$

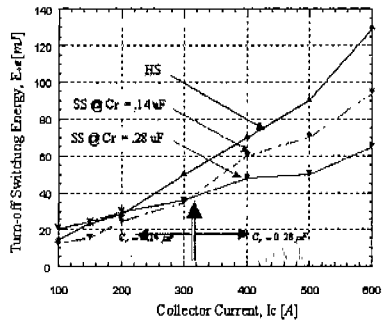


(b) $C_r = 0.28[\mu F]$

Figure 3. Turn-off switching waveforms of ARSI under different resonant capacitors and temperatures at 300 A



(a) $T_J = 25^\circ C$



(b) $T_J = 100^\circ C$

Figure 4. Turn-off switching energy comparisons under HS and SS conditions

switching losses decreases as the value of the gate resistor decreases. As summary, there are two major factors for the gate driver design consideration: one for the lowest drive impedance and one for the slope of induced dv/dt.

Considering these factors can solve designing significant tradeoffs between dv/dt and switching losses. More details were noted in [6].

D. Turn-on soft-switching characteristics

Turn-on switching behavior is characterized mainly under the device temperature and the load current. In ARSI topologies with zero-voltage transition (ZVT), the precise time of the resonant branch to the IGBT is required to minimize the turn-on losses. For this reason, the selection of the resonant components and its conducting time is very critical.

IV. AUXILIARY CIRCUIT DESIGN AND ITS CONTROL

One of the design criteria for the ARSI is in auxiliary circuit design and its control based on the implementation techniques. The design and selection of these components, including resonant inductor and capacitor, and auxiliary switch, etc. is discussed herein.

A. Resonant Capacitor

The selection of the resonant capacitor and inductor is very important because the overall inverter efficiency depends largely on the design and selection of these passive components. The value of the resonant capacitor can be chosen either by achieving a compromise between the turn-off losses and dv/dt or by using the formula below to derive the exact value.

$$\frac{dV_{Cr}}{dt} = \frac{I_{Cr}}{2C_r} \tag{1}$$

Where

$$I_{Cr} = I_{Lr} \pm I_L$$

The symbol depends on the load current direction. When a resonant capacitor is to chosen, it should have a lower equivalent series inductance (ESL) and equivalent series resistance (ESR) and an excellent frequency response to handle the required turn-off current ratings. A polypropylene capacitor can be preferred in the soft-switching inverter.

B. Resonant Inductor

After selecting the resonant capacitor, the resonant inductor should be designed based on the resonant energy balance. The inductor needs sufficient capability during charging time so that the charged energy in the capacitor is fully discharged to the inductor. The time needed depends on turn-on delay time of IGBTs, as in Equation (1). From an energy balance point of view, because the amplitude of the resonant current is required to be larger than the load current for zero voltage switching, the energy relationship between the inductor and capacitor must satisfy the following condition:

$$\frac{1}{2} L_r \cdot I_{Cr}^2 \geq C_r \cdot \left(V_s - 2 \cdot V_{CE(sat)}\right)^2 \tag{2}$$

Where V_S is the dc bus voltage, and $V_{CE(sat)}$ is the device drop voltage for each conducting device of the main device depending on the load current. Equation (2) means that the capacitor energy capability is limited by the function of inductor value and capacitor discharge current. Thus, the resonant inductor value can be calculated as follows:

$$L_r = \frac{V_S - 2 \cdot V_{CE(sat)}}{I_{Lr}} \cdot t_d \tag{3}$$

Considering the turn-on delay time of PWM signal, this value can be obtained from the IGBT selected. For minimizing power conducting loss in the inductor, there are many design options. These two factors can also be translated to the resonant tank impedance $Z = \sqrt{L_r / C_r}$ and resonant frequency $f_{res} = 1/\sqrt{L_r C_r}$. To minimize the peak resonant current, the resonant tank impedance should be considered. According to the selected values of the resonant capacitor and inductor, the auxiliary switch conducting time should be selected by a function of the resonant time and pre-charging time based on the rated load current. The lower permeability core is suitable for the resonant inductor.

C. Auxiliary Switch and Diode

The auxiliary switch requires a high peak current capability and a lower conducting drop voltage in the device. For this requirement, the MCT is the most logical choice. However, with the concern of commercial availability, IGBT is one of the options. Since the auxiliary switch only operates during transitions, the maximum duty ratio of the IGBT should be minimized below 3% of the switching frequency. The resonant branch circuit needs a diode with high reverse recovery characteristics to block the opposite current path of the load current.

D. Control criteria

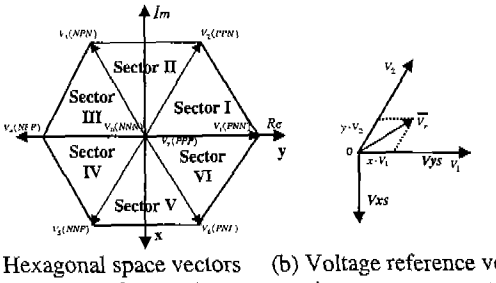
When designing the control circuit and its time sequence, control flexibility with adjustable timing is required for the wide operation ranges for VVVF drives. To stabilize the operation corresponding to the PWM signal as input signal, a monostable multivibrator device is preferred. Besides, the protection circuit for elimination of the short pulse is also added to ensure zero voltage operation under any load condition. For timing control criteria, the relationship between deadtime of the main device and the discharging time of the stored energy of the resonant capacitor should be related to the control of the resonant circuit. There are two possible solutions to implement this in ARSI topologies: fixed timing control and variable timing control. The fixed timing control has an advantage of simple control process, but it has the disadvantage of lower inverter efficiency due to unnecessary high peak resonant current. To overcome and

to restrict the auxiliary switch conducting time, a variable timing control method is preferred to achieve a wide current range.

V. CONTROL CONSIDERATIONS

As this ARS inverter topology has all the auxiliary resonant components on the load side, the three legs of the auxiliary circuit should resonate in coordination with the load current. To satisfy the ZVT condition during commutation period in this topology, at least one of the main switches should be charged or discharged. However, conventional adjacent-space vector modulation is not suitable for the proposed topology and other ac side topologies [10], [11]. In spite of the topological restriction to using zero vectors, the realization of the switching control can be done by changing the voltage vector sequence for a short time to replace the zero vectors. Control strategies are discussed in [7].

Figure 5 shows a three-phase voltage source inverter space vector diagram. If the voltage vector $\overrightarrow{V_r}$ in Sector I is placed in the hexagonal area and is presented by the Park's Plane [10], vector $\overrightarrow{V_r}$ can be synthesized by switching the sequence of the inverter states in Sector I which contains adjacent vectors V1 and V2 and the zero vectors.



(a) Hexagonal space vectors (b) Voltage reference vector

Figure 5. Three-phase voltage source inverter space vectors

The following voltage reference vector equation can be expressed based on Sector I, as $i_a > 0$, $i_b < 0$ and $i_c < 0$.

$$\overrightarrow{V_r} = x \cdot V_1 + y \cdot V_2 + z \cdot V_0 (or \cdot V_7) \qquad (4)$$

Where,

$$x = (V_{ys} + \frac{1}{\sqrt{3}} V_{xs}) \cdot \frac{1}{V_s}$$

$$y = -\frac{2}{\sqrt{3}} V_{xs} \cdot \frac{1}{V_s}$$

$$z = 1 - x - y \qquad (5)$$

x, y and z are weighting factors for the duty cycle of the voltage vectors, respectively. The sum of the duty cycle per switching period is unity. Based on stationary reference frame coordinator [10], a desired voltage vector is synthesized with this sector. V_s is the input voltage of the inverter. For example, the main device sequence should be modified by vector *NPP* instead of *NNN* for a short time until the resonant capacitor charges to provide the zero-voltage turn-on for the next switching sequence. To avoid the zero vectors, if needed, it can be synthesized by two vectors V_1 and V_4. Therefore, a desired reference vector $\overrightarrow{V_r}$ is rearranged as the following:

$$\overrightarrow{V_r} = (x + \Delta x) \cdot V_1 + y \cdot V_2 + \Delta x \cdot V_4 + (z - 2 \cdot \Delta x) \cdot V_7 \qquad (6)$$

Where, Δx is the minimum duty cycle to provide a soft-switching operation. This value can be determined by a function of the auxiliary conducting time. The sequence for all the sectors is the same with this procedure.

The drive system types available for electric propulsive drive applications, we have the induction motor drives and brushless dc motor drives. These motors require a different form of output current waveforms. For our case, a modified SVM scheme is useful for induction motor drive systems and a non-adjancent SVM scheme is useful for brushless dc drive systems. To verify the ZVT operation of the ARSI topology, the circuit was simulated with the Pspice program.

Figure 6 shows the corresponding waveforms of the proposed topology during transitions. Figure 6(a)-(c) shows the gate signal sequences of the main devices in the inverter based on a voltage space vector modulation (SVM). Figure 6(d) shows the body diode currents of the main devices *S4*, *S3* and *S5*, respectively. The total current of S4 for the phase A region is the same as the sum *S3* and *S5*. Figure 6(e) shows the voltage and current waveforms of the main devices during a commutation period, where Ds1 is the diode connected across the main switch S1 on the complementary side.

Figure 7 shows the output current waveforms of the proposed three-phase inverter with voltage space vector modulation. This topology needs *NNN* to be modified to *NPP* and *PPP* to be modified to *PNN* for a short period in Sector I. Similar modifications also need to be applied to other sectors. The output currents, however, remain in a smooth sinusoidal waveform. The simulation result indicates that the proposed topology clearly satisfies the zero-voltage operation during transitions based on the modified SVM control.

Figure 8 shows experimental current and voltage waveforms of ARSI with a load-side resonant circuit. The waveforms in Figure 8(a) indicate zero-voltage switching of IGBT during turn-on. During turn-off, the turn-off voltage and gate voltage was overlapped corresponding to the load current. Figure 8(b) shows the expanded turn-o waveforms of the ARSI. As a conclusion, the ARSI can reduce the switching losses, dv/dt and EMI easily based on the test results.

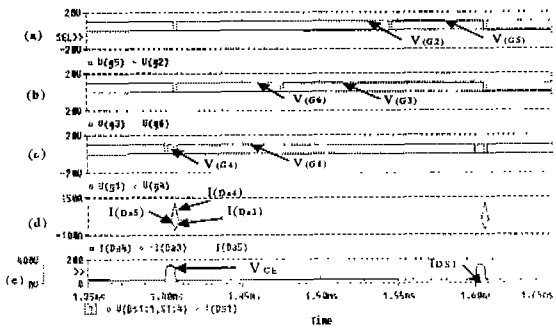


Figure 6. Simulation waveforms during transitions

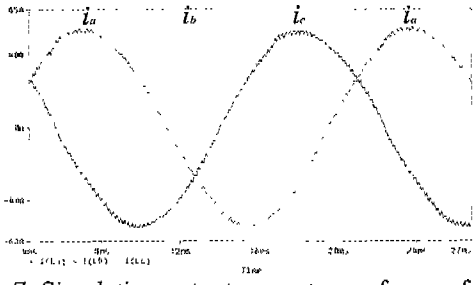
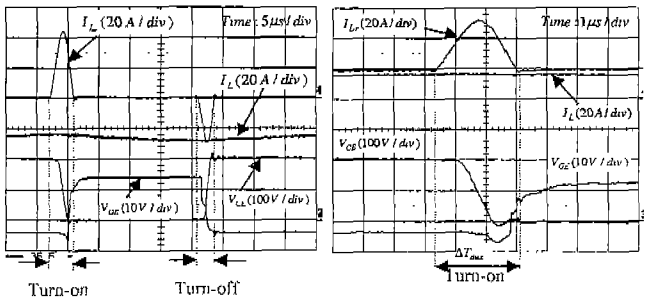


Figure 7. Simulation output current waveforms of ARSI



(a) Turn-on and –off (b) Expanded turn-on

Figure 8. Experimental current and voltage waveforms of ARSI with a load-side resonant circuit

VI. OTHER CONSIDERATIONS

There are other considerations related to power stage layout, packaging and choice of transducer. In an electric propulsive drive system all these considerations are necessary for high reliability and high performance drives. Power lay-out of the inverter should be shifted from the traditional long wire connecting structure to the laminated bus bar structure to eliminate loop inductance in the power connection. This is because the long wiring connection between components generates more parasitic inductance to the system depending on the power rating level. This means that the longer current loop increases a more parasitic inductance and hence affects current and voltage spikes in the system. In order to get a cost-effective inverter which allows convenient maintenance, the layout and connections of a power stage should be considered. Besides, the ARSI needs a current transducer for control and commutation under soft-switching, whereas the EP drives needs the cost-effective device with high reliability.

VII. CONCLUSIONS

The design criteria of the auxiliary resonant snubber inverter using load-side circuit for electric propulsion drives are discussed. In this regard, this paper attempted to develop a set of design criteria for the ARSI. These complex design criteria problems are reduced by the various approaches under soft-switching for EP applications. In addition, the detailed simulation and experimental results were presented to verify the proposed design procedures based on a laboratory prototype to the greatest extent possible. The proposed design criteria of the ARSI would help the implementation of the electric propulsion drive system.

ACKNOWLEDGEMENTS

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