Zero-Voltage and Zero-Current-Switching (ZVZCS) Full Bridge PWM Converter with Zero Current Ripple

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Abstract — **A novel zero voltage and zero current switching (ZVZCS) full bridge (FB) PWM converter with low output current ripple is presented. A simple auxiliary circuit added in the secondary provides ZVZCS conditions to primary switches, ZVS for leading-leg switches and ZCS for lagging-leg switches, as well as reduces the output current ripple (ideally zero ripple). The auxiliary circuit includes neither lossy components nor additional active switches which are demerits of the previously presented ZVZCS converters. Many advantages including simple circuit topology, high efficiency, low cost and low current ripple make the new converter attractive for high performance high power (> 1 kW) applications. The principle of operation, features and design considerations are illustrated and verified on a 2.5 kW, 100 kHz IGBT based experimental circuit.**

I. Introduction

IGBTs usually have higher power density, lower cost comparing to MOSFETs but IGBTs have higher switching loss due to tail current characteristic. To operate IGBTs at high frequency, ZVS with additional snubber capacitor or ZCS could be solution.

To use IGBTs at higher frequencies, ZVZCS-FB-PWM converters have been presented [4-7]. The ZVZCS means the mixed operation of ZVS for leading-leg switches and ZCS for lagging-leg switches in the bridge. The ZVS of leading-leg switches is achieved by the same manner as that of the ZVS full bridge PWM converters [1,2] while the ZCS of lagging-leg switches is achieved by resetting the primary current during the freewheeling period. Due to the ZCS, ZVZCS-FB-PWM converter have several good features compared to ZVS-FB-PWM converter. The primary current for ZCS is reset by different manner; (a) by using the reverse avalanche break down voltage of the leading leg IGBTs[4], where the stored energy in the leakage inductance is completely dissipated in the leading-leg IGBTs; (b) by using the dc blocking capacitor voltage and a saturable reactor [5]; or (c) by adding an active clamp in the secondary side [6] which needs one additional active switch. Using lossy components to reset the primary current [4,5] reduces the overall efficiency and hinders the increase of power handling capability over than 5 kW. Using an active clamp increases the cost and control complexity [6]. Another approach to reset the primary current is by adding a snubber circuit in the secondary side [7] which has no lossy components in the snubber circuit. This circuit, however, has high voltage stress in the secondary rectifier diodes and increased conduction loss by the large circulating energy.

This paper proposes a novel ZVZCS-FB-PWM converter which improves most of the disadvantages of the previously presented ZVZCS-FB-PWM converters [4-7]. A simple auxiliary circuit added in the secondary side not only provides the ZVZCS condition to the primary switches but reduces the output current ripple, ideally zero current ripple[8]. The ZVS mechanism of leading leg switches is also the same as that of the converters in [1,2,5-8]. The ZCS of lagging leg switches, however, are achieved by adding an inductor auxiliary winding and a simple auxiliary circuit in the secondary side. No lossy components are involved nor additional active switch is added. Besides, no large circulating energy and no secondary parasitic ringing is generated. All active and passive devices are operated under low voltage and current stresses. So, most of the problems are solved and additionally reduced output current ripple is achieved.

The basic operation and features of the proposed converter are illustrated. A 2.5 kW, 100 kHz prototype has been built using IGBTs and tested to verify the principle of operation.

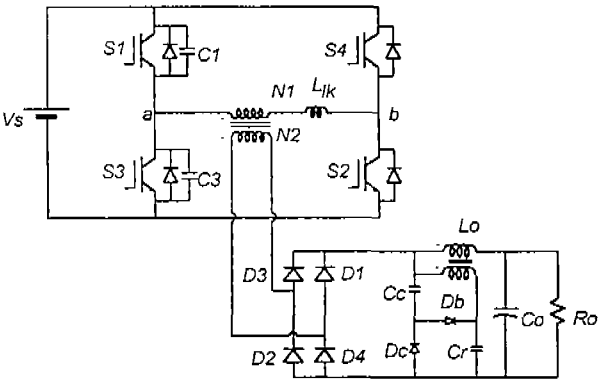


Fig. 1 Circuit topology of the proposed ZVZCS full bridge PWM converter.

II. Operation Principle

To simplify the illustration of ZVZCS operation, it is assumed that all components and devices are ideal and the output filter inductor current is constant. The ripple reduction principle is explained in the other section.

A. ZVZCS operation

The basic operation of the proposed ZVZCS-FB-PWM converter is the same as that of the ZVS-FB-PWM converter, the phase shift PWM control. The new converter has nine operating modes within each operating half-cycle. The equivalent circuits and simplified equivalent circuits are shown in Fig. 2 and 3, respectively and operation waveforms are shown in Fig. 4.

Mode 1: S1 and S2 are conducting and the input power is delivered to the output. The holding capacitor voltage V_{Cc} is increased from zero by the resonance with leakage inductance as shown in Fig. 4. During one resonant period, the V_{Cc} increases twice of inductor voltage(V_{Lo}). The parasitic ringing between the leakage inductance and the junction capacitance of the secondary rectifier diodes is not generated if Cr is included. The simplified equivalent circuit reflected to the primary is shown in Fig. 3. The primary voltage and current and voltage and current of the auxiliary circuit can be obtained as follows:

$$V_{ab}(t) = V_s \tag{1}$$

$$I_p(t) = nI_o(1-\cos(w_a t)) - \frac{V_s - \frac{V_o}{n}}{Z_a}\sin(w_a t) + nI_o, \tag{2}$$

$$I_c(t) = nI_o - I_p(t) \tag{3}$$

$$V_{Cc}(t) = nV_s(1-\cos(w_a t)) - n^2 Z_a I_o \sin(w_a t), \tag{4}$$

where, n is turns ratio (n2/n1) of the transformer winding, n1 is the primary winding, n2 is the secondary winding,

$$n = \frac{n_2}{n_1}, Z_a = \sqrt{\frac{L_{lk}}{n^2 C_c}}, w_a = \frac{1}{\sqrt{n^2 L_{lk} C_c}}$$

Mode 2: The V_{Cc} is maintained to double of inductor voltage V_{Lo}, the input power is still delivered to the output. The primary voltage and current is maintained constantly as follows:

$$V_{ab}(t) = V_s \tag{5}$$

$$I_p(t) = nI_o \tag{6}$$

Mode 3: S1 is turned off and then the current through the primary charges C1 and discharges C3. The primary voltage is decreased and the secondary rectifier voltage is also decreased with the ratio of (n2/n1). The primary voltage linearly decreased as follows:

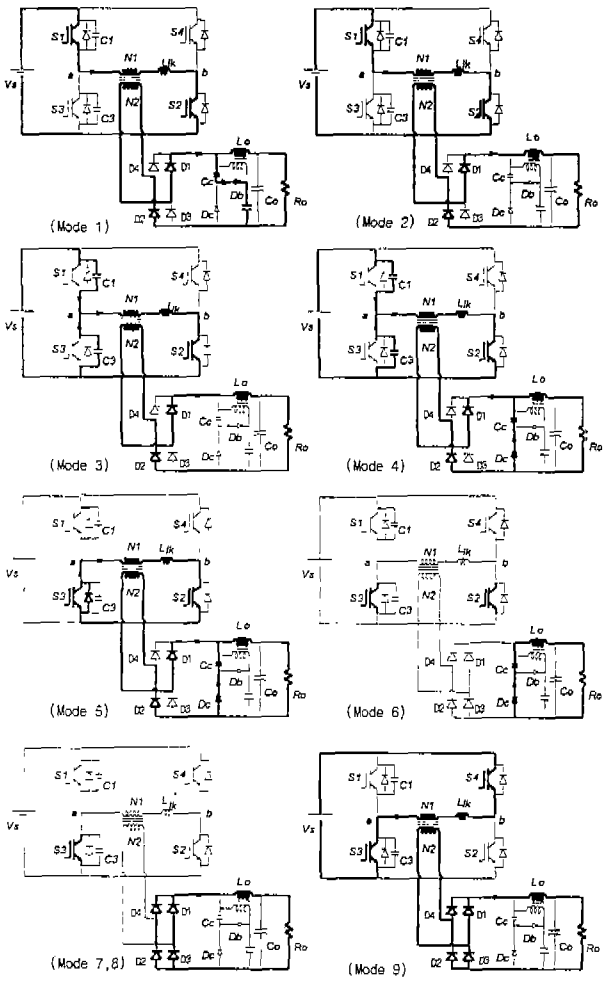


Fig. 2 Equivalent circuits for each operating mode.

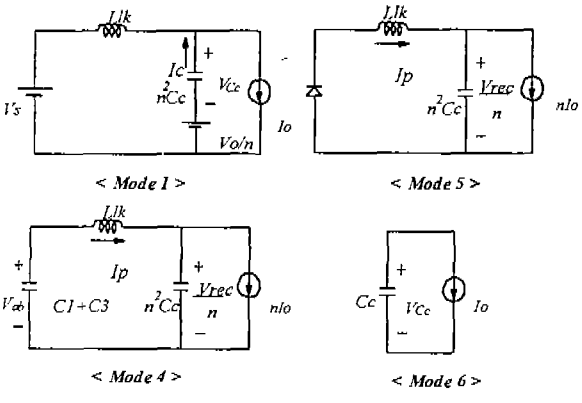


Fig. 3 Simplified equivalent circuits.

$$V_{ab}(t) = V_s - \frac{nI_o}{C1+C3}t, \tag{7}$$

$$I_p(t) = nI_o \tag{8}$$

Mode 4: When the rectifier voltage reaches the holding capacitor voltage V_{Cc}, the diode Dc is turned on and the Cc holds the rectifier voltage, which means the rectifier voltage decreases more slowly than the primary voltage.

The primary voltage decreases almost same rate as before since the stored energy in the leakage inductance still charges C1 and discharges C3. (Cc is assumed much larger than C1 or C3.) The difference between the primary voltage and the reflected secondary voltage is applied to the leakage inductance and the primary current starts decreasing. The simplified equivalent circuit reflected to the primary is shown in Fig. 3. The voltage and current of circuit are as follows:

$$V_{ab}(t) = \frac{nI_o}{w_b}\left(\frac{1}{\frac{2}{w_b}} - \frac{1}{c_{eq}}\right)\sin(w_b t) - \frac{nI_o}{\frac{2}{w_b}}t + 2V_{Lo}, \quad (9)$$

$$I_p(t) = nI_o\left(1 - \frac{C_{eq}}{\frac{2}{w_b}}\right)\cos(w_b t) + \frac{C_{eq}}{\frac{2}{w_b}}nI_o, \quad (10)$$

$$V_{Cc}(t) = -\frac{I_o c_{eq}}{c_c \frac{2}{w_b}}\sin(w_b t) + \frac{I_o c_{eq}}{c_c \frac{2}{w_b}}t + 2V_{Lo}, \quad (11)$$

where, $\omega_b = \sqrt{\frac{n^2 C_c + C1 + C3}{n^2 L_{lk} C_c (C1 + C3)}}$, $C_{eq} = C_1 + C_3$

At the end of that mode, the primary current and the secondary voltage are defined as I_α and V_α.

Mode 5: The C3 is completely discharged and then DS3 is conducting. The reflected secondary voltage is applied to the leakage inductance and the primary current decreases quickly. The Cc supplies more current to the load. The primary current reaches zero at the end of this mode and the rectifier voltage is defined as V_β.

$$I_p(t) = (I_\alpha - nI_o)\cos(\omega_a t) - \frac{V_\alpha}{nZ_a}\sin(\omega_a t) + nI_o, \quad (12)$$

$$V_{Cc}(t) = n(I_\alpha - nI_o)Z_a \sin(\omega_a t) + \frac{V_\alpha}{n}\cos(\omega_a t), \quad (13)$$

Mode 6: The primary current is completely reset and no current flows through the primary. Then the Cc supplies whole load current and thus the rectifier voltage is decreased quickly. From equivalent circuit in Fig.3, the holding capacitor voltage is obtained as follows:

$$V_{Cc}(t) = -\frac{I_o}{C_c}t + V_\beta, \quad (14)$$

Mode 7: When the Cc discharges completely, the rectifier diodes start to conduct and the load current freewheels through the rectifier.

Mode 8: At the end of the freewheeling period, S2 is turned off with complete ZCS since there is no current in the device.

Mode 9: After dead time between S2 and S4, S4 is turned on. This turn-on process is also ZCS since the primary current can not be changed abruptly due to the leakage inductance. The primary current is linearly increased. The rectifier voltage is still zero. This is the end of an operating half cycle.

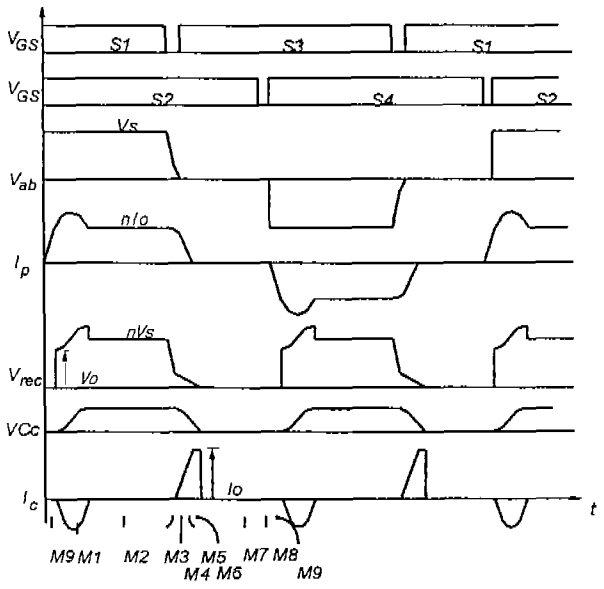


Fig. 4 Operation waveforms.

B. Zero current ripple of the output inductor

The zero ripple current at the output filter inductor using a simple auxiliary circuit coupled with the inductor as shown in Fig. 5 [8] is adopted. The output current ripple can be dramatically reduced without changing the basic dc conversion characteristics and ZVZCS operation.

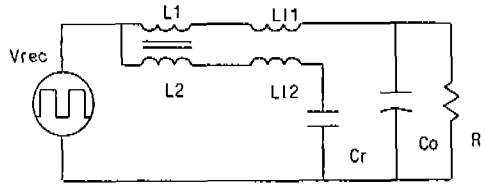


Fig. 5. The coupled inductor at the output filter for zero current ripple.

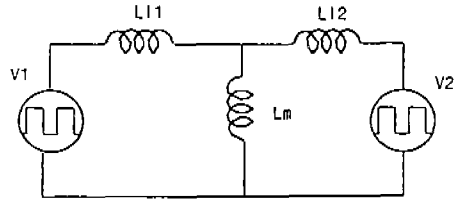


Fig. 6. Equivalent circuit model of the coupled inductor

The analysis of the current ripple in the coupled inductor is well explained in [9] but it is briefly reviewed here. Simplified equivalent circuit is shown in Fig. 6. The coupled inductor is modeled with an ideal transformer and leakage inductors. The square wave voltages are applied to the both primary and secondary

sides of the transformer. Hence, the current analysis is reduced to analysis of the inductor whose both primary and secondary are excited by the proportional switched voltage source V1, V2, as shown in Fig. 6.
From the equivalent circuit model, if the proportionality of inductor switching waveform V1 and V2 is 1:1, the primary and secondary leakage inductance can be expressed as follows[9]:

$$L_{l1} = (1-km)L_1, \tag{15}$$

$$L_{l2} = m(m-k)L_1, \tag{16}$$

where, the coupling coefficient k and the effective turn ratio m is defined as follows:

$$k = \frac{Lm}{\sqrt{L_1 L_2}}, \quad m = \sqrt{\frac{L_2}{L_1}}$$

and Lm is mutual inductance, and L_1, L_2 is the self-inductance of the primary and secondary windings.
If the follow equation is satisfied,

$$m=k, \tag{17}$$

the secondary leakage inductance reduced zero. So, both ends of the primary inductance $(1-k^2)L_2$ are subjected to the same switching voltage waveforms and result in zero voltage across it. Therefore, the zero ripple current on the primary side of inductor is obtained.
The condition (17) is obtained by either changing effective turns ratio m and considering coupling coefficient k to be fixed, or vice versa. The variation of effective turns ration m is discrete in nature, realized by adding or subtracting turns, not continuous. Therefore, the variation of coefficient k which is changed continuously is introduced in [8]. However, the variation of m is adapted in this paper for easy experiment and a fixed inductance.

III. Features and Characteristics

The ZVS of leading leg switches is achieved by the same manner as that of the converters in [1,2,4-7] while the ZCS of lagging leg switches is achieved by adding an inductor auxiliary winding and a simple auxiliary circuit in the secondary side. Neither lossy components nor additional active switch are required to get ZCS. Besides, no large circulating energy is generated. All active and passive devices are operated under low voltage and current stresses. In addition, the proposed converter has wide ZVZCS range, small duty cycle loss, no severe parasitic ringing and zero ripple phenomenon which allows use of a small size output filter. So, most of problems of the previously presented ZVZCS converters[5-8] are solved and additional good feature like zero output current ripple is achieved. This makes the proposed converter very attractive for high power applications.

The auxiliary circuit is simple, which consists of a secondary inductor winding, two diodes and two capacitors. The diodes of the auxiliary circuit are also small (about 30% of main diode). So, the cost increase by the auxiliary circuit is minor.

IV. Experimental Results

A 2.5 kW, 100 kHz prototype of the proposed ZVZCS-FB-PWM converter has been built and tested to verify the principle of operation. Fig. 7 shows the experimental circuit with the parameters and the part numbers of components used.
Fig. 8 shows the experimental waveforms of the primary voltage and current, and the secondary rectifier voltage and Fig. 9 shows their extended waveforms. All waveforms are well matched with the theoretical ones. It can be seen that the primary current is completely eliminated during the freewheeling period by the secondary rectifier voltage. Fig. 10 shows the switching waveforms of lagging-leg switches. It can be seen that the switch S2 is turned off with complete ZCS since the current through it is zero before turning off. A small current pulse when the S4 is turned on is the charging current of switch output capacitance. Figs. 11 show the waveforms of rectifier voltage and holding capacitor voltage and current. The holding capacitor voltage goes to the negative, which is because of the stray inductance of rectifier and auxiliary circuit. Fig. 12 shows inductor current ripple of the proposed circuit and a conventional converter. It can be noted that the ripple of the proposed circuit is considerably smaller than that of a conventional one. The turns ratio of inductor is about 0.65 which is the value to satisfy equation (17). The small semicircle shape of ripple current is due to charging current of holding capacitor. All waveforms are also the same as the expected. Novel circuit allows to use a low cost slow speed IGBTs (10-20 kHz recommended switching frequency) at a very high frequency (100 kHz) with very small size output filter.

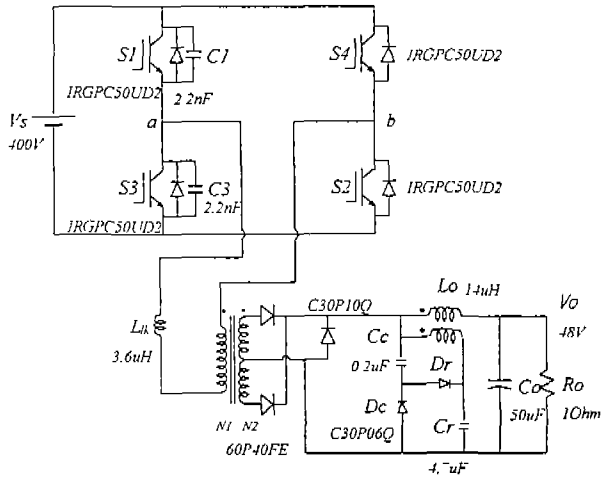


Fig. 7 Experimental circuit diagram of the proposed converter.

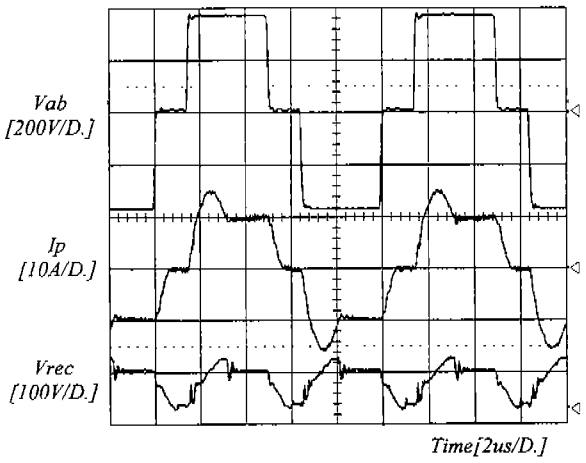


Fig. 8 Experimental waveforms of the primary voltage and current and secondary rectifier voltage.

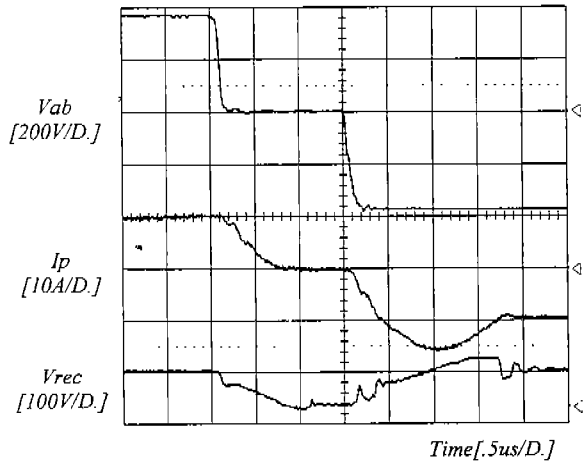


Fig. 9 Extended waveforms of Fig. 8.

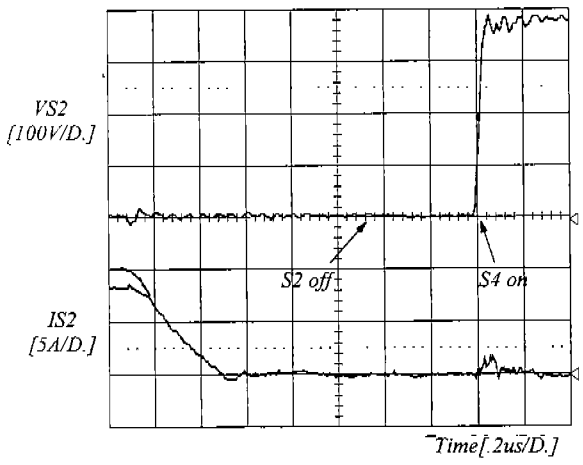


Fig. 10 ZCS waveforms of lagging-leg switches.

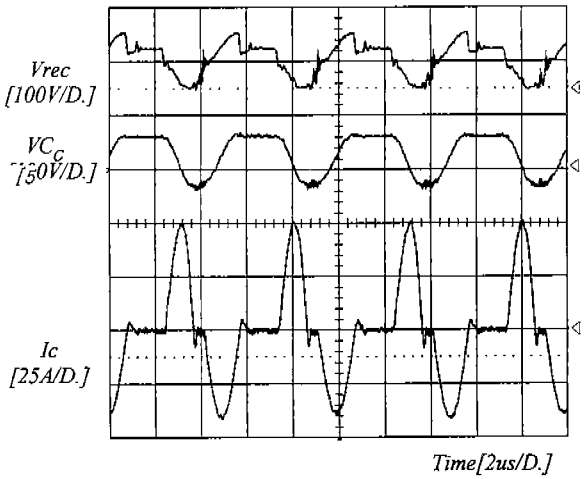
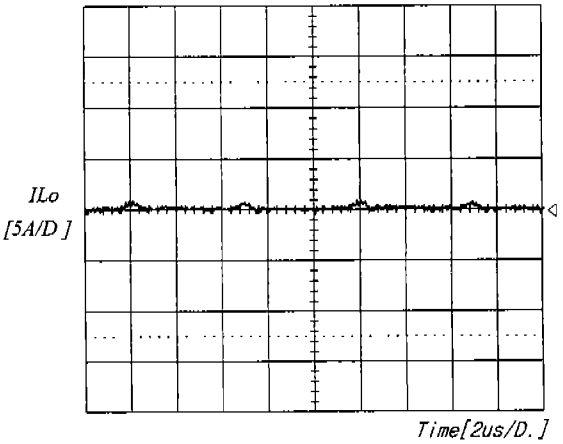
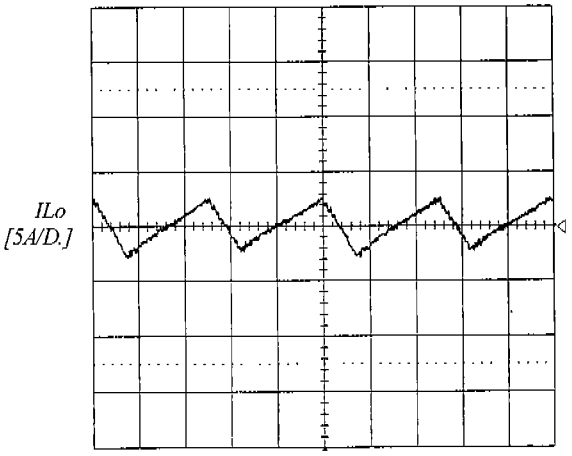


Fig. 11 Waveforms of secondary rectifier voltage and holding capacitor voltage and current.



(a) with auxiliary circuit (ZVZCS operation)



(b) without auxiliary circuit (ZVS operation)

Fig. 12 The comparison of inductor current ripple between a conventional dc/dc converter and the presented dc/dc converter.

V. Conclusion

The novel ZVZCS-FB-PWM converter with a low output current ripple is presented and the operation and features are illustrated. Experimental results from the 2.5 kW, 100 kHz IGBT based prototype is shown to verify the operation principle.

It is shown that ZVZCS operation and low current ripple in the output filter are achieved by using the inductor auxiliary winding and the simple auxiliary circuit and most of problems of the previously presented ZVZCS converters are solved as follows: no lossy components are involved; no additional active switch; no additional device voltage and current stresses are exhibited. The distinct advantages of the new circuit including ZVZCS with wide load range (IGBTs can be used), small duty cycle loss, minimum device voltage and current stresses, and low cost make the proposed converter very promising for high power (> 1 kW) applications with high power density.

References

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