Soft-Switching Three-Level Chopper-Inverter for High-Power Applications

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ABSTRACT–A soft-switching three-level chopper-inverter system was built for high-power applications like Power Conditioning System (PCS) for Superconductive Magnetic Energy Storage (SMES). The system can handle 1800-VDC, 200-A peak, and 250-kW output power. The system was designed to operate with 20-kHz PWM operation with the aid of state-of-the-art zero-current transition type soft-switching. The system is based on the Power Electronics Building Block (PEBB) concept.

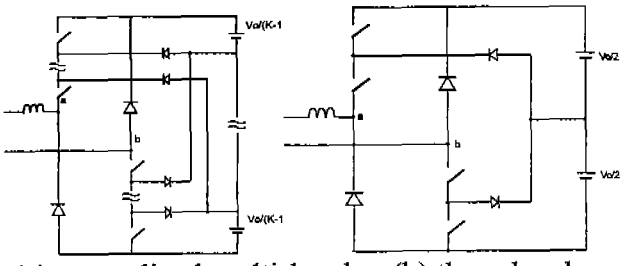
1. INTRODUCTION

High-power high-voltage applications claim high-voltage and high-loss from switching devices. Commonly used switching devices for the high-power applications are GTO and SCR. For the application that requires high-power and high-speed response, thyristors are not suitable simply because of their speed limit. An alternative device for the applications is IGBT. However, the IGBT is still not enough to handle an application like SDI. In this case, the speed limit of the IGBT can be extended by using the soft-switching technique. The soft-switching technique that can help most efficiently is zero-current transition (ZCT) technique. The ZCT can turn off the IGBT with zero-current. There are lots of different types of ZCT topology. Among those ZCT topologies, there is a topology that can reduce reverse recovery of main diode, too. With the ZCT topology, the usefulness of the ZCT circuit can be maximized. By accommodating the ZCT topology, a generalized 250-kW chopper-inverter system was built with 20-kHz PWM operation frequency. The switching frequency can extend the dynamic range of the system up to 1-kHz. One of the applications that can make use of the system fully is a power conditioning system for Superconductive Magnetic Energy Storage (SMES). The SMES is a promising technique for many high-power applications, such as large-pulse power/UPS and utility stabilizer, due to its ability to store a large amount of energy efficiently and its fast response speed. Like a battery, the SMES is basically a DC power storage device and has two-quadrant operation. Unlike a battery, the current direction is fixed, and voltage can be changed.

The converter and the chopper are based on the Power Electronics Building Block (PEBB) concept, and provide significant performance and cost advantages over the existing systems.

2. THREE-LEVEL CHOPPER

A novel general multi-level structure of the two-quadrant boost converter is shown in Figure 1(a), with an example of three-level converter shown in Figure 1(b). Compared with conventional two-level converters, voltage sharing of the series switches can be guaranteed by the clamping diodes.



(a) generalized multi-level (b) three-level

Figure 1. Two-quadrant boost converters

Another major advantage of the multi-level converter is the availability of many more operating modes. The possible sub-topologies of a three-level converter are shown in Figure 2, and many sub-topologies are redundant to each other. These redundant states can be used to reduce switching loss, current ripple and to maintain the charge balance of the dc link midpoint. It is shown that similar performance can be achieved in a three-level converter with 1/4 of the switching loss in a two-level converter [1]. Therefore, a multi-level structure can boost system performance significantly. An important advantage of the multi-level structure is that IGBTs, which are robust and have much lower switching losses than GTOs, can be used up to several MW power range.

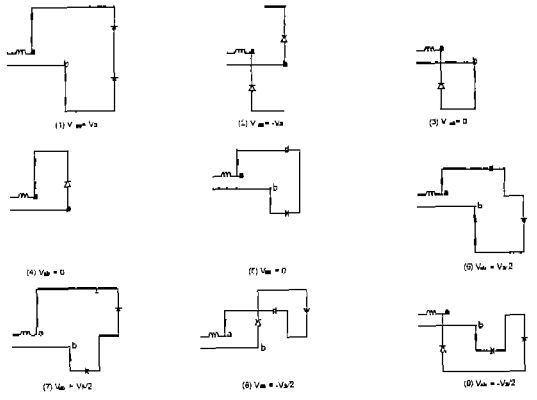


Figure 2. Sub-topologies of the three-level two-quadrant converter

3. THREE-LEVEL VSI

Three-phase multi-level voltage source inverters are suitable for high-power, high-voltage applications. The most popular one is the three-level inverter, first proposed in [2]. Similar to the three-level converters discussed above, the advantages of a three-level VSI can be summarized as follows: voltage across the switches is only half of the dc-bus voltage, switching losses are cut in half with reduced harmonics of output waveforms for the same switching frequency, and power rating increases. However, the disadvantages of the three-level VSI include complex control, large number of devices, and the charge balance problem of the midpoint. The topology of a three-phase VSI is shown in Figure 3.

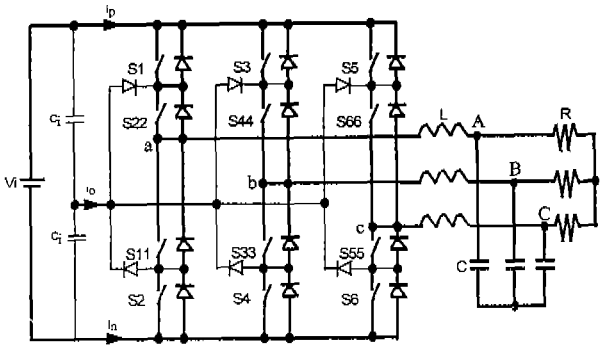


Figure 3. Circuit schematic of a three-level VSI

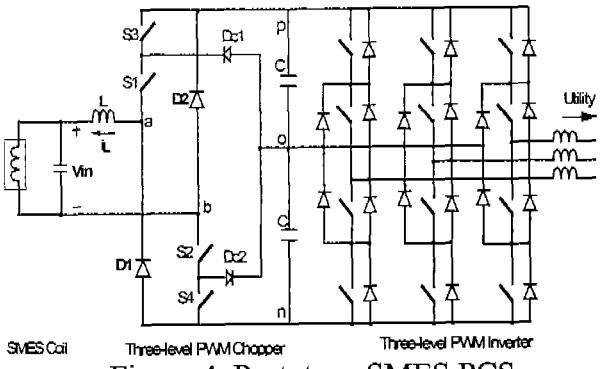


Figure 4. Prototype SMES PCS

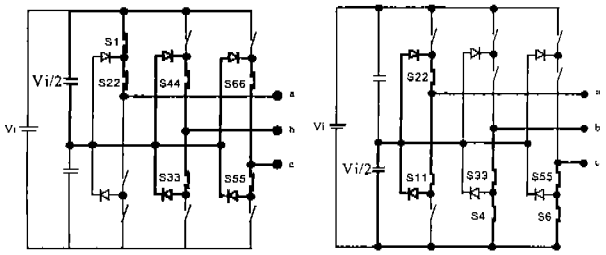
Each leg is composed of two upper and lower switches and their anti-parallel diodes. Two input capacitors split the DC bus voltage in half. In addition, six clamping diodes ensure that voltages across the switches will be determined by the voltages of the input capacitors. The charge balance of the midpoint can be satisfied by using a proper modulation scheme. Figure 4 shows the total system configuration of the SMES PCS.

4. SPACE VECTOR MODULATION

The conditions for the three-level VSI switching states are that the input capacitors

should not short, and the inductor current should be continuous. In general, there are 12^2 switching states for a three-level converter circuit. Only 27 of the 12^2 states satisfy the above conditions. Each phase (a, b, c) can be connected to positive dc-bus, (p), negative dc-bus, (n), and the midpoint, (o). As an example, Figure 5 shows the switching configurations of POO and ONN. It can be observed that, for both switching states in Figure 5, line-to-line voltages are the same as

$$Vab = \frac{Vi}{2}, Vbc = 0, Vca = -\frac{Vi}{2}$$



(a) POO state (b) ONN state

Figure 5. An example of switching states of a three-level VSI

Note also that, for the POO state, the upper capacitor is discharged by phase **a** current, and for the ONN state, the lower capacitor is discharged by phase **a** current, while the output voltages are the same for both switching states. Space vector representation is a very useful and common method of analyzing three-phase converter circuits. As an example, switching states POO and ONN can be shown in a complex plane as in Figure 6, so that the projections of vector $\mathbf{V_{01}}$ on line-to-line voltage axes are as in Figure 5. This requires the magnitude of vector $\mathbf{V_{01}}$ to be $V_i/\sqrt{3}$ and the angle to be 0° The above mentioned 27 switching states can be expressed in terms of voltage space vectors as in Figure 7.

The switching vectors of the three-level VSI can be divided into four groups according to their magnitudes: zero vectors, small vectors, $\mathbf{V_{01}}$, ..., $\mathbf{V_{06}}$, medium vectors, $\mathbf{V_{12}}$, ...$\mathbf{V_{61}}$, and large vectors, $\mathbf{V_1}$, ..., $\mathbf{V_6}$. Different switching vectors have different effects on the charge balance of the midpoint, output ripple, and switching loss. Each small vector represents two different switching combinations, positive and negative.

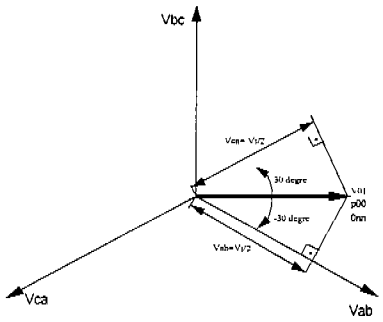


Figure 6. Representing switching states POO and ONN in space vector form.

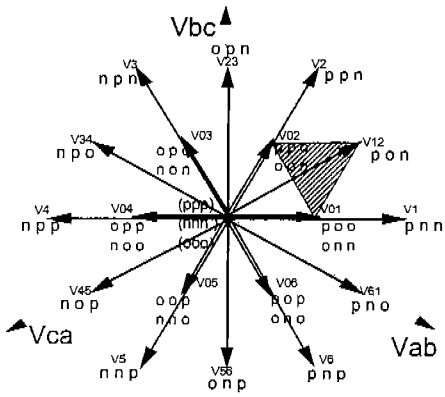


Figure 7. Space vector representation of three-level VSIs

For example, vector $\mathbf{V_{01}}$, when it is obtained from the combination POO, is called a positive-combination-vector ($\mathbf{V_{01p}}$), or, when it is obtained from the negative combination, ONN, is called ($\mathbf{V_{01n}}$). Both vectors produce the same output voltage, but when the positive vectors are applied, the upper capacitor is charged or discharged, and when the negative vectors are applied, the lower capacitor is charged or discharged. This property of the small vectors provides the freedom which can be used to control the charge balance of the midpoint. Combinations that produce medium vectors also affect the midpoint voltage, but there is only one combination for each vector. The large vectors and the zero vectors do not change the voltage of the midpoint. In terms of line-to-line voltages, the magnitude of the large vectors is $2V_i/\sqrt{3}$, and the magnitude of small vectors is $V_i/\sqrt{3}$. The magnitude of the medium vector is equal to

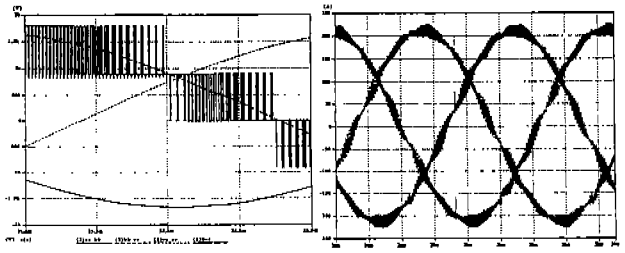
V_i, which is the same as the radius of a circle inscribed into the large hexagon in Figure 7. Therefore, the maximum amplitude of undistorted output line voltage is V_i. The desired output line voltage vector in steady state can be represented as:

$$V = d_m \cdot V_i \cdot e^{j\omega t}$$

where $0 \le d_m \le 1$ is the modulation index, and ω is the frequency of the output voltage.

5. SIMULATION RESULT

A 150-kW three-level VSI from Figure 3 was simulated using SABER. The proposed SVM was programmed in the MAST language of SABER. It can be observed that the transitions between the triangles in SVM are smooth, although the line voltages have distinct multilevel shapes, as seen in Figure 8(a). Figure 8(b) shows the simulated line currents in steady state.



(a) line-to-line voltage (b) line currents

Figure 8. Simulations of the three-phase VSI

6. SOFT SWITCHING

Soft-switching techniques are very important for reducing the switching loss, stress, and noise of multi-level three-phase converters. For the high-power, high-voltage application, the soft switching circuit has to be out of the main power path, the voltage stress of the auxiliary switch should not exceed that of the main switch, the soft switching should be helpful to both turn-on and turn-off of the main switch, and the auxiliary switch should also have to be soft switched. An example boost converter of the proposed ZCT topology that will satisfy those requirements is shown in Figure 9. The topology not only provides for the ZCT operation of the main switch but also helps reduce the main diode current to zero by turning on the auxiliary switch before the main switch is turned on. Figure 10 shows the key waveforms of the topology.

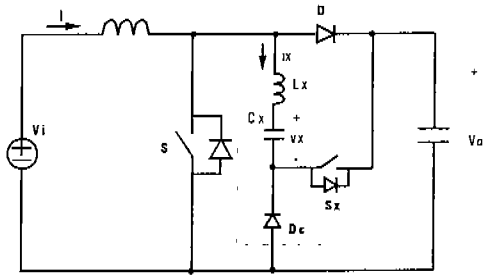


Figure 9. A ZCT boost converter

Figure 11(a) shows an experimental comparison of switching energy loss of the hard switching and the soft switching, and Figure 11(b) shows experimental waveforms of the voltage spike and the energy loss at the main switch.

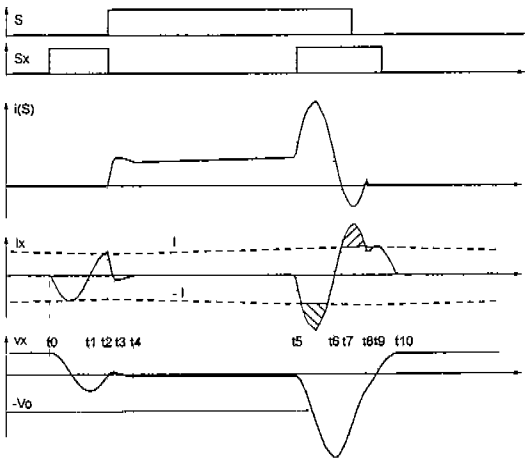


Figure 10. Operational waveforms of the improved ZCT PWM converter

Figure 12 shows one leg of the three-level VSI with ZCT bridges.

7. POWER STAGE SETUP

The one leg of the three-level VSI as a basic PEBB cell is constructed as in Figure 13. Four of the main switches, S1 to S4, and two of the diodes, D1 and D2, are placed in series, as in the schematic diagram. Two auxiliary switches, Sx1 and Sx2, are placed at both ends of the main switch array. For the connection between devices, 1.6-mm-thick copper plate bus bars are used to reduce parasitic inductance. The three-

level DC-link is made with three laminated buses. To generate the desired gate drive signals, a 32-bit DSP and programmable logic devices are used.

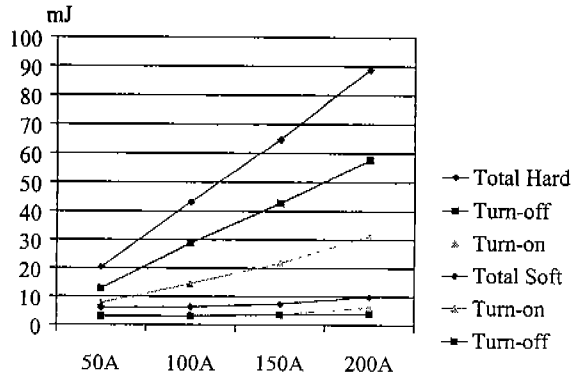


Figure 11. Switching energy loss comparison

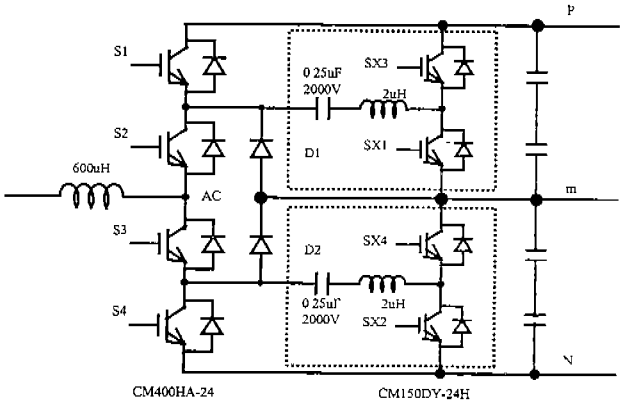


Figure 12. PEBB leg with soft-switching bridges

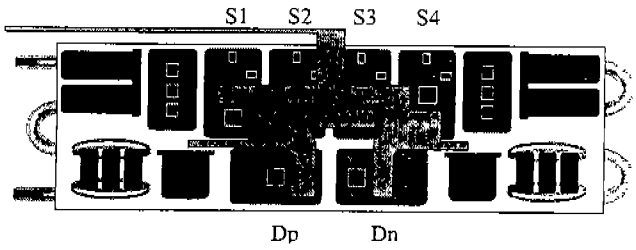


Figure 13. Device layout of the PEBB leg

Five of the PEBB legs were built and tested individually by operating the leg as a half bridge AC VSC with four-quadrant operation. After successful test of the legs, three of the PEBB legs were used to build the VSC, and two simplified legs were used to build the chopper. Figure 14 shows experimental setup of the overall power stage of the system. Each of the PEBB legs are placed vertically with the inlet of cooling water downward. All of water path of the leg are connected in parallel and share one chiller. Voltage and current sensors for DC link and output lines are galvanic isolated. Two of 1000-V 100-A DC power supplies and a 200-kW water heater are used as input power source and load simulator. The system is controlled by 32-bit DSP with space vector modulation (SVM) and DQ coordinate transformation.

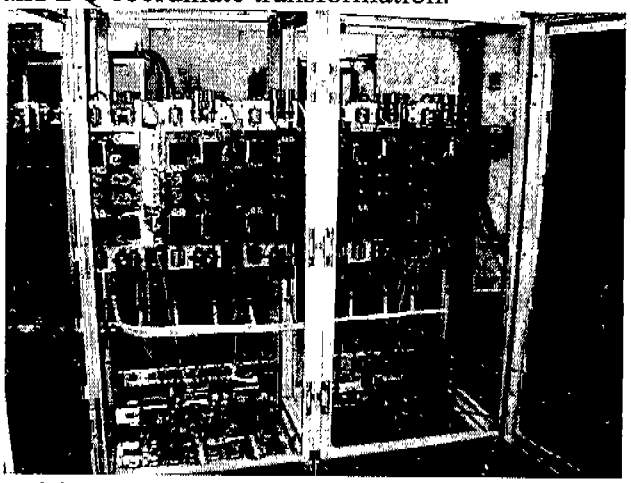


Figure 14. Experimental setup of the system

8. EXPERIMENTAL RESULTS

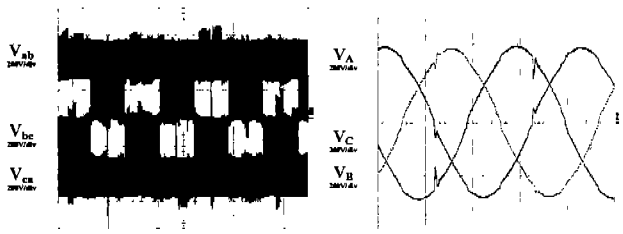
Figure 15(a) shows three-phase line-to-line voltage waveforms of the VSC and (b) shows phase voltages of the resistor load bank. The line-to-line voltage waveform shows the three-level operation clearly.

Figure 16 shows measured transfer function of v_d/d_d of the power stage. The measurement was made with DAC with 20-kHz sampling. The measurement itself shows 30° phase margin at 2-kHz. Considering the delay induced with DSP processing, the power stage transfer function has wider dynamic range than what is measured.

9. CONCLUSIONS

A soft-switching PEBB-based high-voltage high-power three-level VSI and chopper were designed, constructed using IGBT and tested. The system can be PWMed up to 20-kHz. The system can be used for the SMES PCS. Dynamic

range of the power stage is extended up to 2-kHz.



(a) Line-to-line (b) Phase

Figure 15. Three-phase output voltage waveforms

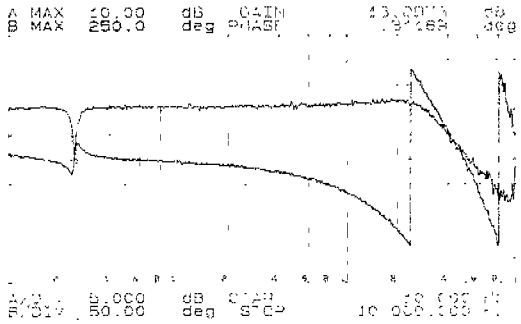


Figure 16. Power stage transfer function

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