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A New Isolated Boost Push-Pull Power Conversion Circuit with Distributed Current and Integrated Magnetic Structure

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Abstract

An improved current-fed push-pull PWM converter with integrated magnetics is presented. With this improved topology, the design of magnetic elements such as an inductor and a transformer becomes easier than that using the conventional topology, especially when the converter is suffered from an extremely high input current. Since this gives twice the voltage conversion ratio compared to the conventional one, it is also suited for the high voltage step-up power conversion process. The operation of the proposed converter is thoroughly analyzed. Also, the theoretical analysis and experimental results are taken from the laboratory level prototype.

I. Introduction

Most of high power level dc/dc converters have been designed to have high voltage and low current for the purpose of improving the efficiency and reducing the device ratings since the considered power source is the universal line voltage in general. However, when the battery is used as a main voltage source. it is essential to install a step-up dc/dc converter because of the low voltage and high current characteristics of the battery itself. At high power levels. the full bridge buck-derived dc/dc converter with isolation from the intermediate high frequency ac link is the preferred topology[6-8]. The main advantages of this topology include the constant frequency operation. PWM control, minimum VA stresses, wide control range, and controllability. However. when this is used as a battery powered converter, it requires large device current ratings and a step-up transformer with large turn ratio in order to provide the high output voltage at minimum controllable duty cycles. Moreover, there is no way of limiting the current drawn from the battery during the turn-on/turn-off of the power switch or various fault conditions in this topology since the source impedance of the battery is low. Therefore. this topology employing large current rating devices and a transformer with large turn ratio is generally not adequate for use in a low voltage battery powered converter.

In order to overcome the problems mentioned above, a current-fed push-pull PWM topology[1-5] can be used in a battery powered converter because it requires less device current ratings and a transformer with appropriate turn ratio than those of full bridge counter parts. The high instantaneous impedance of an inductor is interposed between the power source and the topology itself, which provides a number of significant advantages. especially in high power supplies (>1000W) and high output voltage supplies (>200V)[1]. However, two high current primary windings of the transformer make it difficult to achieve simultaneously a low profile PCB winding design and a high efficiency since each high current primary winding may require several layers of copper in parallel. Furthermore, termination issues related to the primary winding such as a narrow termination area, may increase the packaging complexity and the power loss. Two magnetic components used for an input inductor and an center-tapped transformer, also result in a bulky and heavy power system and increasing the interconnection power loss. Although the required turn ratio is smaller than that required in a full bridge counterpart, it is still large. Therefore, the design of the transformer is difficult and complex when the required step-up voltage conversion ratio is ten times or above.

In this paper, a new current-fed push-pull converter with integrated magnetics is introduced. The proposed converter uses only one magnetic core and gives an effective solution of designing the inductor and transformer elements when the input current is high. Its performance characteristics are superior to those of a conventional current-fed push-pull converter, especially in case of high voltage step-up applications.

The basic principles of operation are analyzed and a design procedure is developed. Experimental results are then presented, which illustrate the converter function and verify the analysis discussed.

II. Operational principles

The circuit diagram of the proposed converter is shown in Fig.1 and its integrated magnetics realization of the power stage is shown in Fig.2. The switches and S_2 operate with the duty cycle of greater than 0.5 like that of the conventional push-pull boost converter. The windings *ab* and *cb* wound on the upper leg and bottom leg, form the inductances L_1 and L_2, respectively. The winding *de* in the center leg forms the secondary side of the transformer. Since the input current is divided into windings *ab* and *cb*, the required wire size of the windings which form the inductors is one half the conventional one. Moreover, there is no center tapped winding on the magnetic core essential to the conventional push-pull boost converter. These facts make the design and implementation of the inductors and transformer easier, and reduce the core losses compared to those of the conventional one.

For the analysis of a circuit operation, the assumptions are made as follows:

- all power semiconductors are ideal
- circuit operates in a steady state
- there is no leakage inductance in the integrated magnetics
- capacitor C_o is assumed to have a constant voltage V_o during a switching period
- the inductances L_1 and L_2 have same values.

The last assumption simply states that the number of turns in the winding ab, N_1, and that in cb, N_2, are same (e.g., $N_1 = N_2 = N$) and the area of upper leg A_1 and that of bottom leg A_2 are same (e.g., $A_1 = A_2 = A$) in the integrated magnetic core.

The key waveforms are shown in Fig.3 and three topological states are shown in Fig.4 for the proposed converter where the continuous conduction mode (CCM) operation is assumed. The detailed description of each topological state is given in the next.

Mode 1 ($T_0 - T_1$: M_1) : Mode 1 begins when both switches S_1 and S_2 are on at $t = T_0$ and terminates when the switch S_2 is turned off at $t = T_1 = dT_S$, where d is the overlapping duty cycle and T_s is the switching period. With the integrated magnetic structure shown in Fig.2, the flux relationships are always satisfied as follows:

$$\varphi_c = \varphi_1 - \varphi_2 \quad (1) \qquad \frac{d\varphi_c}{dt} = \frac{d\varphi_1}{dt} - \frac{d\varphi_2}{dt}. \quad (2)$$

By using the Faraday's law, the voltage equation in mode 1 can be expressed as $V_i = N_1 \frac{d\varphi_1}{dt} = N_2 \frac{d\varphi_2}{dt}$. (3)

Since the induced secondary voltage v_{de} can be obtained as

$$v_{de} = N_s \frac{d\varphi_c}{dt} = N_s \left(\frac{d\varphi_1}{dt} - \frac{d\varphi_2}{dt} \right), \quad (4)$$

this voltage is zero in mode 1 with the assumption that N_1 is the same as N_2. Then, all diodes are reverse biased and I_o is supplied from C_o, which is the same as the on time mode of the boost converter. Also, the voltages v_{ab} and v_{cb} are obtained as $v_{ab} = v_{cb} = V_i$. (5)

The currents $i_1(t)$ and $i_2(t)$ rise linearly with the slope of V_i / L.

Mode 2 ($T_1 - T_2$: M_2) : Mode 2 begins when the switch S_2 is off at $t = T_1$. Since the flux φ_2 cannot change instantaneously, an induced flux which has the same direction and magnitude as those of φ_2, is created at the center leg to maintain a constant flux. Thus, the induced voltage in the center leg v_{de} is now negative and its value is clamped to $-V_o$ since the diodes D_2 and D_3 are forward biased. By using the Faraday's law, the output voltage can be expressed as $V_o = N_s \frac{d\varphi_c}{dt}$. (6)

With the equations (2), (3), and (5), the voltage across the winding cb is obtained as $v_{cb} = -\frac{N}{N_s} V_o - V_i$. (7)

Consequently, the current $i_2(t)$ decreases linearly with the slope of $-(NV_o / N_s - V_i) / L$, while the current $i_1(t)$ rises linearly with the slope of V_i / L. In mode 2, the stored electromagnetic energy in the winding cb is transferred to the load, which is the same as the off time mode of the boost converter. The voltage across the switch S_2, $v_{s2}(t)$ is NV_o / N_s.

Mode 3 ($T_2 - T_3$: M_3) : Mode 3 begins when the switch S_2 is on again. The equivalent circuit for this mode is exactly the same as that of mode 1 as shown in Fig.4.(a).

Mode 4 ($T_3 - T_4$: M_4) : Mode 4 begins when the switch S_1 is off at $t = (1+d)T_s$. The induced voltage in the center leg v_{de} is now positive and its value is clamped to $+V_o$ since the diodes D_1 and D_4 are forward biased. The voltage across the winding ab is obtained as

$$v_{ab} = -\frac{N}{N_s} V_o - V_i. \quad (8)$$

The current $i_1(t)$ decreases linearly with the slope of $-(NV_o / N_s - V_i) / L$. In mode 4, the stored electromagnetic energy in the winding ab is transferred to the load. The voltage across the switch S_1, $v_{s1}(t)$ is NV_o / N_s.

III. A comparison with a conventional current-fed push-pull PWM converter

In this section, the effort is focused on comparing the characteristics of the proposed topology to those of the conventional push-pull boost converter. The detailed analysis is discussed below.

3.1. Voltage conversion ratio

The voltage conversion ratio M is found by applying the volt-second law to the winding cb using equations (5) and (7) as $V_i(1+d)T_S = \frac{N_s}{N} V_o - V_i(1-d)T_S$ (9)

Simplifying the above equation yields

$$M = \frac{V_o}{V_i} = \frac{2N_s / N}{1-d}. \quad (10)$$

The voltage conversion ratio M^* of the conventional one is expressed as [4] $M^* = \frac{V_o}{V_i} = \frac{N_s / N_p}{1-d}$. (11)

It is noted that the turn ratio N_s / N in the proposed converter has the same role as the turn ratio N_s / N_p in the conventional one. For given input and output voltage specifications, the required turns for the secondary winding of the transformer is one half compared to that of the conventional one, which also makes the design of the transformer core easy.

3.2. Voltage and current stresses

The average current of each inductor is reduced to 50% in the proposed topology since the input current is splitted into two inductors. To simplify the analysis, it can be assumed

that the inductors are sufficiently large enough to be approximated by current sources having values equal to one half the dc input current $I_i/2$. Then, from the waveforms shown in Fig.3, the average switch current $I_{sw,av}$ and the RMS switch current $I_{sw,rms}$, can be obtained as

$$I_{sw,av} = 0.5I_i \quad (12) \qquad I_{sw,rms} = 0.5I_i\sqrt{1+d'} \quad (13)$$

where $d' = 1-d$. The peak voltage of the switches, $v_{sw,pk}$, is NV_o / N_s. It is noted that the current and voltage stresses are the same as those of conventional one since the required turn ratio is one half for given input and output voltage specifications.

The peak current $I_{do,pk}$ and RMS current $I_{do,rms}$ of output diodes are obtained as

$$I_{do,pk} = \frac{NI_i}{2N_s} \quad (14) \qquad I_{do,rms} = \frac{NI_i}{2N_s}\sqrt{d}. \quad (15)$$

Compared to those of the conventional one[4], the diode current stresses become one half.

3.3. Input current ripple

The current flowing through each input inductor can be expressed as

$$i_1(t) = \frac{I_i}{2} + \Delta i_1(t) \quad (16) \qquad i_2(t) = \frac{I_i}{2} + \Delta i_2(t) \quad (17)$$

where $\Delta i_1(t)$ and $\Delta i_2(t)$ are the current ripples of L_1 and L_2, respectively. Since the instantaneous input current $i_i(t)$ is $i_1(t)+i_2(t)$, the input current ripple $\Delta i_i(t)$ can be expressed as $\Delta i_i(t) = \Delta i_1(t) + \Delta i_2(t)$. (18)

It is found from Fig.3 that the maximum input current ripple occurs at time $t = T_1$. Substituting $t = T_1$ into the input current ripple obtained in the equation (18), the maximum input current ripple, $\Delta i_{i,pk}$ can be obtained as

$$\Delta i_{i,pk} = \frac{2V_i}{L} dT_s. \quad (19)$$

The maximum input current ripple of the conventional one, $\Delta i_{i,pk}^*$, is expressed as[2-3] $\Delta i_{i,pk}^* = \frac{V_i}{L} dT_s$. (20)

Comparing the equation (19) with (20), the input current ripple is twice that of the conventional one. It is noted, however, that the physical size of an inductor is approximately proportional to its energy storage, i.e., the inductance times the square of the current. Since the two inductors share the input current, each inductor has twice the inductance by keeping the total size constant. Thus, it can be designed that the input current ripple of the proposed converter is the same as that of the conventional one without increasing the core size. Consequently, the advantages of the proposed converter are that the design of the magnetic cores and the selection of the power switches are easier than those of the conventional one, especially when the input current and output voltage are high.

3.4. Critical load resistance (DCM/CCM conditions)

by inspecting the circuit operations, the critical load resistance R_c is obtained a $R_c = \frac{8 \cdot L \cdot (N_s/N)^2}{T_s \cdot (1+d)^2 \cdot (1-d)^2}$.

To operate the proposed converter in the CCM, the load resistance should be smaller than the critical resistance obtained above. In other words, for a given minimum load power specification, the selection of L and d should be done so as not to enter the DCM operation.

IV. Experimental Results

To experimentally characterize the proposed converter, a prototype has been constructed using the components listed in Table. I. The controller is based on the integrated PWM chip UC3823 from Unitrode, which is the same one used for the conventional dc/dc converter.

Fig.6 shows the switch current and voltage waveforms of the proposed converter. The peak current and voltage of the switch S_1 are 5A and 40V, respectively. Since there exists a voltage surge whose magnitude is about 120V at turn-off instant due to the leakage inductance of the integrated magnetics, a voltage clamp circuit is needed as in the conventional dc/dc converter. It is, however, noted that the peak amplitude of the surge voltage is proportional to the leakage inductance times the square of the peak primary current. The conventional converter will feature much higher surge voltage since the current flowing through the primary winding is the same as the input current. This fact makes the design of a clamp circuit easier to dissipate the leakage energy with the proposed topology. Fig.7 shows the inductor current waveforms of $i_1(t)$ and $i_2(t)$, respectively. The average current and peak-to-peak ripple are estimated to be 2A and 2.4A, respectively. It can be seen that the average current of each winding is one half the input current of 4A. Fig.8 shows the waveforms of the secondary voltage v_{dc} and the output diode current i_{do1} or i_{do2}. The peak voltage of v_{dc} is 150V and the peak diode current is estimated to be 1.1A. It clearly shows that the waveforms are well agreed with the theoretical analysis. Fig.9 shows the waveforms of the input current $I_i(t)$ and the voltage v_{ac} which serves as a voltage applied to the primary side of the transformer. Due to interleaving characteristics of $i_1(t)$ and $i_2(t)$, the input current ripple is tolerable even though the current ripple of each winding is large. The peak-to-peak ripple of the input current is 1.2A and the average current is 4A. As for the voltage waveform of v_{ac}, it shows the same wave shape as that of v_{dc} except the generated surge.

VII. Conclusion

In this paper, an improved current fed push-pull dc/dc converter topology is presented, which offers the following distinctive features over a conventional dc/dc converter:

- two times higher step-up voltage conversion ratio
- smaller primary wire size
- only three interconnection at primary side
- higher power density.

In the conventional approach based on a current-fed push-pull dc/dc converter, it is hard to achieve a high step-up voltage conversion ratio, and is difficult to design magnetic elements due to the center-tapped feature of a transformer. The detailed analysis and design considerations

for the proposed converter are described. The prototype has been built to verify the proposed topology. The proposed dc/dc converter is well suited for high step-up voltage and large input current applications such as electric vehicles and fuel cell.

References

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[2] V.J.Thottuvelil, T.G.Wilson, and H.A.Owen Jr, "Analysis and design of a push-pull current fed converter", Proceedings of the Power Electronics Specialists Conference, pp.192-203, 1981.

[3] N.H.Kutkut, D.M.Divan, and R.W.Gascoigne, "An improved full bridge zero voltage switching PWM converter using a two inductor rectifier", IEEE Transaction on Industry applications, vol.31, no.1, pp.119-126, January 1991.

Input voltage V_i	15 V DC
Load resistor R_o	500 Ω
Switching frequency f_s	100 KHz
Core	E55 / PC30 (TDK Inc.)
Inductor turns N	18 (turns)
Secondary turns N_s	52 (turns)
Air gap l_g	1.1 mm
Switch (S_1, S_2)	IRFP250 (MOSFET)
Diode ($D_1 \sim D_4$)	SD15034 (fast recovery)
Capacitor C_o	2200 uF

Table. II. List of parameters

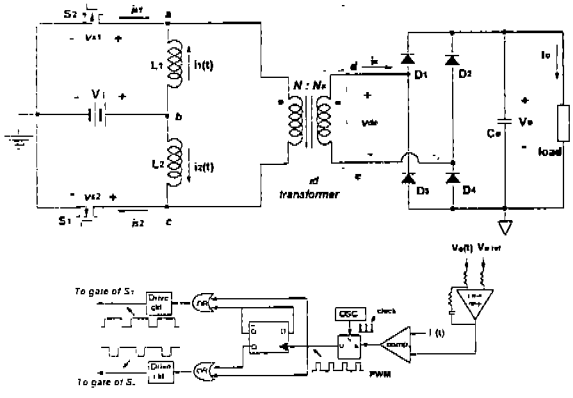

Fig.1. The circuit diagram of the proposed current-fed push-pull PWM converter

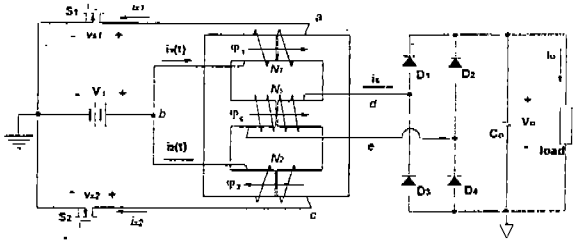

Fig.2. The integrated magnetics realization of the proposed converter ($N_1 = N_2 = N$)

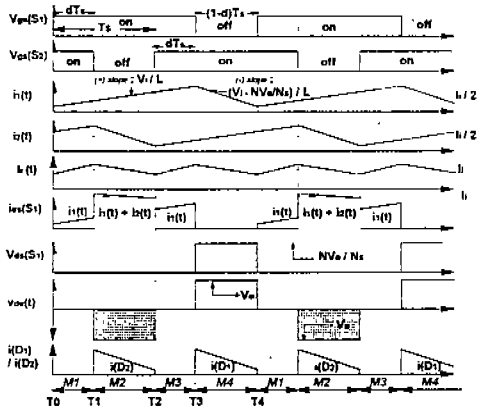

Fig.3. The key waveforms of the proposed converter operated in CCM

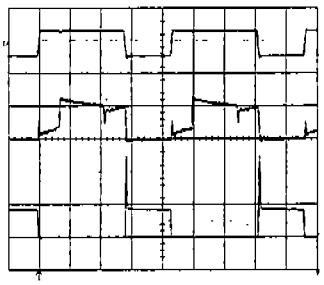

Fig.4. The switch waveforms (*time:5us / div*) : 1st trace: $V_{gs}(S_1)$@20V / div ; 2nd trace: $i_{ds}(S_1)$@4 A / div ; 3rd trace : $V_{ds}(S_1)$@50V / div ;

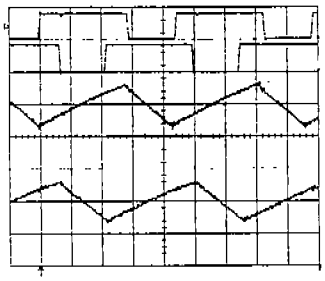

Fig.5. The inductor current waveforms (*time:5us / div*) : 1st trace: $V_{gs}(S_1)$@20V / div ; 2nd trace: $V_{gs}(S_2)$@20V / div ; 3rd trace: $i_1(t)$@2 A / div ; 4th trace : $i_2(t)$@2 A / div ;