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자기결합 무손실 스너버를 갖는 새로운 고역률 단일전력단 AC/DC 컨버터

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Single-Stage Single-Switched AC/DC Converter with Magnetic Coupled Nondissipative Snubber

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Abstract

A new single-stage/single-switched forward converter with magnetic coupled nondissipa-tive snubber is proposed. The proposed converter gives the good power factor correction (PFC), low current harmonic distortion, and tight output voltage regulation. The prototype shows the IEC 555-2 requirements are met satisfactorily with nearly unity power factor. This proposed converter with magnetic coupled nondissipative snubber is particularly suited for low power level power supply applications.

I. Introduction

With the adoption of standards such as IEC555-2, there is a need to look for a converter which can do harmonics rectification, power factor correction, isolated dc-dc conversion, and tight output voltage regulation [1-3]. Such a converter needs to meet the IEC555-2 requirements without adding many components, especially in a low power level system such as computer power supplies. The conventional PWM boost rectifier, operating in a continuous conduction mode(CCM) for power factor correction, is widely used because of its continuous line current, smallest choke, minimum current distortion, and lowest current stress than other methods [4-5]. However, a conventional boost converter requires an additional dc/dc converter in order to provide the output isolation and to give the output voltage lower than the peak input voltage. Therefore, this scheme with its reactive elements, power switches, controllers, and switch drivers, is generally expensive and complex. These prevent the application of a boost converter from low power level power supplies.

Recently, several power conversion topologies have been suggested as a simple high power factor rectifier/regulator. These include a single-ended primary inductance converter (SEPIC) and a flyback converter which perform the power factor correction and isolated output voltage regulation in a single-stage at the expense of the increased high frequency line current distortion [6-7]. Furthermore, the output voltage regulation has a low bandwidth in order to minimize distortions in the input current. Those problems can be overcome with the Integrated High Quality Rectifier/ dc Regulator(IHQRR) and Boost Integrated Flyback Rectifier Energy Dc-dc converter(BIFRED) [1-2], which offer a low cost alternative to more conventional methods of power factor correction while providing a well regulated output voltage and an isolated power conversion. The drawback of BIFRED or IHQRR is, however, a relatively high voltage stress suffered by its switching component and dc-link capacitor due to the load dependent characteristics. In addition, there is a high current stress in a switching component because both the large input current in a discontinuous conduction mode (DCM) operation and the primary current of the transformer flow together into a power switch. These result in a significant

voltage ripple at twice the line frequency in the output voltage. The converter in [11] eliminates this problem, features an excellent output voltage regulation. The main disadvantages in [11] are considerable losses in the voltage-clamp circuit due to its dissipative snubber operation.

In this paper, a new converter based on a forward dc-dc converter with nondissipative LC snubber is introduced. The proposed converter is capable of drawing high quality current waveforms from the ac power source by using a magnetic coupled nondissipative snubber, successfully reducing the surge generation without increasing the power dissipation. Furthermore, a regulated dc output with the fast transient response can be obtained in a single-stage/single-switch with the relatively reduced device stress suffered by a power switch. The basic principle of operation is analyzed and a design procedure is developed. Experimental results are then presented, which illustrate the converter function and verify the analysis presented.

II. Operational Principles of the Proposed Converter

Fig.1 shows the proposed high power factor converter with a magnetic coupled snubber stage. This converter resembles after the forward converter with nondissipative LC snubber, where L_{lk} represents the total transformer leakage inductance reflected to the primary side. The most obvious difference is the magnetic coupled stage in an input side section wound on the inductor core of the nondissipative snubber. This magnetic coupled winding generates a switching frequency modulated voltage V_t which is the reflected voltage from the primary side of a nondissipative snubber inductor during the turn off time of the power switch Q. This high frequency content of V_t is filtered by the inductor L_i to produce an output V_x which adds to V_t. The dc link capacitor C_{DC} is the energy storage capacitor required to store the $120Hz$ ripple energy needed in a single-phase high power factor converter.

For the analysis of a circuit operation, the following assumptions are made:

- all power semiconductors are ideal.
- the circuit operates in a steady state.
- the output filter inductance L_o is sufficiently large to be approximated by a current source with a value equal to the load current I_o.
- L_{lk} is much less than the transformer magnetizing inductance L_m.
- dc link capacitor volotage V_{dc} is larger than the rectified peak input voltage V_i.
- V_i is considered as constant during a switching cycle because the switching frequency is much higher than the line frequency.
- prior to turning the switch Q on, the snubber capacitor is charged to the voltage $V_{c,max}$ which is less than the dc link capacitor voltage V_{DC}.
- $\frac{\pi}{2}\sqrt{L_pC} > T_{on}$.

The last assumption simply states that one-quarter of the resonant period formed by Lp and C is larger than the maximum on-time of the switch Q, which is not the usual case of a forward converter with nondissipative LC snubber (see Ref[10]). Actually, the stored electromagnetic energy in L_p during the on-time of the switch Q is transferred to the input side section to form the voltage V_x. In this sense, the magnetic coupled snubber stage forms an another power conversion circuit, in which the output voltage is V_x and the input source is the stored electromagnetic energy in L_p, or the magnetizing energy in L_m.

Fig.2 shows the five topological states and the key waveforms are shown in Fig.3 for the proposed converter in which the magnetic coupled stage operates discontinuously. The detailed description of each topological state is given in the next:

Mode 1 ($T_0 - T_1$: M_1) : As can be seen in Fig.3, the operation of mode 1 is the same as that of on-time mode in a conventional forward converter. Thus, the currents in the primary winding of a transformer and the output inductor L_o rise linearly. At T_1, the magnetizing current i_{Lm} can be expressed as

$$i_{Lm}(T_1) = i_{Lm,pk} = \frac{V_{DC}}{L_m} DT_s \qquad (1)$$

where D is the duty ratio and T_s is the switching period. In mode 1, the stored energy in the snubber capacitor C is transferred through the diode D_{12} to the snubber inductor L_p in a resonant manner. Therefore, the current flowing through L_p, i_{Lp}, and the voltage across C, v_c, can be written as

$$i_{Lp}(t) = V_{c,max}\sqrt{\frac{C}{L_p}}\ sin\frac{t}{\sqrt{L_pC}} \qquad (2)$$

$$v_c(t) = V_{c,max}\ cos\frac{t}{\sqrt{L_pC}}. \quad (3)$$

On the other hand, the diode D_i in the magnetic coupled stage is reverse biased because the undotted end of the primary winding of the snubber inductor L_p is negative with respect to the dotted end. Thus, the current flowing through the inductor L_f is zero. It is noted that the switch Q should be off before $v_c(t)$ goes to negative. Otherwise, immediately after v_c goes to negative, the diode D_i will be forward biased and the current i_{Lf} will flow, which results in a significant low frequency ripple at the output stage. Therefore, the assumption that $\frac{\pi}{2}\sqrt{L_pC} > T_{on}$ is needed in the proposed converter to assure $v_c(t)$ is always positive.

Mode 2 $(T_1 - T_2 : M_2)$: Mode 2 begins when the switch Q is turned off at T_1. Since the current flowing through the primary winding of a transformer is now interrupted, the voltage across the primary winding reverses its polarity to oppose this change. As such, the voltage at the dotted end of a transformer winding is now negative with respect to the undotted end. The clamp diode D_{11} connected between the dotted end of the primary winding of a transformer and the snubber capacitor C prevents this voltage from falling below $-v_c(t)$. Hence, the rectifier D_{o1} is reverse biased. At the same time, the freewheeling diode D_{o2} is forward biased and allows the output inductor L_o to discharge its stored energy to satisfy the load requirements.

In mode 2, the stored energy in the magnetizing inductance L_m and the leakage inductance L_{lk} is transferred through the diode D_{11} to the snubber capacitor C in a resonant manner. This energy shift finishes at T_4, when the magnetizing current becomes zero. Since the diode D_{11} conducts, the voltage across the primary winding of a snubber inductor L_p is clamped to $-V_{DC}$ and remains there throughout mode 2. Since L_p and L_s are wound on the same core as shown in Fig.1, the undotted end in L_s is positive with respect to the dotted end. This voltage $(V_t = nV_{DC})$ forces to increase the current i_{Lf} lineary as shown in Fig.3, with the positive slope of $(V_i + nV_{DC} - V_{DC})/L_f$. To explain the modes 2 and 3, the switching waveforms of various currents with their slopes are depicted in Fig.4. As can be seen in Figs.2 and 4, the current flowing through the diode D_{12} is

$$i_{D12}(t) = i_{Lp}(t) - ni_{Lf}(t) \quad (4)$$

where it is assumed that $i_{Lp}(t) \approx i_{Lp}(T_1) = V_{c,max}\sqrt{\frac{C}{L_p}}sin\frac{DT_s}{\sqrt{L_pC}}$ during mode 2 interval since L_p is large enough to neglect the variation of $i_{Lp}(t)$. At T_2, the current i_{Lf} can be written as

$$i_{Lf}(T_2) = i_{Lf,pk} = \frac{V_i + nV_{DC} - V_{DC}}{L_f}t_c \quad (5)$$

where t_c is the duration of mode 2. From Fig.4, the current slope of i_{D12} during mode 2 can be obtained as

$$slope\ of\ i_{D12}|_{modc2} = -(\frac{V_{DC}}{L_p} + n\frac{V_i + nV_{DC} - V_{DC}}{L_f}). \quad (6)$$

During mode 2, the stored energy in the primary snubber inductor L_p is transferred to the magnetic coupled stage. Mode 2 ends when the diode D_{12} stops conducting. Using the equations (5) and (6), the duration of mode 2,t_c,can be easily obtained as follows:

$$t_c = \frac{L_pL_fV_{c,max}\sqrt{\frac{C}{L_p}}sin\frac{DT_s}{\sqrt{L_pC}}}{L_fV_{DC} + n(V_i + nV_{DC} - V_{DC})L_p}. \quad (7)$$

Mode 3 $(T_2 - T_3 : M_3)$: After the current i_{D12} is reduced to zero, the voltage $V_t = nV_{DC}$ can not force i_{Lf} to increase since the clamped voltage across the primary snubber inductor V_{DC} is not reflected to the magnetic coupled stage. Thus i_{Lf} decreases to zero during mode 3. This current has the negative slope of $(V_i - V_{DC})/(L_s + L_f)$. Using the current slopes shown in Fig.4, the duration of mode 3, t_d, can be easily obtained as follows:

$$t_d = \frac{L_s + L_f}{L_f}\frac{V_i}{V_{DC} - V_i}t_c. \quad (8)$$

Mode 4 $(T_3 - T_4 : M_4)$: After mode 3, the discontinuous current mode in the magnetic coupled stage is occurred. On the other hand, the stored energy in the magnetizing inductance is being shifted to the snubber capacitor via the path $D_{11} - L_m - C$. Mode 4 ends when the magnetizing current i_{Lm} becomes zero.

Mode 5 $(T_4 - T_5 : M_5)$: At T_4, when the magnetizing current becomes zero, the diode D_{11} is turned off. The voltage across the snubber capacitor at T_4 can be obtained as

$$v_c(T_4) = V_{c,max} \approx \sqrt{\frac{L_m}{C}}i_{Lm}(T_1) \quad (9)$$

or, more precisely, including the transformer leakage inductance L_{lk}, it becomes

$$V_{c,max} \approx \sqrt{\frac{L_m}{C} i_{Lm}(T_1)^2 + \frac{L_{lk}}{C}\left(\frac{I_o}{N}\right)^2}. \qquad (10)$$

This is derived from the fact that the stored electromagnetic energy in the magnetizing inductance L_m and the leakage inductance L_{lk} finishes shifting to the snubber capacitor at T_4. In practice, a numerical calculation is nessesary to find $V_{c,max}$ at various load condition. Note that in the proposed converter, the snubber capacitor C must be large enough so that the maximum voltage across the snubber capacitor $V_{c,max}$ is less than the dc link voltage V_{DC}. Otherwise, the diode D_{12} will conduct at T_4, resulting in an unwanted mode of operation of the proposed converter. During mode 5, the voltage across the snubber capacitor v_c remains $V_{c,max}$. When the switch Q is turned on at T_5, another switching cycle starts.

It is noted that the output current influences only during mode 1 and the PFC by using a magnetic coupled snubber stage is achieved only during modes 2 and 3. During modes 2,3,4,and 5, the output stage is not influenced by the rectified input voltage since the freewheeling diode D_{o2} is forward biased. Hence,the proposed converter is independent of the output voltage regulation and power factor correction which is not possible in a BIFRED. As a result, the output voltage ripple at twice the line frequency appeared in a BIFRED can be eliminated in the proposed converter. Usually, the dc link voltage V_{DC} is designed to be higher than the peak line voltage in the proposed converter. The voltage across the magnetic coupled stage in an input side section V_x should be equal to the dc link voltage minus the ac line rectified voltage. In order to achieve a high power factor, the peak value of i_{Lf} should be a rectified sinusoidal form. Then, the rectified line current $|i_{in}|$ will also be a rectified sinusoidal form due to the DCM operation of the magnetic coupled stage in an input side section. The required characteristics of the magnetic coupled stage in an input side section are shown in Fig.5. In the proposed converter, since V_t is nV_{DC} during mode 2, the average voltage of V_t over one switching cycle V_x is proportional to $nV_{DC}t_c$. When V_i is close to a zero voltage, t_c has its maximum value as can be seen in equation (7) for given parameters and V_x becomes a high voltage. When V_i is close to the peak voltage $V_{i,pk}$, t_c has its minimum value, and V_x becomes a low voltage. Moreover, the peak values of i_{Lf} will follow the high frequency voltage pulses $V_{Lf}(= V_i + nV_{DC} - V_{DC})$ whose amplitudes are modulated by a line voltage with dc offset $(n-1)V_{DC}$. If the turn ratio of a coupled snubber inductor n is set to one, only the rectified input voltage V_i is applied across the inductor L_f. Thus, the peak values of i_{Lf} follow the rectified input voltage V_i in this proposed converter. Therefore, the characteristics of the magnetic coupled snubber stage in the proposed converter are the same as those shown in Fig.5.

III. Analysis and Design Consideration

In this section, the effort is focused on the selection of important parameters such as the magnetic coupled nondissipative snubber, input inductor, switching frequency, magnetizing inductance, and turn ratio of transformer required in the proposed converter operation. The detailed analysis of the proposed converter will be described

To further simplify the analysis, it is assumed that the turn ratio of the magnetic coupled inductor is one,e.g., $L_p = L_s = L$, and $V_{c,max} \leq V_{DC}$ for any load conditions.

3.1. Selection of snubber capacitor and snubber inductor

In general, the snubber capacitance is selected such that the power loss of the switch will be minimized. The power loss has been estimated as a function of snubber capacitance using a simple switch model. Refer to Appendix for a detailed analysis.

Some examples based on a 900-V, 30-A IGBT are shown in Fig.6 as a function of snubber capacitance for a switched current of 5 A, which is the current needed for the proposed topology of a 100 W converter. Based on these results, it has been found that a switching frequency of around 100 KHz can be obtainable with a snubber capacitor of 22 nF. This gives the power loss of approximately 3.1W.

During the switch conduction period, a quarter-wave resonance arises through the snubber capacitor, magnetic coupled inductor, diode D_{12}, and switch Q. The magnetic coupled snubber inductor can be obtained from the assumption that $\frac{\pi}{2}\sqrt{L_p C} \geq T_{on}$ as follows:

$$L = \frac{1}{C}\left(\frac{2D_{max}T_s}{\pi}\right). \qquad (11)$$

From this equation, the required snubber inductor

L for $D_{max} = 0.4$ and $T_s = 10us$ is about 290 uH.

3.2. Charging and dischaging time of the input inductor

It is essential to choose a switching period greater than the sum of DT_s and $(t_c + t_d)$ to ensure that the coupled snubber inductor core is reset before starting the next switching cycle and the discontinuous current conduction occurs in the input current.

Substituting equation (9) into equation (7) gives the duration of mode 2, $t_c (= T_2 - T_1)$, as

$$t_c = \frac{L_f i_{Lm}(T_1)\sqrt{LL_m} sin\frac{DT_s}{\sqrt{LC}}}{L_f V_{DC} + LV_i} \tag{12}$$

where it is assumed that the effect of the leakage inductance is neglected to simplify the analysis. If the influence of a parasitic resistance on the output voltage V_o is neglected, then V_o can be obtained as follows:

$$V_o = \frac{V_{DC}}{N} D \tag{13}$$

where N is the turn ratio of the transformer. Substituting equations (1) and (13) into equation (12) gives

$$t_c = \frac{NV_o T_s \sqrt{\frac{L}{L_m}} sin\frac{DT_s}{\sqrt{LC}}}{V_{i,pk}(\gamma + \alpha sin\theta)}. \tag{14}$$

where $\alpha = L/L_f$, $\gamma = V_{DC}/V_{i,pk}$, and $\theta = w_L t$. From equation (8), the time interval $t_d (= T_3 - T_2)$ can be rewritten as follows :

$$t_d = \frac{(\alpha + 1)}{\gamma - sin\theta} t_c. \tag{15}$$

Then, $t_c + t_d$ as a function of θ can be expressed as

$$(t_c + t_d)(\theta) = \frac{NV_o T_s \sqrt{\frac{L}{L_m}} sin\frac{DT_s}{\sqrt{LC}}}{V_{i,pk}(\gamma + \alpha sin\theta)} - \frac{kT_s}{\gamma - \alpha sin\theta} \leq (1 - D_{max})T_s \tag{16}$$

where $k = NV_o\sqrt{\frac{L}{L_m}} sin\frac{DT_s}{\sqrt{LC}}/V_{i,pk}$. To satisfy this inequality (16), k should be designed to have a small value and γ should be designed to have a large value. The inequality (16) is less affected by α and T_s. In fact, α and T_s are related to the maximum obtainable output power as will be shown in a later section.

3.3. Line current distortions and power factor

It is noted that the input current waveform is not purely sinusoid and contains harmonic distortion due to the DCM operation. This can be represented by a function of k, α, and γ. From equation (5) and Fig.4, the average inductor current $I_{Lf,c}$ during the time t_c can be written as

$$I_{Lf,c}(\theta) = \frac{1}{2T_s} i_{Lf,pk} t_c = \frac{1}{2T_s} \frac{V_m sin\theta}{L_f} t_c(\theta) \tag{17}$$

while the average inductor current $I_{Lf,d}$ during t_d can be written as

$$I_{Lf,d}(\theta) = \frac{1}{2T_s} i_{Lf,pk} t_d = \frac{1}{2T_s} \frac{V_m sin\theta}{L_f} t_d(\theta). \tag{18}$$

Then, the average current $I_{Lf,av}(\theta) (= |I_{in}(\theta)|)$ can be found by the sum of $I_{Lf,c}$ and $I_{Lf,d}$ over a switching period T_s as

$$I_{Lf,av}(\theta) = I_{Lf,c} + I_{Lf,d} = \frac{1}{2T_s} \frac{V_m sin\theta}{L_f} t_c(\theta). \tag{19}$$

Using equation (19), the power factor can be expressed as

$$p.f = \frac{P_i}{V_{i,rms} I_{in,rms}} \tag{20}$$

where

$$P_i = \frac{1}{\pi} \int_0^{\pi} V_m sin\theta I_{Lf,av}(\theta) d\theta \tag{21}$$

and

$$V_{i,rms} I_{in,rms} = \sqrt{(\frac{1}{\pi} \int_0^{\pi} {I_{Lf,av}}^2(\theta) d\theta)} \frac{V_{i,pk}}{\sqrt{2}}. \tag{22}$$

The rectified input current waveforms of $i_{Lf,av}$ and the corresponding power factors for several values of k, α, and γ are plotted in Fig.7 provided that $(t_c + t_d)_{max} \leq (1 - D_{max})T_s$.

It can be concluded that the high power factor of better than 0.98 for any specific parameter sets can be obtained.

3.4. DC link voltage stress and ouput power

By applying the input-output power balance principle, the dc link voltage V_{DC} can be expressed as

$$\frac{\alpha N^2 {V_o}^2 T_s sin\frac{DT_s}{\sqrt{LC}}}{2\pi L_m P_o} \int_0^{\pi} \frac{sin^2\theta}{(V_{DC}/V_{i,pk} - sin\theta)(V_{DC}/V_{i,pk} + \alpha sin\theta)} d\theta = 1. \tag{23}$$

Fig.8 shows a plot of the dc link voltage as a function of the output power for different switching frequencies. As can be seen in this figure, V_{DC} increases as output power decreases. Hence, it is recommended to use the variable switching frequency control described in [12].

Once the dc link voltage is obtained, it is straightforward to determine the switch voltage/current stress. From Fig.3, the peak switch voltage, $V_{ds,pk}$, is expressed as

$$V_{ds,pk} = V_{DC} + V_{c,max} \leq 2V_{DC} \qquad (24)$$

and the peak switch current, $i_{ds,pk}$, is expressed as

$$i_{ds,pk} = i_{Lm}(T_1) + \frac{I_o}{N} + i_{Lp}(T_1) \leq \frac{V_{DC}}{L_m} D_{max} T_s + \frac{I_{o,max}}{N} + \frac{V_{DC}}{L} D_{max} T_s \qquad (25)$$

where $I_{o,max}$ denotes the full load current.

To maximize the output power P_o, it is desirable to select N, T_s as large as possible and L_f and L_m as small as possible. However, it is noted that there exist a maximum bound on N and a minimum bound on L_m as indicated previously. Therefore, a low switching frequency f_s is to be selected to increase the output power P_o, which results in a reduced overall effieciency and a increased converter size. A small input inductance L_f should be designed with large core geometry and air gap to avoid magnetic saturation (see Ref[8]), which results in a reduced overall effieciency.

IV. Experimental Results

To experimentally characterize the magnetic coupled snubber technique in a single-stage PFC application, a breadboard model has been constructed using the following parameters listed in Table I. The controller is based on the integrated PWM chip UC3823 from Unitrode, which is the same one used for the conventional dc/dc converter.

Table 1: Proposed converter parameters list

T_s	10us	R_o	3 ohm
L	250uH	C	22nF
L_m	480uH	N	6
L_i	200uH	C_i	1uF
L_o	36uH	C_o	330uF
L_f	50uH	C_{DC}	220uF

Fig.9 shows the experimental waveforms of the breadboard circuit operating at 60V dc input. All the top traces in Fig.9 represent the gate drive voltage $V_{gs}(Q)$ with its duty ratio D of 0.3. Fig.9(a) shows the switch voltage v_{ds} and current i_{ds}. The peak switch voltage is limited to 200V, and the peak switch current is 5 A. This peak switch current consists of three parts: the magnetizing current $i_{Lm}(T_1)$ of 1.7 A, the primary side current reflected from the load current $\frac{I_o}{N}$ of 0.8A, and the peak value of the snubber inductor current $i_{Lp}(T_1)$ of 2.5 A. Fig.9(b) shows the snubber capacitor voltage $v_c(t)$ and snubber inductor current $i_{Lp}(t)$. It is noted that one-quarter of the resonant period formed by L_p and C is equal to the on-time of Q (e.g. $\frac{\pi}{2}\sqrt{L_pC} = T_{on}$) for this operating condition. Fig.9(c) shows the voltage across the input inductor $v_{Lf}(t)$ and the input inductor current $i_{Lf}(t)$. It can be observed that $t_c + t_d$ is less than $0.5DT_s$, so it is not a problem to select the duty ratio D as 0.4, which is the same as that of the conventional forward converter. Fig.9(d) shows the voltage across the snubber inductor $v_{Lp}(t)$ and the snubber capacitor current $i_c(t)$. During the on-time of Q, $v_{Lp}(t) = -v_c(t)$, and $i_c(t) = -i_{Lp}(t)$. However, during the off-time of Q, $v_{Lp}(t)$ becomes V_{DC} during mode 2, $(V_{DC} - V_i)L_s/(L_f + L_s)$ during mode 3, or zero during modes 4 and 5. Also, $i_c(t)$ becomes $i_{Lm}(t) + i_{D12}(t)$ during mode 2, $i_{Lm}(t)$ during mode 3, or zero during modes 4 and 5. Fig.9(e) shows the primary transformer voltage and the output inductor current. It can be seen that, at turn-on transition, there exists a current ringing in the output inductor current waveform. This current ringing is mainly due to the reverse recovery problem of the output rectifiers D_{o1} and D_{o2}. Fig.9 shows that all the waveforms are agree well with the theoretical analysis.

Fig.10 shows the turn-on/turn-off transient waveforms of the main power switch Q. It can be observed that, at turn-on transient, there is a switch current ringing due to the reverse recovery problem of the output rectifiers D_{o1} and D_{o2}. During the turn-on time, the falling V_{ds} intersects the rising I_{ds} at a quite low current value. Therefore the integral $\int V_{ds} I_{ds} dt$ taken over the turn-on time is small so that the average dissipation over a full cycle is also small, as is expected in the conventional transformerized converter. Furthermore, during the turn-off time, the rising V_{ds} intersects the falling I_{ds} at a quite low voltage value so that the integral $\int V_{ds} I_{ds} dt$ taken over the turn-off time is small in the proposed converter. Fig.11 shows the dc link waveforms for the power factor correction operation. It is quite clear that the power factor correction has been achieved by the magnetic coupled snubber stage. Fig.12 shows the oscillograms of the line current and voltage. The line current shows the sinusoidal waveform keeping in-phase with the

line voltage. Thus, the high power factor can be obtained by using the proposed magnetic coupled snubber technique. Fig.13 shows the oscillograms of the output voltage V_o, output inductor current i_{Lo}, and rectified input voltage $|V_i|$ at full load. It can be seen that low frequency ripple components are small in the proposed converter with a magnetic coupled nondissipative snubber. Fig.14 shows the overall efficiency and the power factor as a function of the output load for low and high input voltages (100Vrms and 120Vrms). It can be seen that the efficiency of the proposed converter is 84 % at full load, which is better than that of other single-stage converter such as a BIFRED. The power factor stays relatively high for the entire load range. Fig.15 shows the measured line current harmonics superimposed on the specified IEC555-2 Class D limits. This clearly shows that the proposed converter meets the regulation with a considerable margin, and the measured power factor is 0.978.

V. Conclusion

In this paper, a single-stage,single-switch isolated ac/dc converter topology, based on a forward converter incoporating the magnetic coupled nondissipative snubber technique, is presented. The proposed new magnetic coupled snubber based technique gives the good power factor correction and low line current harmonic distortions with high efficiency. Furthermore, the proposed converter is capable of producing an isolated output voltage regulation in a single-stage and single-switch without the significant output voltage ripple at twice the line frequency. The analysis and design consideration for the proposed converter are described. Based on this analysis, nearly optimal values for the magnetic coupled snubber components are selected for the high efficiency operation of the proposed converter. The prototype successfully meets the IEC555-2 requirements with a efficiency of above 84 % . Thus, the proposed converter is best suited for low power applications where the cost is one of the prime objectives.

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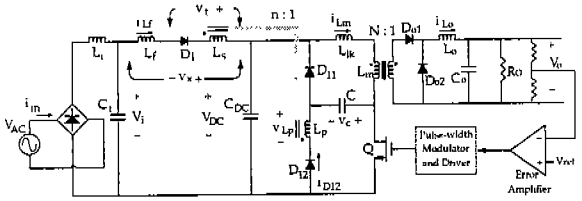


Fig.1. Proposed high power factor converter with a magnetic coupled nondissipative snubber

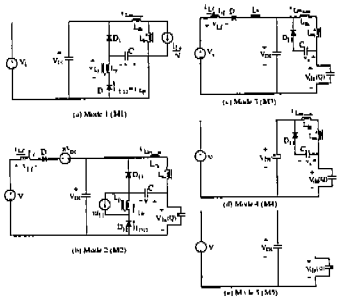


Fig.2. Topological sequences for different operation stage of the proposed converter

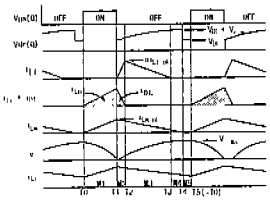


Fig.3. Steady-state waveforms of the proposed converter

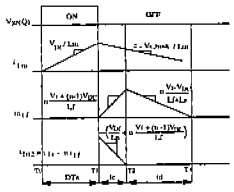
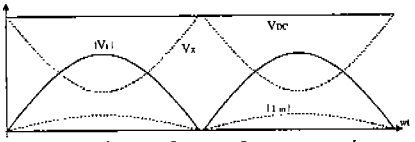
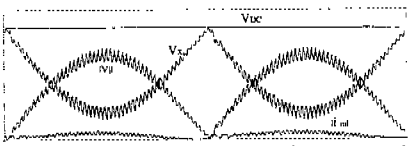


Fig.4. Current waveforms with their slopes



(a) Required waveforms of power factor correction operation



(b) Simulated waveforms of power factor correction operation

Fig.5. Idealized dc link waveforms of power factor correction operation

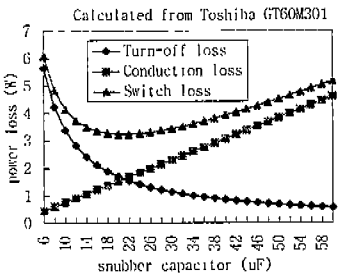


Fig.6. IGBT switch loss as a function of snubber capacitance

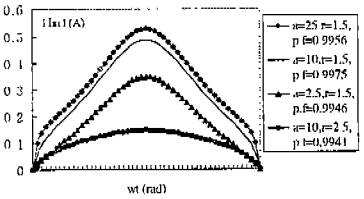


Fig.7. Rectified input current waveforms and power factor (p.f) for selected parameters (k = 3.0)

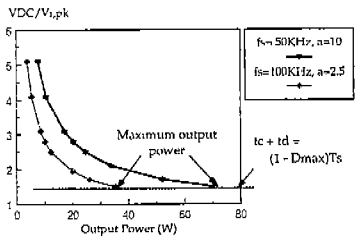


Fig.8. Dc link voltage as a function of output power for selected switching frequency and input inductor

Fig.9(a)

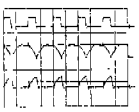


Fig.9(b)

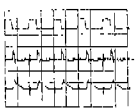


Fig.9(c)

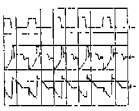


Fig.9(d)

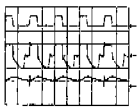
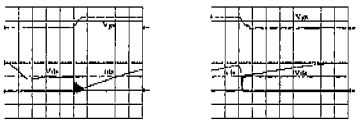
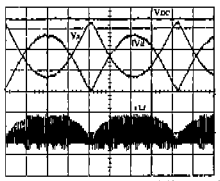


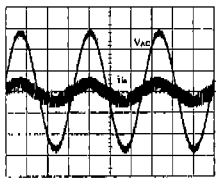
Fig.9(e)
Fig.9. Experimental waveforms of the proposed converter operating at 60V dc input



(a) Turn-on waveforms; (b) Turn-off waveforms
top : Vgs(Q) @ 20V/div; top trace: Vgs(Q) @ 20V/div
bottom : Ids(Q) @ 5A/div;bottom trace: Vds(Q) @ 100V/div
Vds(Q) @ 100V/div Ids(Q) @ 5A/div
Fig.10. Turn-on / turn-off transient waveforms of the main power switch Q



Voltage:50V/div ; Current:2A/div ; Time:2ms/div
Fig.11. Experimental dc link waveforms of power factor correction operation



Voltage:100V/div ; Current: 5A/div ; Time: 5ms/div

Fig.12. Experimental waveforms of line current and voltage

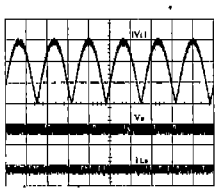
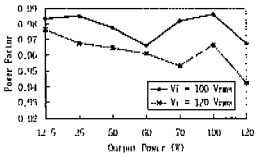
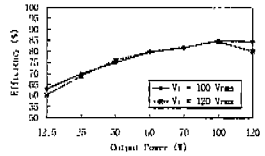


Fig. 13. Experimental waveforms of line voltage,output voltage,and output current ; top trace: Vi @ 50V/div ; Vo @ 50mV/div , Bottom trace: Io @ 50mA/div



(a) Power factor as a function of output power



(b) Overall efficiency as a function of output power
Fig.14. Power factor and overall efficiency as a function of output power

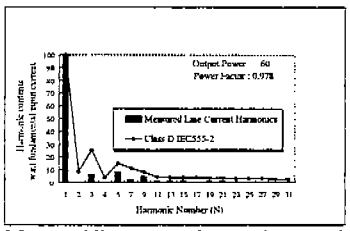


Fig.15. Measured line current harmonics superimposed on the specified IEC555-2 Class D limits