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하프 브릿지 컨버터를 기반으로 한 고효율을 갖는 고역률 정류기의 설계

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Design of High Quality Regulator with High Efficiency Based on Half-Bridge Topology

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Abstract- Design of sigle stage AC/DC converter with high power factor and high efficincy based on half-bridge topology for low power application is proposed. To obtain design equations, modelling and detailed analysis are performed. The proposed converter gives good power factor and high efficiency by employing aynchronous rectifiers. To verify the performances of the proposed converter 90W-converter has been designed. This prototype converter meets IEC555-2 requirements with near unity power factor.

1. Introduction

In order to meet the requirements in the standards such as IEC 555-2 which requires that the harmonocs of the line current stays certain level, a power factor correction(PFC) circuit is added at the utility interface of an ac-dc switched mode power supply. It is accomplished by the addition of a dedicated AC/DC front-end converter which controls its switching device in such a manner that the input current following a sinusoidal reference, followed by an off line DC/DC converter to provide a regulated and isolated DC output[1]. While this approach has a good characteristic of power factor correction and fastoutput regulatons. it is costly and inefficient since the power is converted twice and has two independent control loops. Accordingly, the two stage approach is not desirable in low power level applications[2].

Recently many single stage approach was suggested to achieve both power factor correction and conversion from AC line to desired DC output. For a simpe converter, PFC converter based on flybak topology is available. This converter has advantages that the desired output voltage can be obtained by simple single power stage with input-output isolation and any inductor is not required for PFC[3]. However, it has high EMI noise of the line current which requires a large input filter[4]. To overcome these drawbacks several topologies are proposed. Among them SEPIC[4,5] and BIFRED[6] are most eminent. These converter inherently draw a line current waveform of a high current waveform of high quality in a discontinuous conduction mode(DCM) and provide isolated DC output. Unfortunately SEPIC and BIFRED have undesirable characteristics cspecially in a low voltage applications such as computer power supplies and other electronic equipments that these toplogies have a large low frequency output voltage ripple, which requires a large output filter and cannot obtain a high efficiency due to switching loss and rectification loss.

In this paper, design of AC/DC PFC converter

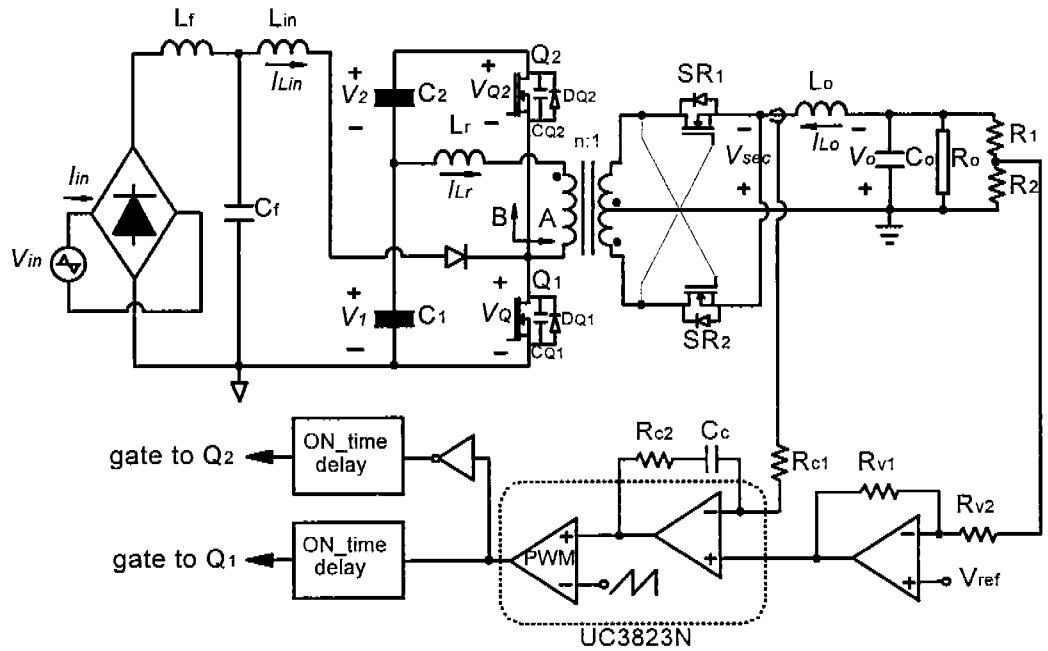

Fig. 1 Schematic of AC/DC converter based on half-bridge converter

based on half bridge topology suitable for low power level application is introduced. This converter is capable of drawing a high quality AC line current waveform and pure DC output voltage without a significant 120Hz ripple. The voltage and curent stress on active components of the proposed converter are relatively low compared to conventional converters with one switch. This leads to the increase of overall efficiency by use of low rating switches which have low on-resistance.

In converters with low output voltage, it is quite difficult to obtain a high efficiency due to the rectification loss of the output stage. Rectification loss in a conventional 100W DC/DC converter is approximately 50% of total loss. One of the suitable method to keep the effciency to a desired level is synchronous rectifiers by which the almost voltage drop is substituted with a resistance type voltage drop(R_{DSON})[7]. So synchronous rectifiers are adopted for output rectification method of the proposed converter.

The modelling employing the averaing method and detailed analysis are performed to derive design equations of power stage. By use of these design equations, the optimal design procedure is suggested and zero voltage switching(ZVS) condition to improve the efficiency is derived. According to the design procedure. a prototype AC/DC converter suitable for low power level application is designed and experimented

2. Operation principle.

The basic structure of the proposed converter can be understood as a cascade connection of s boost converter followed by a half-bridge converter with asymmetrical controll[8]. Fig. 1 shows the proposed converter. Figs. 2 and 3 are key waveforms and equivalent circuitsfor mode analysis. To illustrate the steady-state operation, several assumption are made:

(a) The switches Q_1 and Q_2, are ideal except for the output capacitance and internal diode.

(b) The parasitic capacitance of the transformer is ignored

(c) The output filter inductor is so large enough to be treated as a constant current source during switching mode.

Mode 1

Q_1 is conducting and the input inductor current I_{Lin} linearly increased with the slope of $|V_{in}|/L_{in}$ The power, however, is not delivered to the output because transformer is shorted and the output current $I_{Lo}(t)$ still freewheels through the internal diodes of Mosfets used as synchronous rectifiers and transformer

This mode stops when the leakage inductor

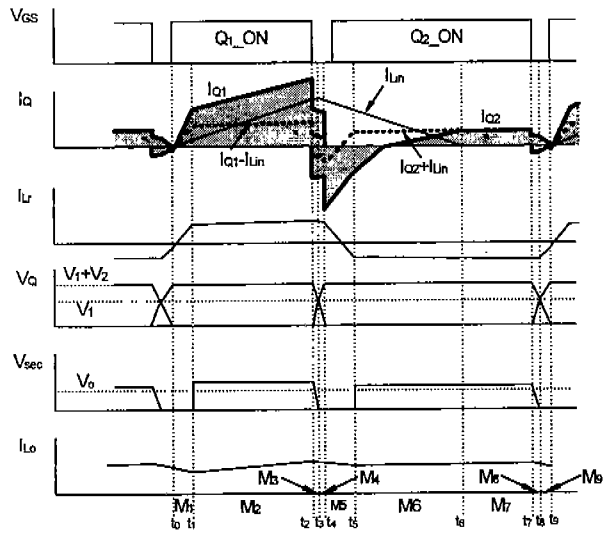

Fig.2 Key waveforms for mode analysis

current $I_{Lr}(t)$ expressed in eq. (1) reaches I_{Lo}/n.

$$I_{Lr}(t) = -I_{Lo1} + \frac{V_{in}}{L_{in}} t \tag{1}$$

where I_{Lo1} is

$$I_{Lo1} = \sqrt{\left(\frac{I_{Lo}}{n}\right)^2 - \left(\frac{V}{Z}\right)^2} \tag{2}$$

and Z is $\sqrt{\frac{L_r}{2C_Q}}$.

This initial condition can obtained using eq. (12).

Mode 2

Mode 2 begins when the voltage in the secondary of the transformer reaches $(V_1 - L_r \frac{di}{dt}) \cdot \frac{1}{n}$ and the power is delivered to the output. Since switch Q_1 has the role of charging the inductor L_{in} in the boost converter and delivering the power to the output in the half-bridge converter, the current flowing in Q_1 is the sum of the charging current of L_{in} and the output current reflected to the primary of the transformer as follows:

$$I_{Q1}(t) = \frac{I_{Lo}}{n} + \frac{|V_{in}|}{L_{in}} t \tag{3}$$

Mode 3

Q_1 is turned off, but the power is transferred to the output ,which leads the output current reflected to the primary in the transformer to flow in L_r since $V_{CQ1}(t)$ is less than V_1. Thus the output capacitance of Q_1 is charged rapidly by $I_{Lr}(t)$ and I_{Lo}/n and $V_{CQ1}(t)$ can be expressed as:

$$V_{CQ1}(t) = \frac{I_{Lo}/n + I_{Linpk}}{2C_Q} t \tag{4}$$

Mode 3 continues until $V_{CQ1}(t)$ reaches V_1.

Mode 4

After $V_{CQ1}(t)$ increases over V_1, the output current starts freewheeling. $I_{Lr}(t)$ starts decreasing in the resonant manner of L_r and C_Q which lead to the decrease of the slope of $V_{CQ1}(t)$. In this mode $I_{Lr}(t)$ and $V_{CQ1}(t)$ can be written in eqs. (5) and (6):

$$I_{Lr}(t) = \left(\frac{I_{Lo}}{n} + I_{Linpk}\right)\cos\left(\sqrt{\frac{1}{2L_rC_Q}}\, t\right) - I_{Linpk} \tag{5}$$

and

$$V_{CQ1}(t) = \left(\frac{I_o}{n} + I_{Linpk}\right) Z \sin\left(\sqrt{\frac{1}{2L_rC_Q}}\, t\right) \tag{6}$$

Mode 5

$V_{CQ1}(t)$ reaches V_1+V_2 and the internal diode of Q_2 starts conducting, which results that all $I_{Lr}(t)+I_{Lin}(t)$ flow through this internal diode. As can be seen in the key waveforms, ZVS condition of Q_2 is sufficiently satisfied since $V_{CQ2}(t)$ is sustained at zero and the switch current i_{Q1} flows in the negative. In this mode i_{Lr} decreases linearly with the slope of $-V_2/L_r$ until it reaches $-I_{Lo}/n$ and can be expressed as:

$$I_r(t) = I_{Lo5} - \frac{V_2}{L_r} t \tag{7}$$

where I_{Lo5} is

$$I_{Lo5} = \sqrt{\left(\frac{I_{Lo}}{n} + I_{Linpk}\right)^2 - \left(\frac{V}{Z}\right)^2} - I_{Linpk} .$$

This initial condition can be obtained by eqns 5 and 6.

Mode 6

After $I_{Lr}(t)$ decreases to $-I_{Lo}/n$, the energy stored in the capacitor C_2 is transferred to the load. The impedances seen from A and B respectively are

$$|Z_A| = n^2 \sqrt{\frac{(R_o - \omega^2 L_o C_o R_o)^2 + (\omega L_o)^2}{1 + (\omega R_o C_o)^2}} \tag{8}$$

$$|Z_B| = \frac{2}{\omega C} \tag{9}$$

where ω is a line frequency in rad/sec.

Since Z_A is much larger than Z_B all $I_{Lin}(t)$ flows through the internal diode of Q_2 with the slope of $[|V_{in}|-(V_1+V_2)]/L_{in}$, which results that the input

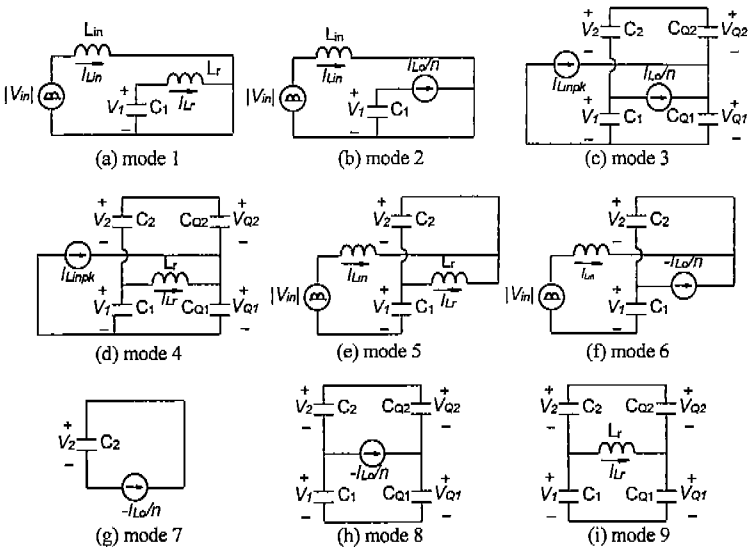

Fig. 3 Equivalent circuits for each mode

current $I_{Lin}(t)$ does not influence on the output voltage ripple. As a result, this converter can perform the output regulation and power factor correction independently. This mode stops when $I_{Lin}(t)$ expressed in eq. (10) reaches zero.

$$I_{Lin}(t) = I_{Linpk} + \frac{|V_{in}| - (V_1 + V_2)}{L_{in}} t \qquad (10)$$

Mode 7

Once $I_{Lin}(t)$ reaches zero, the operation of this mode is identical to that of tha conventional half-bridge converter with the asymmetrical control.

Mode 8 and 9

The operations in these modes are also identical to those of the conventional half-bridge converter. $V_{CQ2}(t)$, however, rises more slowly than $V_{CQ2}(t)$, since the output capacitance of Q_2 is charged only by $I_{Lr}(t)$. In mode 8 and 9, expressions of $V_{CQ2}(t)$ are respectively are

$$\begin{cases} V_{CQ2}(t) = \dfrac{I_{Lo}}{2C_Q n} t \\ I_{Lr}(t) = \dfrac{I_{Lo}}{n} \end{cases},$$

during $V_{CQ2}(t) \le V_2$ (11)

and

Mode	Time interval
Mode 1	$t_{M1} = \dfrac{(I_{Lo1} + I_{Lo}/n)L_r}{V_1}$
Mode 2	$t_{M2} = D T_s - t_{M1}$
Mode 3	$t_{M3} = \dfrac{2C_Q V_1}{I_{Linpk} + I_{Lo}/n}$
Mode 4	$t_{M4} = \sqrt{2L_r C_Q} \sin^{-1}\left(\dfrac{V_2}{(I_{Lo}/n + I_{Linpk})Z} \right)$
Mode 5	$t_{M5} = \dfrac{(I_{Lo4} + I_{Lo}/n)L_r}{V_2}$
Mode 6	$t_{M6} = \dfrac{L_{in} I_{Linpk}}{V_1 + V_2 - V_{in}}$
Mode 7	$t_{M7} = (1-D) T_s - t_{M4} - t_{M5} - t_{M6}$
Mode 8	$t_{M8} = \dfrac{2C_Q n V_2}{I_{Lo}}$
Mode 9	$t_{M9} = \sqrt{2L_r C_Q} \sin^{-1}\left(\dfrac{nV_1}{I_{Lo}Z} \right)$

Table 1 Time intervals of each mode

$$\begin{cases} V_{CQ2}(t) = \dfrac{I_{Lo}}{n}\sqrt{\dfrac{L_r}{2C_Q}} \sin\left(\sqrt{\dfrac{1}{2L_r C_Q}}\, t\right) \\ I_{Lr}(t) = \dfrac{I_{Lo}}{n} \cos\left(\sqrt{\dfrac{1}{2L_r C_Q}}\, t\right) \end{cases}$$

during $V_2 < V_{CQ2}(t) \le V_1 + V_2$ (12)

Using eqs. from (1) to (12), time interval of each mode is obtained as shown in Table 1.

3. Modelling

Design of the proposed converter begins with

deriving model equations. To do this following assumptions are made :

(A) C_1 equals to C_2 with a value of C.

(B) C_{Q1} equals to C_{Q2} with a value of C_Q.

(C) Dead times are negligible.

Averaging over one switching cycle provides the overall action of the proposed converter. The resulting large signal equations are given in eqs. from (13) to (17).

$$v_1 + v_2 \equiv v_C \tag{13}$$

$$\dot{i}_{Lin} = \frac{1}{R_e}\left(|v_{in}| + \frac{v_{in}^2}{v_C - |v_{in}|}\right) \tag{14}$$

$$\dot{v}_C = -\frac{i_{Lo}}{nC} + \frac{1}{CR_e}\left(\frac{v_{in}^2}{v_C - |v_{in}|}\right) \tag{15}$$

$$\dot{i}_{Lo} = -\frac{(1-D)v_C - nv_o}{L_o n}D + \frac{Dv_C - nv_o}{L_o n}(1-D) \tag{16}$$

$$\dot{v}_o = \frac{i_o}{C_o} - \frac{v_o}{R_o C_o} \tag{17}$$

where $R_e = \frac{2L_{in}}{D^2 T_s}$

4. Design

4.1 Selection of L_{in}

To determin the value of L_{in}, steady state analysis must be performed previosly. The steady state equations of link capacitor voltage V_C and output capacitor voltage V_o are obtained by averaging thse state equations from (14) to (16) over half of a line cycle. Assuming that the duty ratio D and switching period T_s are constant, the high frequency average model equations are again averaged over half of a line cycle to get the solutions of V_C and V_o. The solutions are

$$V_C = \frac{V_{inrms}}{\sqrt{2}}\left(1 + \sqrt{1 + \frac{0.852n^2D^2R_o}{L_{in}f_s D(1-D)}}\right) \tag{18}$$

and

$$V_o = \frac{2V_C D(1-D)}{n} \tag{19}$$

To maintain a sinusoidal line current, the converter must operate in discontinuous conduction mode(DCM) over entire cycle. This condition requres that I_{Lin} reaches to zero before the end of the switching period T_s. expressed as

$$I_{Linpk} = \frac{V_{inpk}}{L_{in}}DT_s = \frac{V_C - V_{inpk}}{L_{in}}D_a T_s \tag{20}$$

where D_a is the time ratio at which I_{Linpk} reaches zero when switch Q_1 turns off and must be less than $1-D$ to meet the discontinuous conduction condition.

Thus DCM condition is

$$D_a \le 1 - D \tag{21}$$

where $D_a = \frac{V_{inpk}}{V_C - V_{inpk}}D$

From eqs. (18), (19) and DCM condition (21). the design guideline of L_{in} is

$$L_{in} \le \frac{3.408D^3(1-D)R_o V_{inrms}^2}{2f_s V_o^2 - 2f_s V_o^2(1-D)} \tag{22}$$

4.2 Selection of switches and transformer turns ratio n

Using eqs. (18) and (19), the link capacitor voltage in steady state is derived as follows:

$$V_C = \frac{2\sqrt{2}V_{inrms}L_{in}f_s V_o^2}{2L_{in}f_s V_o^2 - 3.408D^3(1-D)R_o V_{inrms}^2} \tag{23}$$

Thus, the voltage stress on switches Q_1 and Q_2 becomes

$$V_{Q1} = V_{Q2} = V_C \tag{24}$$

Another factor to select switches is the current stress. The current stresses on Q_1 and Q_2, however, are different since the current of switch Q_1 is the sum of the boost inductor current and that of switch Q_2 is the difference of those two currents. Therefore selection of switch is based on Q_1 and eq. (25) shows the peak current flowing in Q_1.

$$I_{Q1} = \frac{V_{inpk}}{L_{in}}DT_s + \frac{I_{Lo}}{n} + \frac{(1-D)V_s}{n^2 L_o}\frac{DT_s}{2} \tag{25}$$

Since the turns ratio n, in general, is so large that the last term of eq. (25) can be negligible, this equation is rewritten as follows:

$$I_{Q1} \approx \frac{V_{inpk}}{L_{in}}DT_s + \frac{I_{Lo}}{n} \tag{26}$$

Hence the designer should choose switches which satisfy eqs. (23), (24) and (26).

The transformer turns ratio n can be chosen using eqs. (19) and (23) with the predetermined value of L_{in}.

4.3 Selection of L_r

To improve the efficiency of a converter, zero voltage switching(ZVS) of switches are nccessary. This condition depends on the switch

output capacitance and the leakage inductance. As shown in Fig. 2 the ZVS of Q_2 is accomplished very easily from the fact that the energy of the output capacitance of Q_2 is discharged by the large current $I_{Lin}+I_{Lr}$. However it is relatively difficult for Q_1 to be turned on softly since only I_{Lr} remains. So, it is sufficient that design of L_r is focused on only the ZVS condition of Q_1. From mode 8 and 9 in Fig. 2, Q_1 is turned on at zero voltage provided that

$$t_{M8}+t_{M9}\le t_{M8}+t_{i_L=0} \tag{27}$$

where $t_{i_L=0}$ means the time at which I_{Lr} expressen in eq. (12) decrease to zero. With eq. (18), and inequality (27),

$$\frac{V_1 n R_o}{V_o}\sqrt{\frac{2C_Q}{L_r}}\le 1 \tag{28}$$

is obtained.

To maintain balaced volt second on the power transformer primary V_1 must be $(1-D)V_c$. Therefore, with eq. (18), inequality (28) and this relationship the ZVS condition of Q_1 can be written in inequality (29)

$$F\le 1 \tag{29}$$

where

$$F\equiv\frac{n\sqrt{C_Q}R_o(1-D)V_{inrms}}{\sqrt{L_r V_o}}\left(1+\sqrt{1+\frac{0.852n^2D^2R_o}{L_{in}f_sD(1-D)}}\right).$$

This inequalty is the function of load resistor R_o and duty ratio D. Duty ratio according to load variation can be calculated using eqs. (18) and (19). The relationship between R_o and D is

$$1.704nV_{inrms}^2R_o(D^4-D^3)+2\sqrt{2}\,V_oL_{in}f_sV_{inrms}(D^2-D)+nV_o^2L_{in}f_s=0 \tag{30}$$

Finally, the design equation of L_r is

$$L_r\ge\left[\frac{n\sqrt{C_Q}R_o(1-D)V_{inrms}}{V_o}\left(1+\sqrt{1+\frac{0.852n^2D^2R_o}{L_{in}f_sD(1-D)}}\right)\right]^2 \tag{31}$$

4.4 Selection of L_o

Define

$$t_1=t_{M3}+t_{M4}+t_{M5} \tag{32}$$

$$t_2=t_{M8}+t_{M9}+t_{M1} \tag{33}$$

then the peak to peak output current ripples are determined in eqs. (34) and (35).

$$\Delta I_{Lo1}=(DT_s-t_2)\left|\frac{(V_1/n-V_o)}{L_o}\right| \tag{34}$$

$$\Delta I_{Lo2}=[(1-D)DT_s-t_1]\left|\frac{(V_1/n-V_o)}{L_o}\right| \tag{35}$$

If the maximum duty ratio is limited in 0.5, ΔI_{Lo1} is greater than ΔI_{o2}. Thus, the design guideline of the output inductor L_o can be made as :

$$L_o=\frac{(DT_s-t_2)|(V_1/n-V_o)|}{\Delta I_{o1}} \tag{36}$$

4.5 Selection of synchronous rectifiers

It is a well-known fact that when a Mosfet is used for output rectifier, power losses are caused by its R_{DSON} resistance. However, the output power is dissipated by not only R_{DSON} but also diode voltage drop V_{DSON} since Mosfet can not turned on during the transformer secondary voltage is below the threshold voltage of Mosfet, V_{th}. In mode 3 and mode 8 the secondary voltage is able to be written eq. (37)

$$V_{sec}=\begin{cases}\frac{1}{n}\left(V_1-\frac{I_{Linpk}+I_{Lo}/n}{2C_Q}t\right) & \text{for } t_{M3}\\ \frac{1}{n}\left(V_2-\frac{I_{Lo}/n}{2C_Q}t\right) & \text{for } t_{M4}\end{cases} \tag{37}$$

By equating (37) to V_{th} the diode conduction time intervals are

$$t_{ON1}=t_{M3}+t_{M4}-\frac{2(V_1-nV_{th})C_Q}{I_{Linpk}+I_{Lo}/n} \tag{38}$$

and

$$t_{ON2}=t_{M8}+t_{M9}-\frac{2(V_2-nV_{th})C_Q}{I_{Lo}/n} \tag{39}$$

Thus, the desigh equation to select of a Mosfet used for rectifier is made as:

$$P_{loss}=I_{Lo}{}^2R_{DSON}\left(1-\frac{t_{ON1}+t_{ON2}}{T_s}\right)+I_{Lo}V_{DSON}\left(\frac{t_{ON1}+t_{ON2}}{T_s}\right) \tag{40}$$

5. Desigh Example

To validate the above design equations, aconverter has been desinged for the specifications :

rms input voltage : $80V_{rms}$ - $150V_{rms}$
output voltage : 5V
output power : 25W - 90W
switching frequency : 100kHz

The worst-case of DCM and current stress

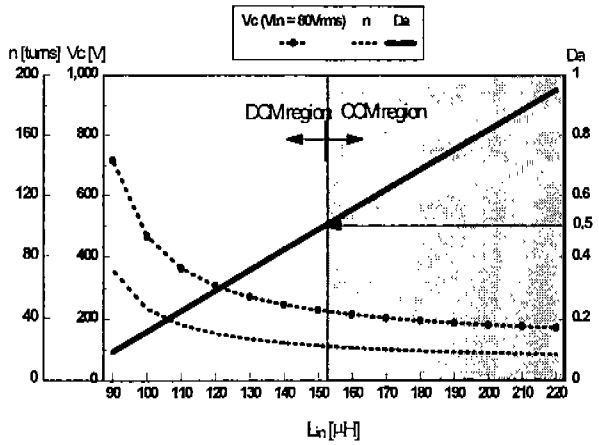

Fig. 4 Link voltage V_c, transformer turns ratio n and D_a versus L_{in} at the worst-case of DCM(V_{in}=80V_{rms}, P_o=90W, D=0.5)

occurs with maximum power throughput

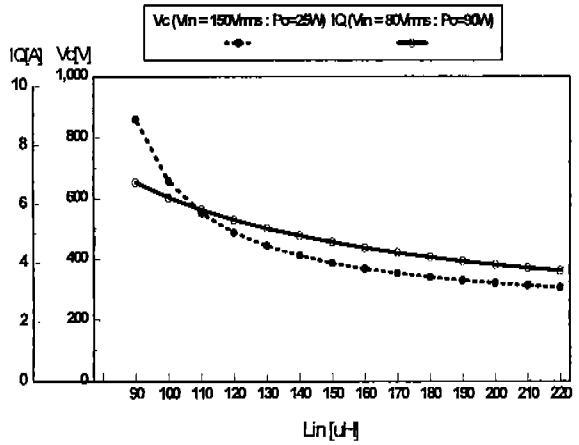

Fig. 5 Maximum current and voltage stresses versus L_{in}

(minimum load resistor) and minimum line voltage at maximum duty ratio. Also switches have the maximum voltage stress at maximum input voltage and minimum power throughput. Fig. 4 shows the link capacitor voltage V_c, transformer turns ratio n and Da using eqs. (19) (21) and (23) with V_{in}=80V_{rms} and P_o=90W (R_o=0.278Ω) at D=0.5 as a function of boost inductor L_{in}. The critical value of L_{in} is calculated as 151.6μH from eq. (22). In this design we have used 150μH for L_{in}. Base on this value, n=22.87 is able to be obtained with V_c=228.7V from eqs. (19) and (23).

Maximum voltage stress at V_{in}=150V_{rms} and P_o=25W (D=0.175) and maximum current stress

Switching frequency(f_s)	100kHz
Switches(Q_1,Q_2)	IRFP450
Synchronous rectifiers(SR_1,SR_2)	SMP60N03-10L
Input Inductor(L_{in})	150uH
Output inductor(L_o)	5uH
Filter inductor(L_f)	80uH
Link capacitors(C_1,C_2)	220uF
Output capacitor(C_o)	330uF
Filter capacitor(C_f)	0.1uF
Diodes	S30L60
Bridge diode	D6SB60L
PWM chip	UC3823N
Transformer turns ratio(n:1)	22:1

Table 2. the components of the prototype converter

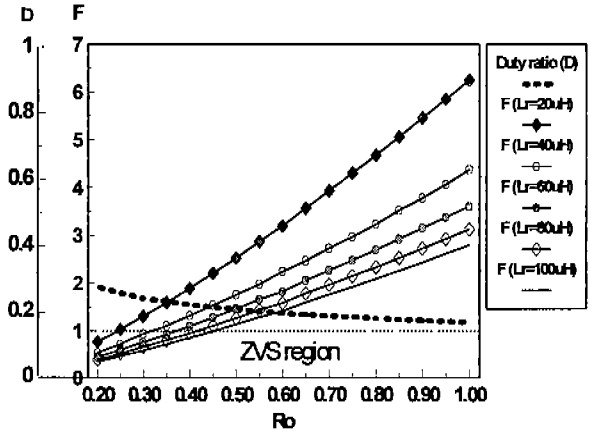

Fig. 6 ZVS condition under load and L_{in} variations

at V_{in}=80V_{rms} and P_o=90W (D=0.5) are depicted in Fig. 5 from eqs. (23) and (26). By using the predetrmined value of L_{in}=150μH, the maximum voltage and current stresses are 387.08V and 4.56A respectively. In the selection of switches, Additional voltage from rining effect caused by transformer leakage inductance must be considered. A possible choice is the *IRFP450*, which has BV_{DSS}=500V and $I_{D(on)}$=13A.

Fig. 6 shows the duty ratio D and ZVS condition according to load resistor R_o and leakage inductance L_r using eqs. (29) and (30). As can be seen in this figure the larger L_r becomes the more widely the load is able to be changed with ZVS. If a large L_r is selected to meet the ZVS condition in the wide load variation, the freewheeling interval becomes wider and the powering interval smaller. This results that the current stress of switches grow higher

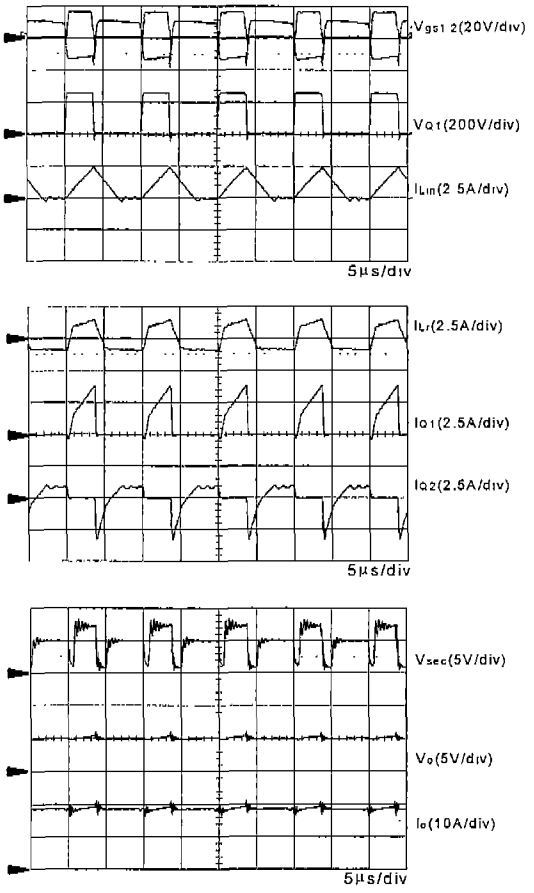

Fig. 7 Experimental waveforms at a 110V_{DC} input voltage

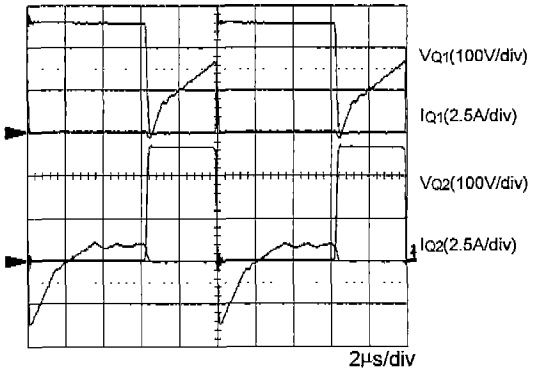

Fig. 8 Experimental waveforms of drain-to-source voltage superimposed on the current flowing in switches

to obtain the same output power. So it lies with a designer to select a value of L_r with the consideration of load variation range with ZVS and the currrent stress of switches. In this design 40uH is selected.

In the prototype converter design current ripple and rectification power loss should not pass

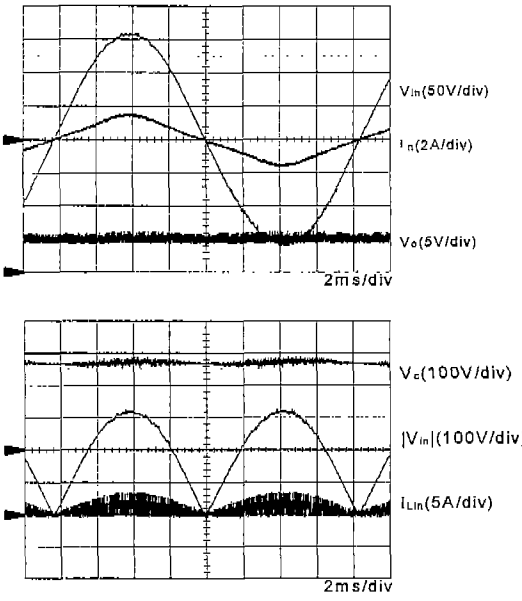

Fig. 9 Experimental waveforms of an line current/voltage, output voltage, and link voltage at V_{in}=110V_{rms} and P_o=90W

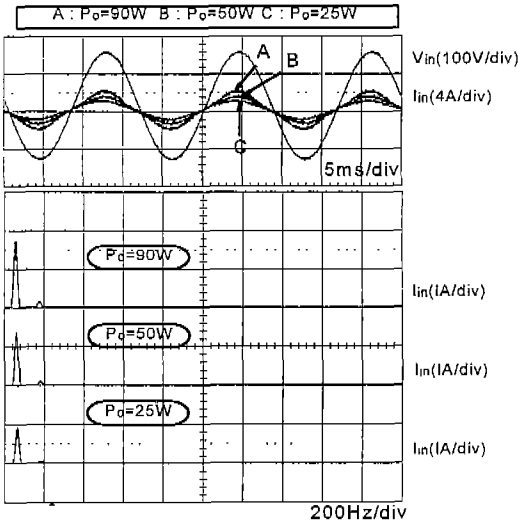

Fig. 10 Experimental waveforms of line current/voltage under load variations and their FFT results

over 2A and 5W respectively. From eqs. (36) and (40) the minimum L_o and the maximum R_{DSON} are 3.34uH and 10mΩ. Thus, this prototype converter is implemented with L_o=5uH and *SMP60N03-10L*
which has R_{DSON}=10mΩ. Table 2 lists the components of the prototype converter

6. Experimental results.

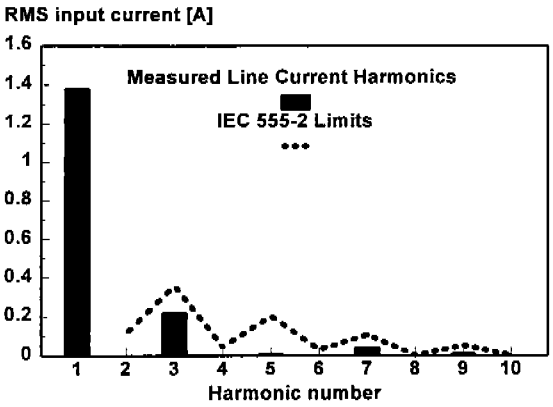

Fig. 11 The measured line current harmonics superimposed on IEC555-2 class-D limits

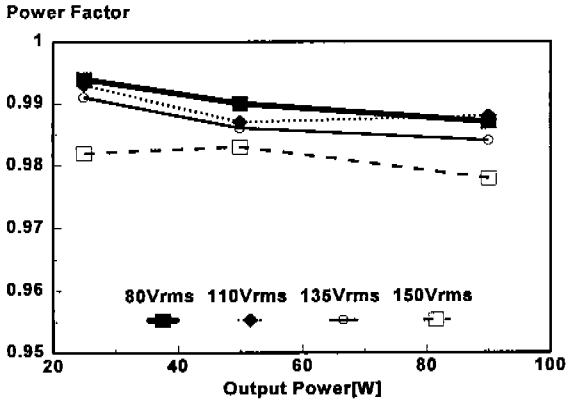

Fig. 12 Power factor under load and line voltage variations

Fig. 7 shows the measured key waveforms and Fig. 8 shows the drain to source voltage of the switches Q_1, Q_2 superimposed on current flowing in the switches at V_{in}=110V_{rms}. It can be seen that all the waveforms are agree with the theoretical analysis and design and the ZVS condition is achieved. The experimental wave forms of the line current/voltage, output voltage, input inductor currnet as well as the link voltage at V_{in}=110V_{rms} are depicted in Fig. 9. As can be seen in this figure, the filtered line current follows the line voltage well without phse difference. From Figs. 10 and 11 this converter meets the IEC555-2 class-D limit successfully. Fig. 12 shows the power factor under load and input variations. From this figure the power factor can be obtained above 0.98. Fig. 13 shows that the efficiency at rated condition is about 85%.

7. Conclusion

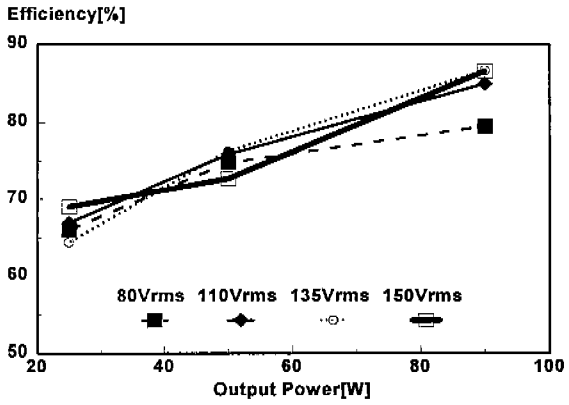

Fig. 13 Efficiency of the proposed converter under load and line voltage variations

In this paper, the desigh equations of single stage PFC AC/DC converter for low power level application based on half bridge topology is proposed. By using design equations design of 90W converter is performed. It gives the good power factor, low harmonic distortion, and high efficiency. The experimental results show that the prototype converter meets IEC555-2 class-D limits. The power factor is above 0.98 and the efficiency around 85% at rated condition.

8. References

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