A *PSpice* Modeling of PFC Circuit Using Soft-Switched Boost Converter

H.S. Mok, G.H Choe,   S.E. Jeong,   J.Y. Choi,
Kon-Kuk Univ.   Hanyang Univ.   Korea Institute of
Science and Technology.

Abstract

Single-phase and three-phase AC to DC power converters are becoming frequently used for high voltage/high power applications such as telecommunications. They often require input/output transformer isolation for safety, a unity input power factor for minimum reactive power, free input harmonic currents fed back to the AC power distribution system and, finally, high efficiency and high power density for minimum weight and volume. The proposed boost converter for power factor correction (PFC) provides a unity input power factor, low harmonic distortion and high efficiency along with reduced volume and weight. Single-phase 220VAC input/380VDC 1KW output prototype is constructed and experimental results will be verified with those of *PSpice* simulation.

I. Introduction

In most power electronics applications, the power input is in the form of 60Hz sine wave ac voltage provided by the electric utility company, which is converted desired dc output voltage. Increasingly, the recent trend is to use diode rectifiers at the first converting stage to convert the ac input to dc with large capacitor connected as a filter on the dc side to reduce dc side ripple. However, this large size filter capacitor gets charged to the peak of the ac input voltage drawing highly distorted current from the utility. But recently, harmonic pollution of the utility becomes big issues and strict standards and guidelines imposes the amount of current distortion allowed into the utility, and simple diode rectifiers connected with large input capacitors

are becoming restricted. Proper circuits for single phase and three phase inputs to achieve a nearly sinusoidal current rectification at a unity power factor should be provided for a majority power electronics applications such as switch-mode power supplies. The proposed boost converter provides a unity input power factor, low harmonic distortion and high efficiency along with reduced volume and weight. Single-phase 220VAC input/380VDC 1KW output prototype is constructed and experimental results will be verified with those of *PSpice* simulation.

II. Operation Mode of ZVT-PWM Boost Converter

The implementation of the power factor correction (PFC) circuit with DC output rectification has been popular recently and an attempt was made combining both PFC and zero-voltage-transition (ZVT) for better efficiency and reduced harmonic contents of the input currents. For an improved power density and higher switching frequency, ZVT technique was applied to boost converter shown in
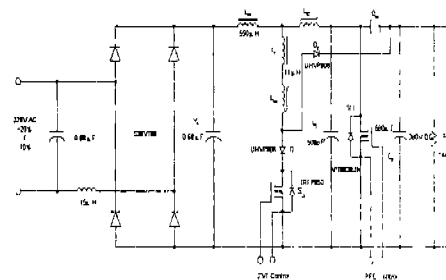

Fig. 1. 100KHz 1KW PFC Ckt. Using Boost ZVT PWM Converter

Fig. 1. This topology utilize the parasitic capacitance of the MOSFET switches and the necessary amount of inductance for resonant switching with ZVT, and its expected key voltage and current waveforms are shown in Fig. 2.
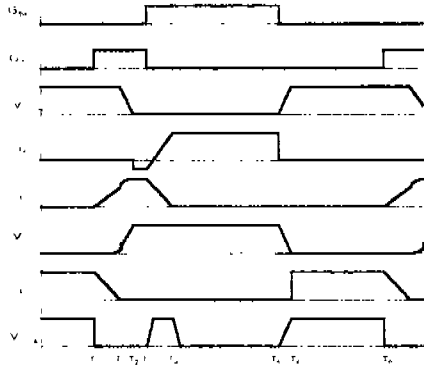

Fig. 2. Expected Key Waveforms of
the ZVT-PWM Boost Converter

There are seven operating modes within one switching cycle as shown in Fig. 3 and each operating mode is summarized as follows:
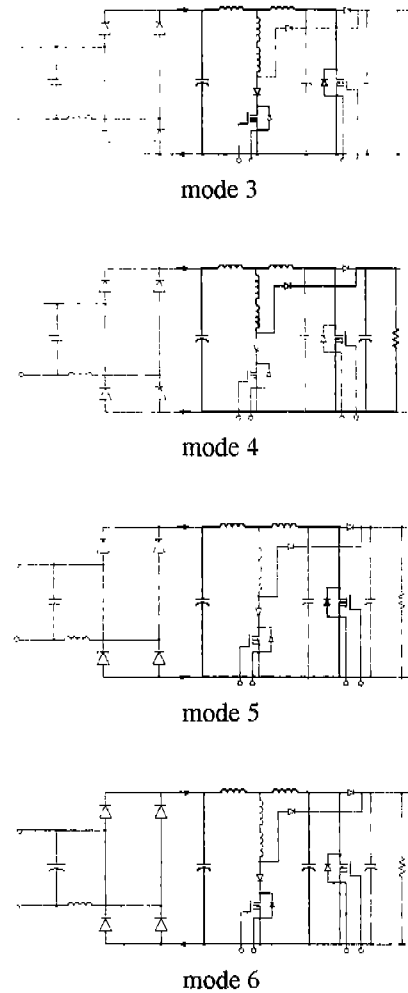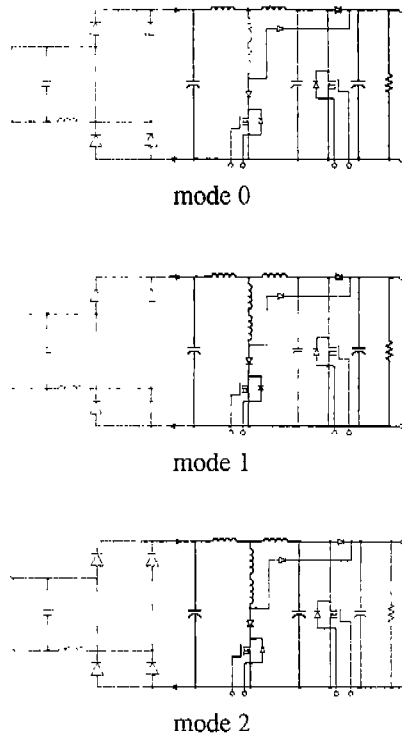

mode 0

mode 1

mode 2

mode 3

mode 4

mode 5

mode 6

Fig. 3. Operating Modes of
the ZVT-PWM Boost Converter

● mode 0 (prior to T_0): The main diode D_m is only conducting and supplying energy to the load from rectified ac source. Remaining all the other switches and diodes are turned off and L_{S2} has been saturated.

● mode 1 (T_0 - T_1): Before turning on main switch S_m, the auxiliary switch S_a starts to turn on. L_r current i_{Lr} linearly ramps up with the slope of Eqn. (1) before L_{S1} saturates and with the slope of Eqn. (2) after L_{S1} saturates.

$$\frac{di_r}{dt} = \frac{V_{IN}}{L_r + L_{S1}} \tag{1}$$

$$\frac{di_r}{dt} = \frac{V_{IN}}{L_r} \qquad (2)$$

Correspondingly, D_m current i_{Dm} is decreasing according to the above equations. However, when L_{S2} is out of saturation, i_{Dm} decreases to zero as following rate:

$$\frac{di_r}{dt} = \frac{V_{IN}}{L_r + L_{s2}} \qquad (3)$$

The resulting shape of L_r current i_{Lr} and D_m current i_{Dm} are shown in Fig. 4., which reduces unnecessary duty cycle loss in the process of achieving zero-voltage switching for main switch S_m. The required time is simplified as follows neglecting the effect of two saturable inductors L_{S1} and L_{S2}:

$$t_{01} = \frac{I_L}{\frac{V_o}{L_r}} \qquad (4)$$
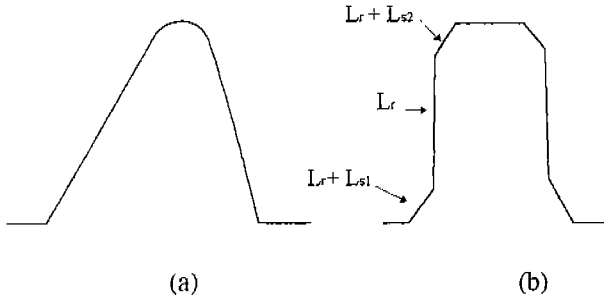

(a)   (b)

Fig. 4. Inductor Current Waveform (a) without and
(b)with two saturable inductors L_{S1} and L_{S2}

● mode 2 (T_1- T_2): When i_{Lr} reaches I_L at T_1, D_m turns off with zero-voltage and zero-current switching and C_r is discharged until the resonance brings its voltage to zero at T_2. and its anti-parallel diode of S_m starts to conduct. The minimum required interval for this period is a quarter of whole resonant cycle (T) as given:

$$t_{12} = \frac{T}{4} = \frac{\pi}{2}\sqrt{L_r C_r} \qquad (5)$$

● mode 3 (T_2- T_3): The anti-parallel diode of S_m starts to conduct and the gate signal is applied to main switch S_m at zero-voltage. The minimum time delay between S_a and S_m gate-drive turn-on signals is determined as following:

$$T_D \geq t_{01} + t_{12} = \frac{I_L}{\frac{V_o}{L_r}} + \frac{\pi}{2}\sqrt{L_r C_r} \qquad (6)$$

● mode 4 (T_3- T_4): The auxiliary switch S_a turns off at T_3, and S_m starts to conduct. The energy of L_r is transferred to the load through the auxiliary diode D_2, then, i_{Lr} decays to zero. The fast recovery diode D_1 is placed to prevent the conduction of S_a body diode due to the resonance between L_r and S_a output capacitance after T_4.

● mode 5 (T_4- T_5): The auxiliary diode D_2 turns off at zero-current switching while its reverse recovery current is limited by the saturable inductor L_{s1} and the main switch S_m fully conducts. Then, finally, the whole procedure of zero-voltage switching for main switch S_m is finished.

● mode 6 (T_5- T_6): At T_5, the main switch S_m turns off at zero voltage in charging the resonant capacitor C_r with the rate of Eqn.(7):

$$\frac{dV_{Sm}}{dt} = \frac{I_L}{C_r} \qquad (7)$$

III. Implementation of ZVT-PWM Boost Converter using PSpice

A. PFC Controller Using Peak-Current Mode Control

The ML4812 is designed to optimally facilitate a "boost" type power factor correction system. In a typical application, the ML4812 functions as a current regulator. The current which is necessary to terminate the cycle is a product of the sinusoidal line voltage times the output of the error amplifier which is regulating the output DC voltage. In order to provide stable operation in case duty cycle exceeds 50%, ramp compensation is programmable with an external resistor. Figure 5 (a) and (b) show a block diagram of ML4812 and its implementation using *Pspice*.
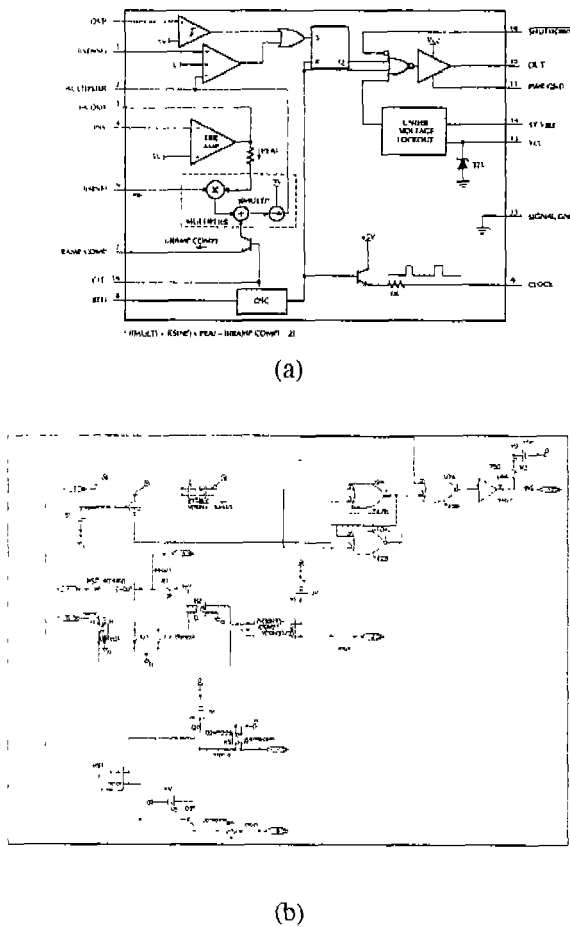
B.   Saturable Inductor

Saturable inductors are used in the proposed PFC system, which is enable to shorten the conduction time of auxiliary switch S_a. Figure 6 shows the characteristics of an ideal saturable inductor and a linear inductor below and Fig. 7 is a detailed implementation of the ideal saturable inductor.

(a)

(b)

Fig. 5. (a) Block diagram of ML4812 (b) its implementation using *Pspice*
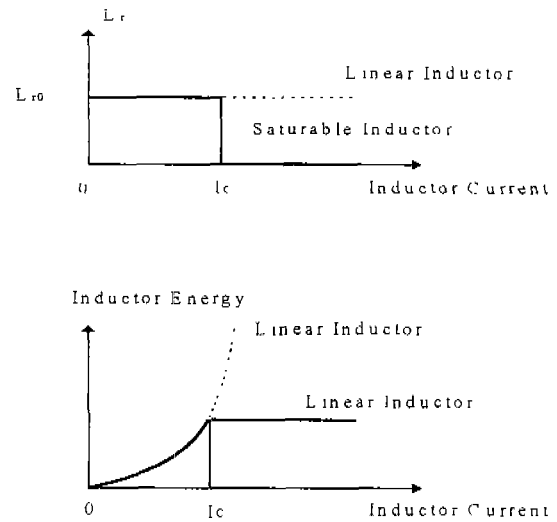

Fig. 6. Characteristics of an ideal saturable inductor and a linear inductor
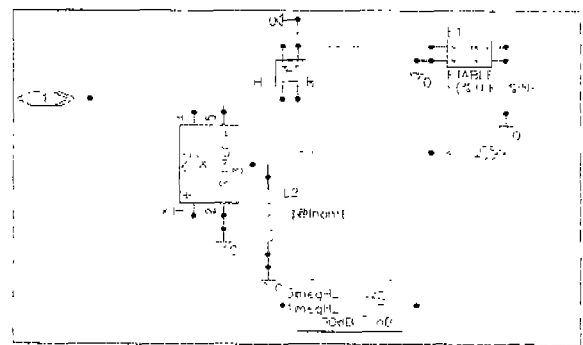

Fig. 7. a detailed implementation of the ideal saturable inductor

VI. Conclusions

At present, the cost, slightly higher power losses, and complexity of active current shaping have prevented their widespread usage. However, this may change in the future because of increased device integration leading to lower semiconductor cost, a strict enforcement of harmonic standards, and some of the advantages mentioned above. Another factor in favor of the active line-current shaping is as follows: in power supplies to computers, a sinusoidal line current is important to avoid the added kVA rating and, hence the increased cost of the UPSs, and standby diesel generators, which often supply computer systems. Therefore, ICs and other components suitable for these applications have become available, which will lower the cost of development and the components of the PFC circuit.

This paper addresses the analysis and design of three single-phase ac-to-dc converter which draws high quality input current waveforms from the ac source Compared with a hard-switching FET converter operating at 100 kHz for a single-phase, the proposed converter shows a fairly good improvements in efficiency and reducing harmonics due to the soft-switching effect.

References

|1| R.F. Brewster and A.H. Barret, "Three-phase AC to DC voltage converter with power line harmonic current reduction," U.S. Patent 4 143 414, Mar. 6, 1979.

|2| M.J. Kocher and R.L. Steigerwald, "An AC to DC converter with high quality input waveforms," *IEEE Trans. Power Electronics*, pp. 63-75, 1982.

|3| S. Manias and P.D. Ziogas, "A novel sinewave in AC to DC converter with high-frequency transformer isolation," *IEEE Trans. Ind. Electron.*, vol. IE-32, no. 4, pp. 430-438, Nov. 1985.

|4| J.A. Sabate, V. Vlatkovish, R.B. Ridly, F.C. Lee and B.H. Cho, "Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter," *Proc. of IEEE APEC 1990*, pp. 275-284.

|5| J.G. Cho, J.A. Sabate, G. Hua and F.C. Lee, "Zero-voltage and zero-current switching full-bridge PWM converter for high power applications, " *Proc. of IEEE PESC 1994*, pp. 102-108.

Appendix
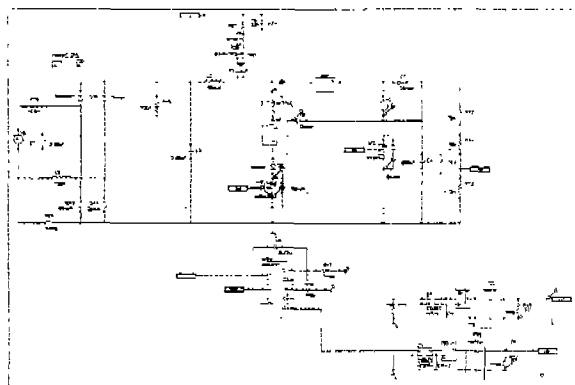
* Schematics Netlist *

R_R15	$N_0001 HS3_Isine 750k
R_R16	HS3_rampcom 0 170k
R_R17	HS3_mult 0 210k
D_HS3_D3	$N_0014 0 Dbreak
V_HS3_HS2_V2	$N_0030 0 5V
X_HS3_HS2_U2	$N_0030 vdc $N_0031
$N_0032 HS3_eaout uA741	
D_HS3_HS2_D3	HS3_eaout vdc Dbreak
V_HS3_HS2_V3	$N_0031 0 8V
V_HS3_HS2_V6	$N_0032 0
V-D_HS3_D4	$N_0015 0 Dbreak
V_HS3_V1	$N_0016 0 9V
V_HS3_V9	$N_0017 0 15V
R_HS3_R3	$N_0017 HS3_out 750
V_HS3_V7	$N_0018 0 5V
R_HS3_R2	$N_0019 HS3_clock 1k
V_HS3_V8	$N_0020 0 5V
V_HS3_V4	$N_0021 0 5V

Q_HS3_Q1 $N_0021 $N_0036
HS3_Iramp Q2N2222

G_HS3_ABM311 $N_0016 HS3_mult
VALUE { (V($N_0022)*
+ V($N_0023)
+ -V($N_0024)/2)   }

H_HS3_H2 $N_0022 0 VH_HS3_H2 1

VH_HS3_H2   HS3_Ierr $N_0015 0V

H_HS3_H1 $N_0023 0 VH_HS3_H1 1

VH_HS3_H1   HS3_Isine $N_0014 0V

H_HS3_H3 $N_0024 0 VH_HS3_H3 1

VH_HS3_H3   HS3_Iramp HS3_rampcom
0V

X_HS3_U9A $N_0035 $N_0025
$N_0026 $G_DPWR $G_DGND 7428 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0

X_HS3_U7A $N_0035 $N_0026
$N_0027 $G_DPWR $G_DGND 7428 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0

Q_HS3_Q3 $N_0020 $N_0035 $N_0019
QbreakN

X_HS3_U8A $N_0027 HS3_out
$G_DPWR $G_DGND 7407 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0

X_HS3_U10A $N_0026 $N_0028
$N_0025 $G_DPWR $G_DGND 7428 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0

V_HS3_HS1_V2 $N_0035 0
+PULSE 0 5 {1/100kHz-1u} 10n 10n {1u}
{1/100kHz}

V_HS3_HS1_V1 $N_0036 0
+PULSE 0 3.5 0 {1/100kHz-1u} {1u} 10n
{1/100kHz}

R_HS3_R1   HS3_eaout HS3_Ierr   10k

E_HS3_SUM1 $N_0029 0 VALUE
{V($N_0018)+V(HS3_mult)}

E_HS3_E1 $N_0028 0 TABLE { V(i.
$N_0029) }
+ ((-15,0) (-0.001,0) (0,0) (0.001, 5)   (15,5))

R_R21   HS3_clock 0   10k

E_SLIMIT1 $N_0040 0 VALUE
{(((30)+(0))/2) + ((((30)-(0))/2) *

+ TANH((1k)*(V($N_0002)-(((30)+(0))/2))/((((30)-
(0))/2))))}

E_SLIMIT2 $N_0038 0 VALUE
{((((30)+(0))/2) + ((((30)-(0))/2) *
+ TANH((1k)*(V($N_0003)-(((30)+(0))/2))/((((30)-
(0))/2))))}

R_HS6_R1   0 0   1meg

F_HS6_F1 $N_0038 0 VF_HS6_F1 1

VF_HS6_F1 $N_0037 pfc 0V

E_HS6_E1 $N_0037 0 $N_0038 0 1

R_HS5_R1   0 0   1meg

F_HS5_F1 $N_0040 0 VF_HS5_F1 1

VF_HS5_F1 $N_0039 zvt 0V

E_HS5_E1 $N_0039 0 $N_0040 0 1

E_E1 $N_0002 0 TABLE { V(HS3_clock,
0) }
+ ((-15,0) (-0.01,0) (1,0) (1.1,30)   (15,30))

E_E2 $N_0003 0 TABLE { V(HS3_out,
0) }
+ ((-15,0) (-0.01,0) (1,0.0) (1.1,30)   (15,30))

R_R12 $N_0005 $N_0004   178k

R_R14 $N_0004 vdc   178k

D_D8 $N_0042 $N_0005 Dbreak

D_D9   0 $N_0006 Dbreak

R_R13   vdc 0   4.75k

D_D6   0 $N_0007 Dbreak

C_C7 $N_0008 $N_0009   0.68uF

V_V6 $N_0010 $N_0009
+SIN 0 {Vrms*sqrt(2.)} 60Hz 0 0 0

D_D10 $N_0011 $N_0001 Dbreak

D_D11 $N_0008 $N_0001 Dbreak

D_D12   0 $N_0011 Dbreak

D_D13   0 $N_0008 Dbreak

R_R25 $N_0009 0   1meg

L_L5 $N_0009 $N_0011   15uH IC=3

C_C4 $N_0005 0   680uF IC=350V

M_M2 $N_0007 zvt 0 0 IRF840

H_HS7_H1 $N_0043 0 VH_HS7_H1 1

VH_HS7_H1 $N_0041 $N_0042 0V

X_HS7_X1 $N_0044 0 $N_0045
$N_0046 $N_0041 ZX

L_HS7_L2 $N_0045 0   {{Ls}}

```
E_HS7_E1          $N_0047 0 TABLE
{ V($N_0043, 0) }
+ ( (-0.3,0.0),(-0.29,0.1), (0, 1), (0.29,1), (0.3,0.1) )
E_HS7_LOPASS1          $N_0044 0
CHEBYSHEV {V($N_0047)} LP (1megHz
5megHz) 1dB
+   50dB
H_HS8_H1          $N_0050 0 VH_HS8_H1 1
VH_HS8_H1          $N_0048 $N_0049 0V
X_HS8_X1          $N_0051 0 $N_0052
$N_0053 $N_0048 ZX
L_HS8_L2          $N_0052 0   {{Ls}}
E_HS8_E1          $N_0054 0 TABLE
{ V($N_0050, 0) }
+ ( (-0.3,0.0),(-0.29,0.1), (0, 1), (0.29,1), (0.3,0.1) )
E_HS8_LOPASS1          $N_0051 0
CHEBYSHEV {V($N_0054)} LP (1megHz
5megHz) 1dB
+   50dB
C_C8          0 $N_0012   1n
R_R27          $N_0012 i   33k
R_R28          0 $N_0012   100
C_C9          $N_0012 i   47n
F_F1          0 $N_0012 VF_F1 0.005
VF_F1          $N_0013 $N_0053 0V
R_R1          $N_0005 0   144
D_D5          $N_0042 $N_0007 Dbreak
M_M3          $N_0006 pfc 0 0 IRF840
C_C2          $N_0001 0   0.68uF IC=0
C_C6          vdc HS3_eaout   0.47u
R_R19          zvt 0   1meg
R_R22          pfc 0   1meg
L_L2          $N_0001 $N_0013
550uH  IC=3.5A
V_V5          $N_0049 $N_0006 DC
0V
L_L3          $N_0053 $N_0046
{-2.*Ls+11u}
R_R26          $N_0010 $N_0008
0.01
D_D7          $N_0049 $N_0005
Dbreak
```