'97 대한전기학회 창립 50주년 하계학술대회 논문집 (PEO 6)

캐패시터를 이용한 구형파 펄스전압발생 전원장치

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Square Pulse-Power Generation Using Capacitor Energy Source

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Abstract - Depending on the energy storage-element they are categorized into two types. One is called voltage-fed type when capacitors are used as energy storage elements. The other goes by the name of current-fed which utilizes inductors as energy storage elements. This paper deals with the basic concept of pulse-power generation in the view points of load matching for the voltage-fed type.

Introduction

Pulse generators which are capable of forming square voltage-pulses based on pulse forming lines(PFL) have been widely used in the industry applications. The PFL is composed of a charging source, a closing switch and identical LC elements. The widely used ones are based on the voltage-fed PFL in which energy is stored in the electrostatic field of capacitors and the energy is discharged into a load through the closing switch. Due to the availabiliby of powerful closing switches such as spark gaps, thyratrons, ignitrons, thyristors, this voltage-fed types of pulse generators are usual practices.

I. Pulse generator with open-end forming line

The simpliest electrical scheme of a voltage-fed pulse generator is shown in Fig. 1. The followings are nomenclatures used in this paper.

V_O : charging voltage of PFL Capacitors
ρ : characteristic impedance of the PFL ; $\rho=\sqrt{L/C}$
K : pulse closing switch
R_L : resistance of the load
Z : charging current-limiting element
V_r : voltage across the load

For simplicity, it is assumed that the closing switch is ideal ; that PFL is lossless ; that the PFL is similar to line with distributed parameters (i.e. Coaxial cable).

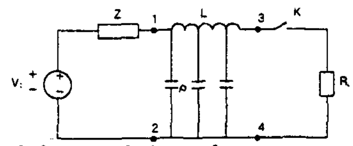

Fig. 1. Scheme of the pulse generator with PFL consisting of identical LC-elements

One of the important characteristics of the pulse generators is the amplitude of output power. To obtain the maximized output power from a given scheme, it is necessary to minimize the releasing time of the stored energy. To achieve this purpose the load R_L should be matched with the characteristic impedance ρ of PFL, that is, $\rho=R_L$.

Once the condition is satisfied, the pulse duration (the releasing time of the stored energy) is equal to two times of the one-way transmission time of the PFL, $\delta=\sqrt{LC}$, that is, $t_P=2\delta$.

Closing the siwtch K in Fig. 1. results in the equivalent circuit presented as shown in Fig. 2.

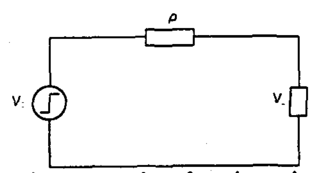

Fig. 2. Equivalent pulse-forming circuit for the pulse generator of Fig. 1.

The voltage across the load is

$$V_L = V_O \frac{R_L}{\rho + R_L}$$

If ρ is equal to R_L, the amplitude of pulse voltage across the load is $V_O/2$.

From the moment of closing K a falling wave of voltage propageates along PFL form output terminal (3-4) to its input terminal(1-2).

The amplitude of the falling wave $\Delta_1 V$ is

$$\Delta_1 V = V_L - V_O.$$

For the given condition of $\Delta_1 V = V_O/2$.

The distribution of the voltage along PFL after closing the switch K is dipicted as shown in Fig. 3.

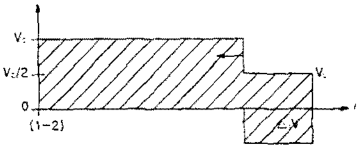

Fig. 3. Voltage along PFL after connecting the load to PFL by closing K

The falling wave with voltage of $\Delta_1 V$ is propagates along PFL to terminal (1-2) during the one-way transmission time ($\delta = \sqrt{LC}$) of the PFL, where L and C are the total inductance and capacitance of the PFL, respectively.

After arriving the input terminal (1-2), the falling wave meets a virtual open-chain circuit (because $Z \gg \rho$) and is reflected with amplitude of $\Delta_2 V$.

$$\Delta V_2 = -\Delta_1 V \frac{Z}{\rho + Z} = -\Delta_1 V \frac{1}{1 + \rho/Z} \approx -\Delta_1 V$$

The distribution of the voltage along PFL after reflecting the falling wave with voltage of $\Delta_1 V$ is shown in Fig. 4.

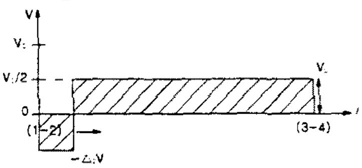

Fig. 4. Voltage distribution along PFL after reflecting the falling wave from the input terminal(1-2).

The reflected wave with voltage of $-\Delta_2 V$ propagates along PFL from the input (1-2) to the output terminal (3-4) during the time δ when it arrives at the output of the PFL, it meets the matched load R_L. By this time all the PFL energy is depleted and the process is finished. The pulse amplitude is equal to $V_O/2$.

II. Effect of the load mismatching

The *effect of the load mismatching* results in a series of voltage steps across the load. For the load condition of $R_L > \rho$ the voltage steps reduces gradually, whereas it oscilates when $R_L < \rho$. Fig. 5. shows the voltage waveforms for three different load conditions.

(a) $R_L = \rho$ (b) $R_L = 2\rho$ (c) $R_L = \frac{\rho}{2}$

Fig. 5. Pulse-voltage waveforms for the matched load (a) and the mismatched loads(b, c).

The amplitudes of each voltage steps are difined in the references [1]-[4]. It shows the minimal pulse duration for the matched load, hence, the pulse power is maximized. It also shows that the pulse duration is elongated for the mismatched load. This unintentional long pulse leads to more loss and low system-efficiency. Particulary, when the load (R_L) is less than the characterisitc impedance(ρ), the system has reactive power due to the oscilating pulse voltage.

The pulse load power for the matched load is

$$\begin{aligned} R_L &= i_L \cdot V_L \\ &= \frac{V_O}{2\rho} \cdot \frac{V_O}{2} \\ &= \frac{V_O^2}{4\rho} \end{aligned}$$

III. Summary

The basic concept for square pulse-voltage generation with a voltage-fed type has been discussed in the paper.

The load match is the key issue to obtain the optimized system which has the minimal pulse duration and the maximized pulse power.

Due to the limited space, some important issues such as double pulse forming lines, closing switch and combined systems are not covered.

These will be published in the future.

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